SGM5352-16
16-Bit, 4 Channels, Voltage-Output Digital-to-Analog Converter

GENERAL DESCRIPTION

The SGM5352-16 is a low power, 4 channels, 16-bit, voltage-output DAC. It operates from a 2.7V to 5.5V supply and the monotonicity is guaranteed by design.

The SGM5352-16 sets the output range of each DAC channel by using an external reference voltage. It incorporates a power-on reset circuit that ensures the DAC output powers to 0V.

The SGM5352-16 uses a 3-wire serial SPI interface.

The SGM5352-16 is available in Green TSSOP-16 and WLCSP-1.64×1.62-16B packages. It operates over an ambient temperature range of -40℃ to +125℃.

FEATURES

- **Power Supply Range: 2.7V to 5.5V**
- **16-Bit DAC, Monotonicity Guaranteed by Design**
- **6LSB (TYP) Relative Accuracy**
- **Low Power Operation: 0.4mA at 2.7V**
- **Power-On Reset to Zero-Scale**
- **10μs (TYP) Settling Time**
- **-100dB (TYP) AC Crosstalk**
- **Simultaneous or Sequential Output Update and Power-Down**
- **1.8V to 5.5V Logic Interface**
- **Available in Green WLCSP-1.64×1.62-16B and TSSOP-16 Packages**

APPLICATIONS

Industrial Instrumentation
Factory Automation
Process Control
Servo-Control
Data Acquisition Systems

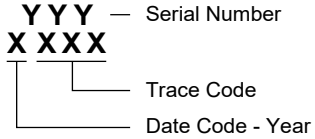
PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM5352-16	WLCSP-1.64×1.62-16B	-40℃ to +125℃	SGM5352-16XG/TR	OUA XXXX	Tape and Reel, 3000
	TSSOP-16	-40℃ to +125℃	SGM5352-16XTS16G/TR	SGM535216 XTS16 XXXXX	Tape and Reel, 4000

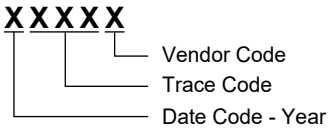
MARKING INFORMATION

NOTE: XXXX = Date Code and Trace Code. XXXXX = Date Code, Trace Code and Vendor Code.

WLCSP-1.64×1.62-16B



TSSOP-16



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Input Voltage Range ..... -0.3V to 6V
Digital Input Voltage Range ..... -0.3V to AV_{DD} + 0.3V
Output Voltage Range ..... -0.3V to AV_{DD} + 0.3V
Package Thermal Resistance
WLCSP-1.64×1.62-16B, θ_{JA} ..... 107℃/W
WLCSP-1.64×1.62-16B, θ_{JC} ..... 41℃/W
TSSOP-16, θ_{JA} ..... 94℃/W
TSSOP-16, θ_{JC} ..... 37℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 4000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Operating Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

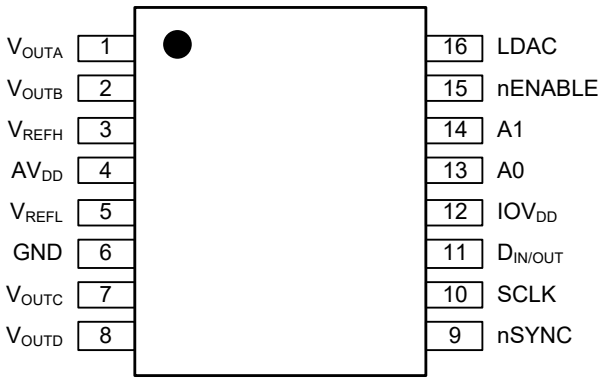
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

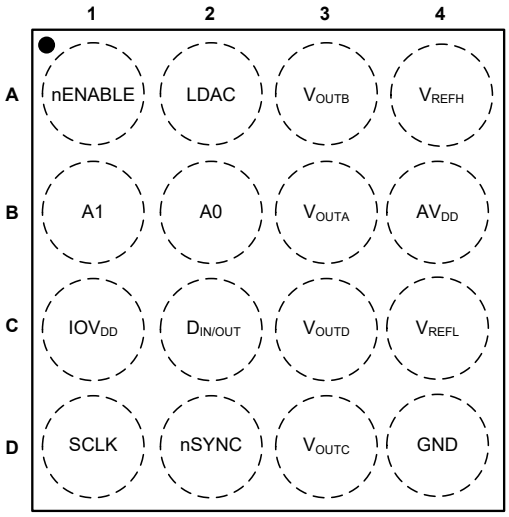
PIN CONFIGURATIONS

(TOP VIEW)



TSSOP-16

(TOP VIEW)



WLCSP-1.64×1.62-16B

PIN DESCRIPTION

PIN		NAME	FUNCTION
TSSOP-16	WLCSP-1.64×1.62-16B		
1	B3	V_{OUTA}	Analog Output DAC A.
2	A3	V_{OUTB}	Analog Output DAC B.
3	A4	V_{REFH}	Positive Reference Voltage Pin.
4	B4	AV_{DD}	Power Supply Pin. It can be operated from 2.7V to 5.5V.
5	C4	V_{REFL}	Negative Reference Voltage Pin.
6	D4	GND	Ground Pin.
7	D3	V_{OUTC}	Analog Output DAC C.
8	C3	V_{OUTD}	Analog Output DAC D.
9	D2	nSYNC	Frame Synchronization Input Pin. Active low. When this pin goes low, data can be transferred into the input shift register, or transferred out of the DAC register or data buffer.
10	D1	SCLK	Serial Clock Input Pin. The data transfer rate is up to 50MHz.
11	C2	$D_{IN/OUT}$	Serial Data Input/Output Pin. When used as the input pin, data is clocked into the 24-bit input shift register on the falling edge of SCLK; when used as the output pin, data is clocked out of the DAC register or data buffer on the rising edge of SCLK.
12	C1	IOV_{DD}	Digital I/O Power Supply.
13	B2	A0	Device Address 0.
14	B1	A1	Device Address 1.
15	A1	nENABLE	Enable Pin. Active low. Connect the SPI interface to the serial port.
16	A2	LDAC	Load DAC Registers Pin. When rising edge triggered, all DAC registers are loaded.

ELECTRICAL CHARACTERISTICS

(AV_{DD} = 2.7V to 5.5V, Full = -40℃ to +125℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Static Performance (1)						
Resolution			16			Bits
Relative Accuracy		Measured by line passing through codes 485 and 64741		6	14	LSB
Differential Nonlinearity		16-bit monotonic		0.5	1	LSB
Zero-Code Error		Measured by line passing through codes 485 and 64741		0.42	3	mV
Zero-Code Error Drift				4		μV/℃
Full-Scale Error		Measured by line passing through codes 485 and 64741, (AV_{DD} = 5.5V, V_{REF} = 5.4V) and (AV_{DD} = 2.7V, V_{REF} = 2.5V)		0.06	0.3	% of FSR
Gain Error		Measured by line passing through codes 485 and 64741, (AV_{DD} = 5.5V, V_{REF} = 5.4V) and (AV_{DD} = 2.7V, V_{REF} = 2.5V)		0.01	0.2	% of FSR
Gain Temperature Coefficient				1		ppm of FSR/℃
Power Supply Rejection Ratio	PSRR	R_L = 2kΩ, C_L = 200pF		0.1		mV/V
Output Characteristics (2)						
Output Voltage Range			0		V_{REFH}	V
Output Voltage Settling Time		R_L = 2kΩ, C_L = 500pF		10		μs
Slew Rate				1		V/μs
Capacitive Load Stability		R_L = ∞		2		nF
		R_L = 2kΩ		10		
Code Change Glitch Impulse		1LSB change around major carry		20		nV-s
Digital Feedthrough				0.1		nV-s
DC Crosstalk		Full-scale swing on adjacent channel, AV_{DD} = 5V, V_{REF} = 4.096V		0.05		LSB
AC Crosstalk		1kHz sine wave		-100		dB
DC Output Impedance		At mid-point input		0.3		Ω
Short-Circuit Current		AV_{DD} = 5V		37		mA
		AV_{DD} = 3V		35		
Power-Up Time		Coming out of power-down mode, AV_{DD} = 5V		15		μs
		Coming out of power-down mode, AV_{DD} = 3V		13		
AC Performance						
Signal-to-Noise Ratio	SNR	BW = 20kHz, AV_{DD} = 5V, f_{OUT} = 1kHz, 1st 19 harmonics removed for SNR calculation		54		dB
Total Harmonic Distortion	THD	BW = 20kHz, AV_{DD} = 5V, f_{OUT} = 1kHz, 1st 19 harmonics removed for SNR calculation		-62		dB
Spurious-Free Dynamic Range	SFDR	BW = 20kHz, AV_{DD} = 5V, f_{OUT} = 1kHz, 1st 19 harmonics removed for SNR calculation		66		dB
Signal-to-Noise and Distortion	SINAD	BW = 20kHz, AV_{DD} = 5V, f_{OUT} = 1kHz, 1st 19 harmonics removed for SNR calculation		53		dB
Reference Input						
V_{REFH} Voltage			0		AV_{DD}	V
V_{REFL} Voltage				0		V
Reference Input Current		V_{REFL} = GND, V_{REFH} = AV_{DD} = 5V		85	110	μA
		V_{REFL} = GND, V_{REFH} = AV_{DD} = 3V		50	70	
Reference Input Impedance		V_{REFL} < V_{REFH}		59		kΩ

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = 2.7V to 5.5V, Full = -40℃ to +125℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Logic Inputs (2)							
Input Low Voltage	V_{IL}	IOV_{DD} = 5.5V				1.2	V
		IOV_{DD} = 1.8V				0.4	
Input High Voltage	V_{IH}	IOV_{DD} = 5.5V		2.1			V
		IOV_{DD} = 1.8V		1.3			
Pin Capacitance					2		pF
Power Requirements							
Supply Voltage	AV_{DD}			2.7		5.5	V
Digital Input-Output Supply Voltage	IOV_{DD}			1.8		5.5	V
Supply Current	I_{DD}	Normal mode, input code = 32768, no load, reference current not included, V_{IH} = IOV_{DD} and V_{IL} = GND	IOI_{DD}		0.03	1	μA
			AV_{DD} = 5.5V		0.45	0.7	mA
			AV_{DD} = 2.7V		0.4	0.6	
		All power-down modes, V_{IH} = IOV_{DD} and V_{IL} = GND	AV_{DD} = 5.5V		0.45	4	μA
			AV_{DD} = 2.7V		0.32	4	
Power Efficiency							
I_{OUT}/I_{DD} Power Efficiency		I_L = 2mA, AV_{DD} = 5V			95		%

NOTES:

1. Linearity calculated using a reduced codes range of 485 to 64741; output unloaded.
2. Specified by design and characterization; not production tested.

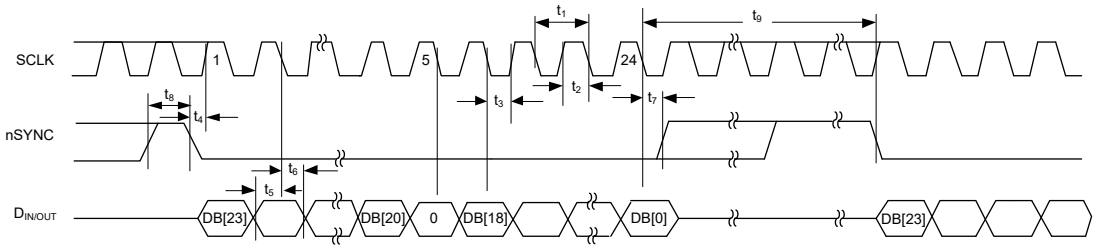
TIMING CHARACTERISTICS

(AV_{DD} = 2.7V to 5.5V, Full = -40℃ to +125℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Cycle Time (3)	t_1	IOV_{DD} = AV_{DD} = 2.7V to 3.6V	20			ns
		IOV_{DD} = AV_{DD} = 3.6V to 5.5V	20			
SCLK High Time	t_2	IOV_{DD} = AV_{DD} = 2.7V to 3.6V	10			ns
		IOV_{DD} = AV_{DD} = 3.6V to 5.5V	10			
SCLK Low Time	t_3	IOV_{DD} = AV_{DD} = 2.7V to 3.6V	10			ns
		IOV_{DD} = AV_{DD} = 3.6V to 5.5V	10			
nSYNC Falling Edge to SCLK Rising Edge Setup Time	t_4	IOV_{DD} = AV_{DD} = 2.7V to 3.6V	0			ns
		IOV_{DD} = AV_{DD} = 3.6V to 5.5V	0			
Data Setup Time	t_5	IOV_{DD} = AV_{DD} = 2.7V to 3.6V	5			ns
		IOV_{DD} = AV_{DD} = 3.6V to 5.5V	5			
Data Hold Time	t_6	IOV_{DD} = AV_{DD} = 2.7V to 3.6V	5			ns
		IOV_{DD} = AV_{DD} = 3.6V to 5.5V	5			
24th SCLK Falling Edge to nSYNC Rising Edge	t_7	IOV_{DD} = AV_{DD} = 2.7V to 3.6V	0			ns
		IOV_{DD} = AV_{DD} = 3.6V to 5.5V	0			
Minimum nSYNC High Time	t_8	IOV_{DD} = AV_{DD} = 2.7V to 3.6V	20			ns
		IOV_{DD} = AV_{DD} = 3.6V to 5.5V	20			
24th SCLK Falling Edge to nSYNC Falling Edge	t_9	IOV_{DD} = AV_{DD} = 2.7V to 5.5V	100			ns
$D_{IN/OUT}$ Tri-State to Driven	t_{10}	IOV_{DD} = AV_{DD} = 2.7V to 5.5V	15			ns
24th SCLK Falling Edge to $D_{IN/OUT}$ Tri-State	t_{11}	IOV_{DD} = AV_{DD} = 2.7V to 5.5V	0			ns

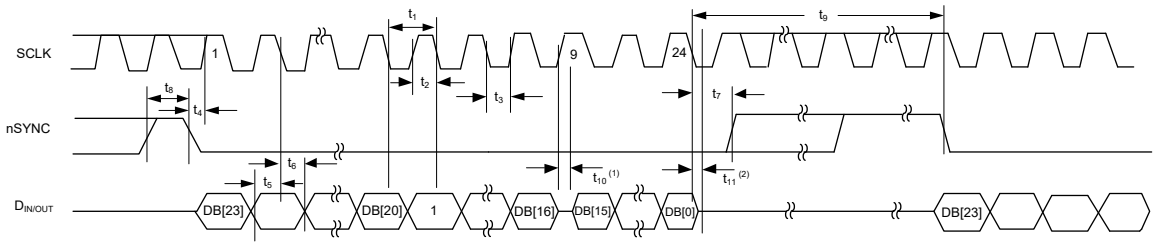
NOTES:

1. All input signals are specified with t_R = t_F = 3ns (10% to 90% of AV_{DD}) and timed from a voltage level of (V_{IL} + V_{IH})/2.
2. Refer to Figure 1 and Figure 2.
3. Maximum SCLK frequency is 50MHz at IOV_{DD} = AV_{DD} = 2.7V to 5.5V.



NOTE: 1. When DB[19] = 0, this is a write operation, the data DB[18:0] is locked into DAC on each falling edge of SCLK.

Figure 1. Serial Write Operation



NOTES:

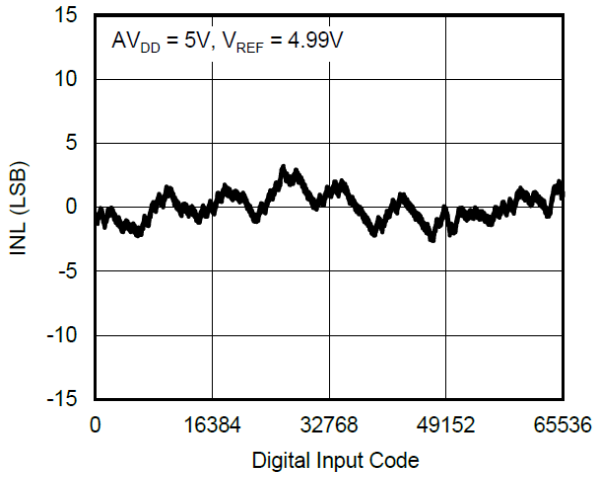
1. When DB[19] = 1, this is a read operation, the data DB[15:0] is read from DAC. On the rising edge of 9th of SCLK, the $D_{IN/OUT}$ is switched from input to output, the data of internal register is put on the bus on each rising edge of SCLK.
2. On the 24th falling edge of SCLK, the $D_{IN/OUT}$ is turned off to Hi-Z.

Figure 2. Serial Read Operation

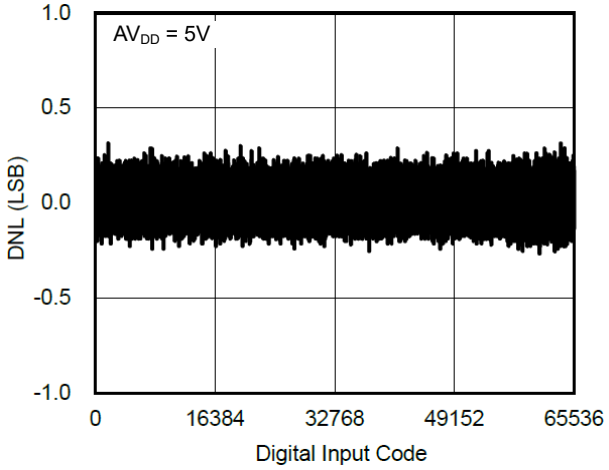
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25℃, unless otherwise noted.

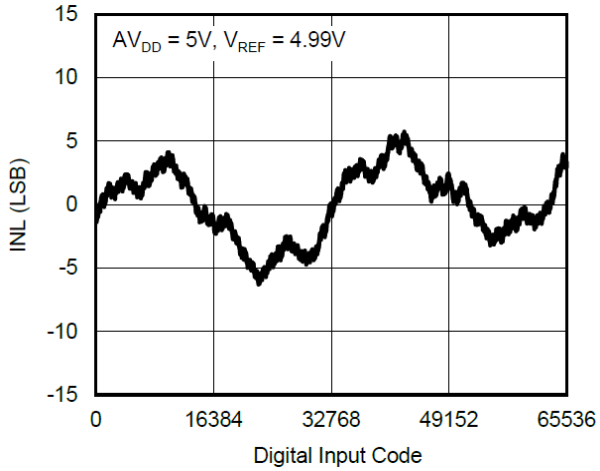
INL vs. Digital Input Code (Channel A)



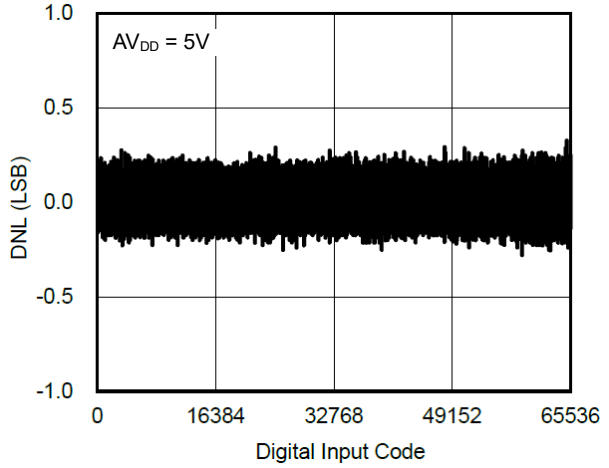
DNL vs. Digital Input Code (Channel A)



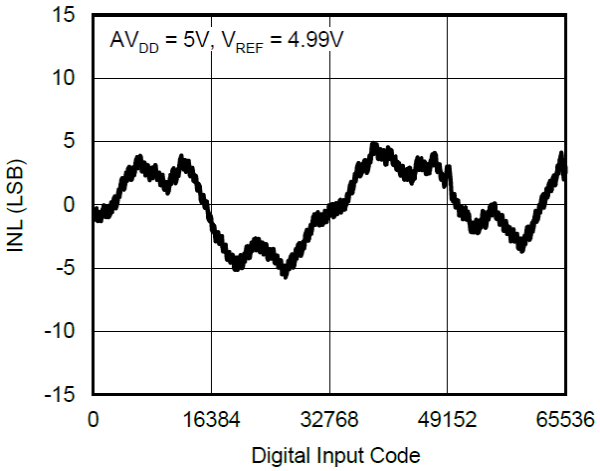
INL vs. Digital Input Code (Channel B)



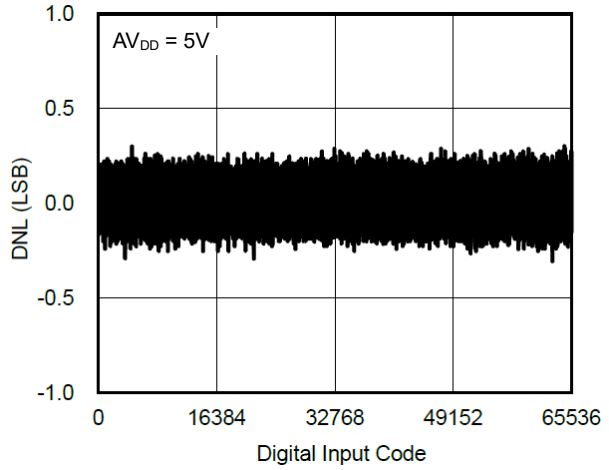
DNL vs. Digital Input Code (Channel B)



INL vs. Digital Input Code (Channel C)



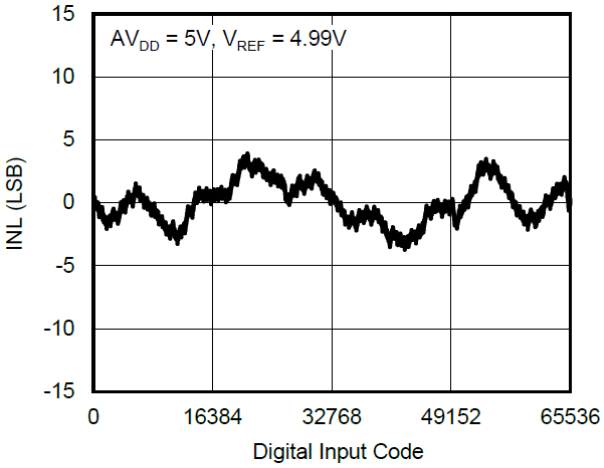
DNL vs. Digital Input Code (Channel C)



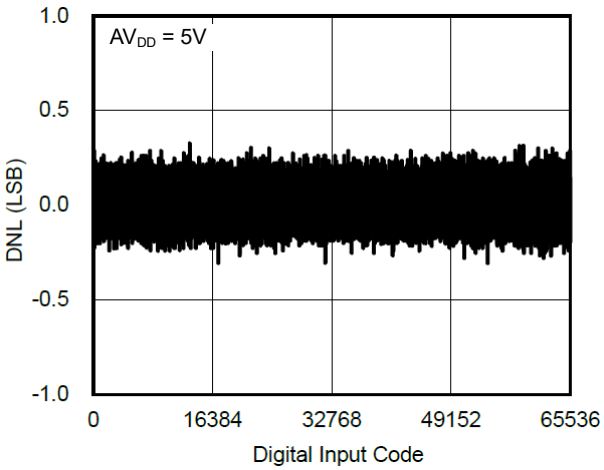
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, unless otherwise noted.

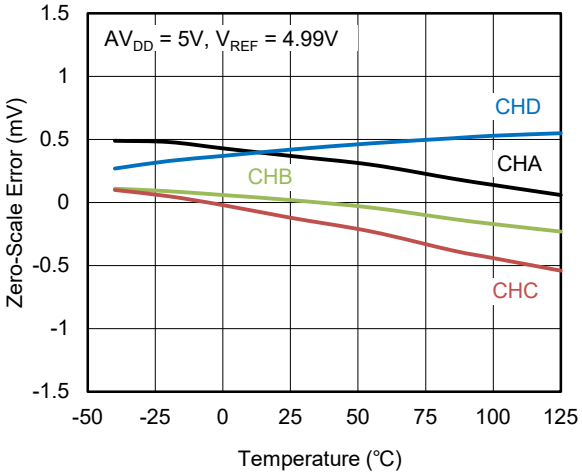
INL vs. Digital Input Code (Channel D)



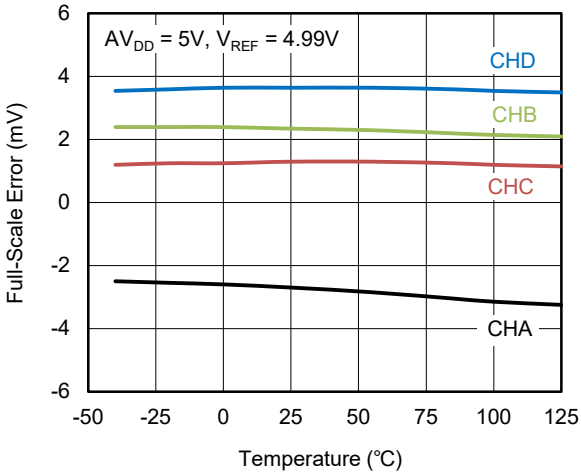
DNL vs. Digital Input Code (Channel D)



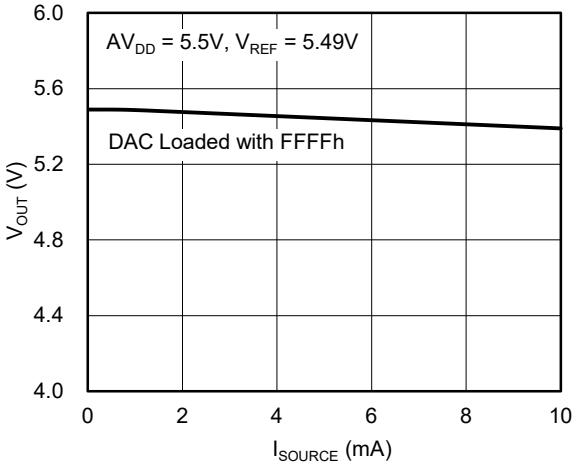
Zero-Scale Error vs. Temperature



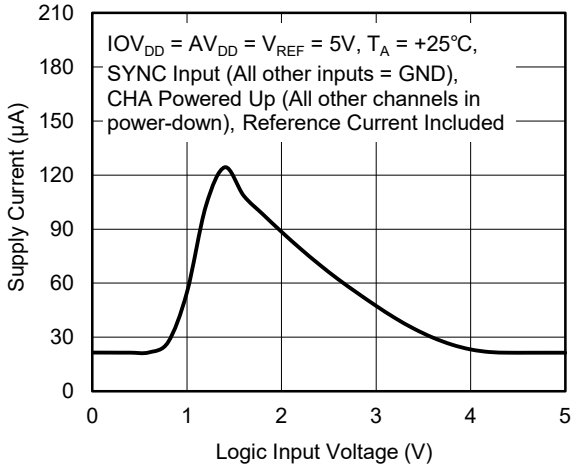
Full-Scale Error vs. Temperature



Source Current Capability (All Channels)



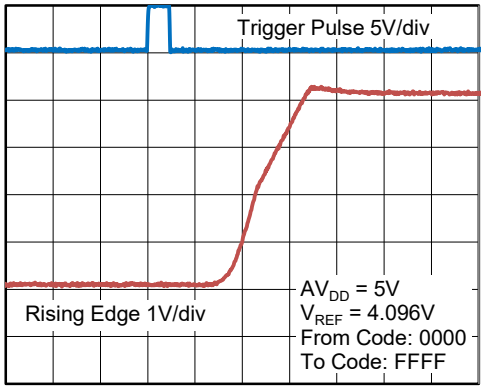
Supply Current vs. Logic Input Voltage



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

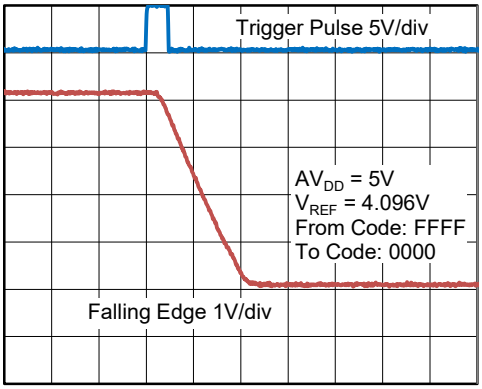
T_A = +25℃, unless otherwise noted.

Full-Scale Settling Time, 5V Rising Edge



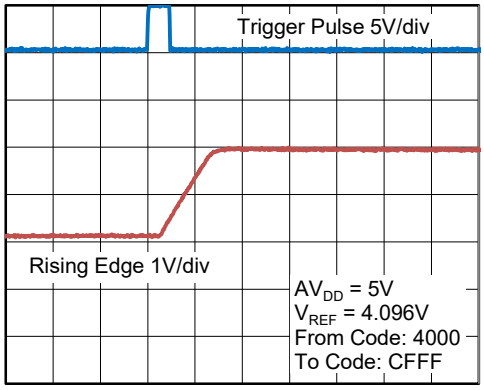
Time (2μs/div)

Full-Scale Settling Time, 5V Falling Edge



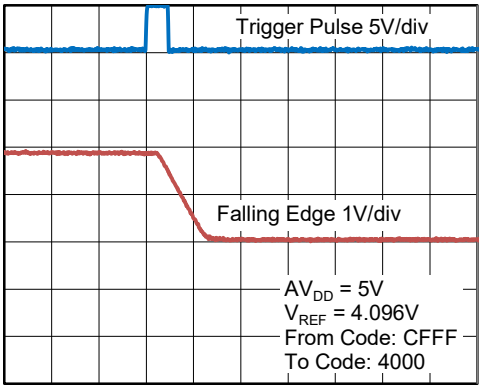
Time (2μs/div)

Half-Scale Settling Time, 5V Rising Edge



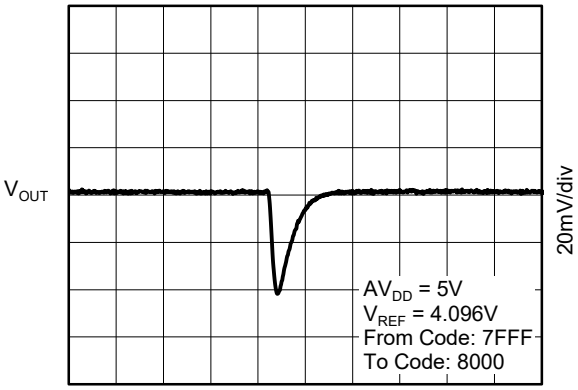
Time (2μs/div)

Half-Scale Settling Time, 5V Falling Edge



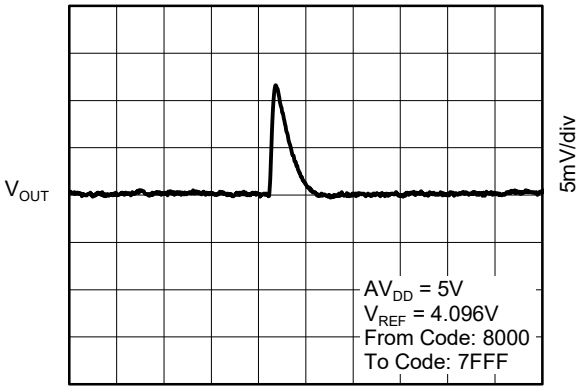
Time (2μs/div)

Glitch Energy: 5V, 1LSB Step, Rising Edge



Time (2μs/div)

Glitch Energy: 5V, 1LSB Step, Falling Edge

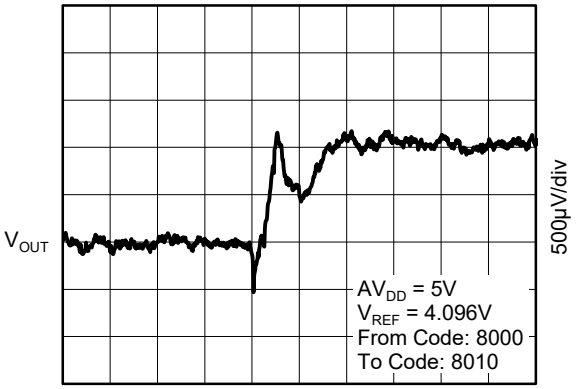


Time (2μs/div)

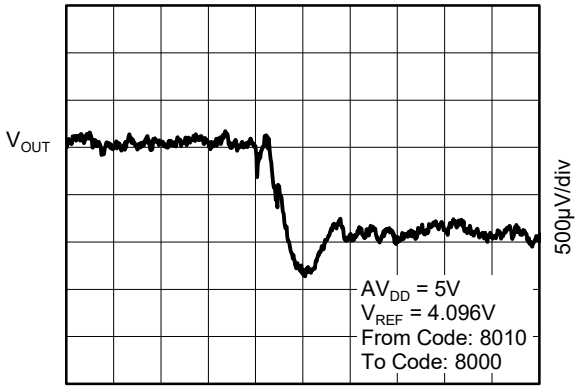
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, unless otherwise noted.

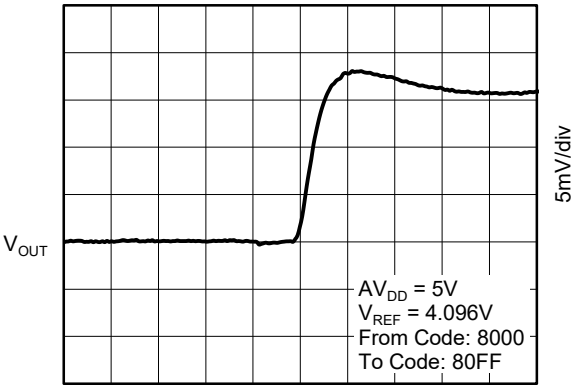
Glitch Energy: 5V, 16LSB Step, Rising Edge



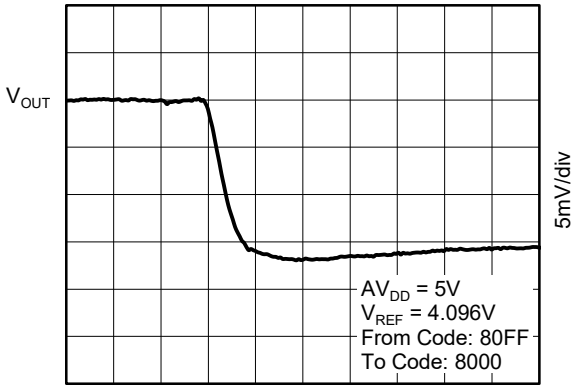
Glitch Energy: 5V, 16LSB Step, Falling Edge



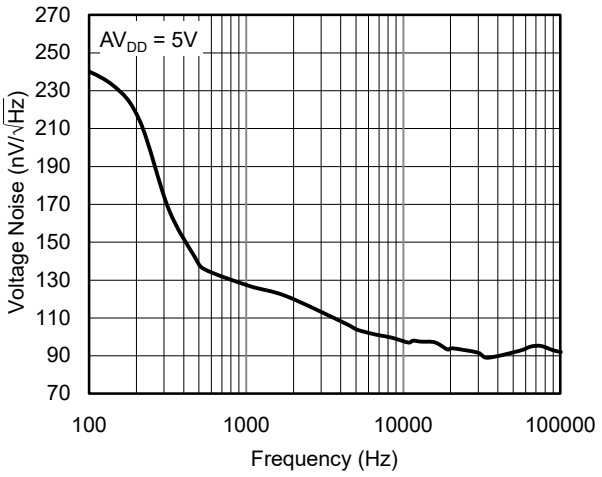
Glitch Energy: 5V, 256LSB Step, Rising Edge



Glitch Energy: 5V, 256LSB Step, Falling Edge



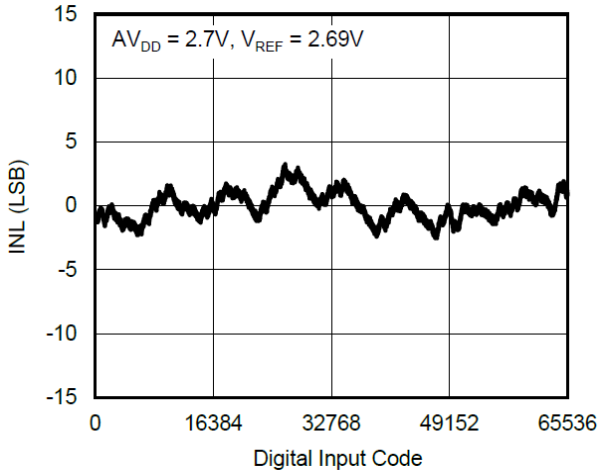
Output Noise Density



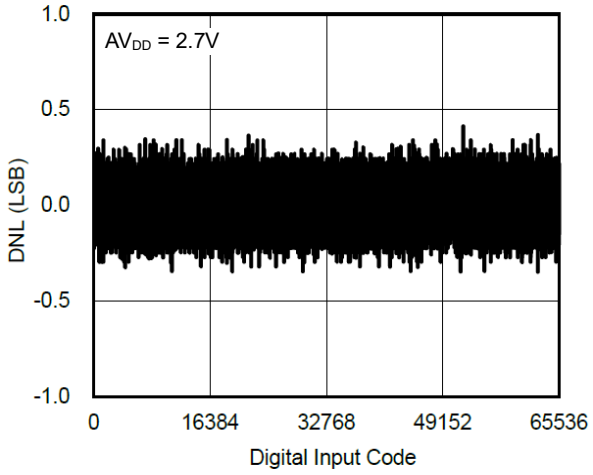
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, unless otherwise noted.

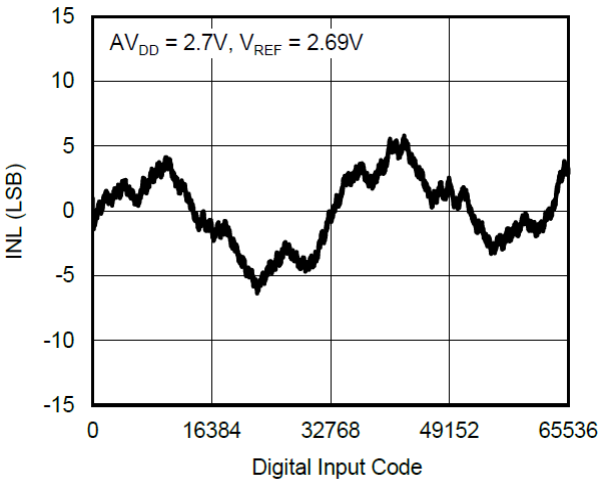
INL vs. Digital Input Code (Channel A)



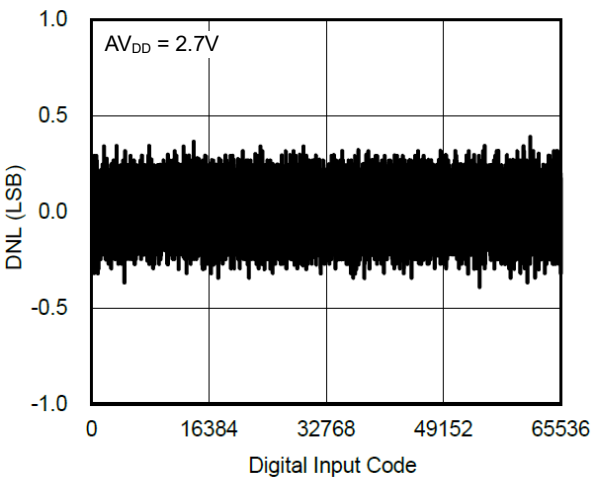
DNL vs. Digital Input Code (Channel A)



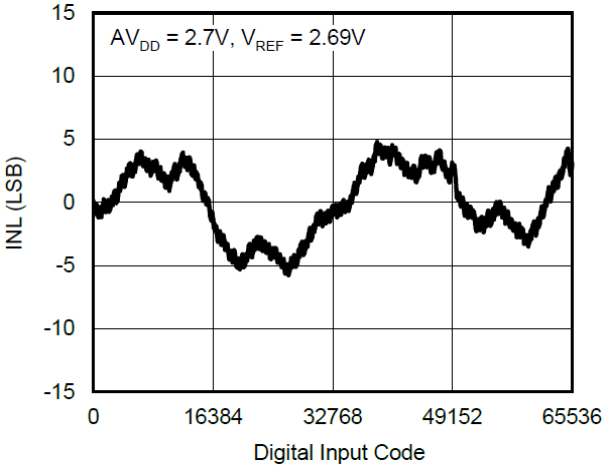
INL vs. Digital Input Code (Channel B)



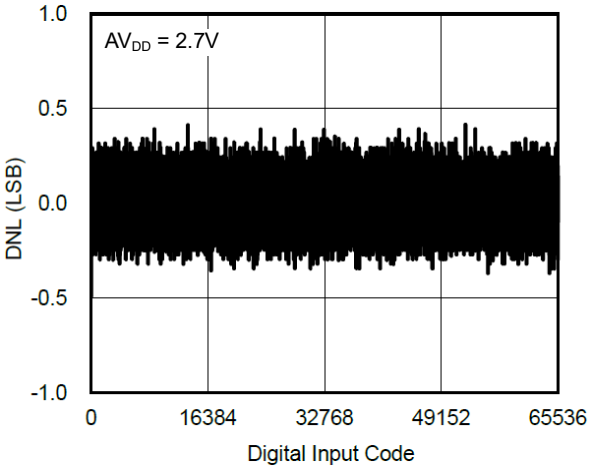
DNL vs. Digital Input Code (Channel B)



INL vs. Digital Input Code (Channel C)



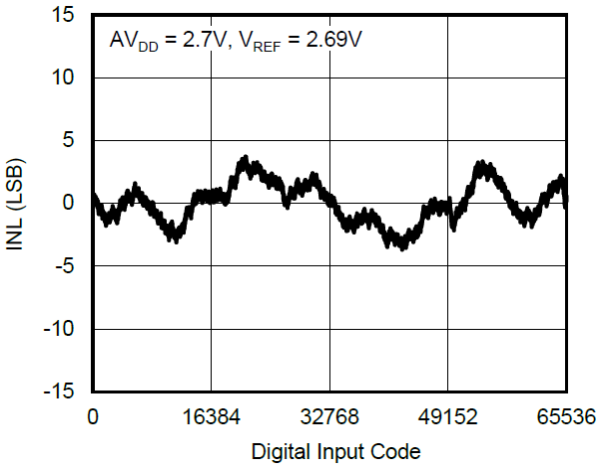
DNL vs. Digital Input Code (Channel C)



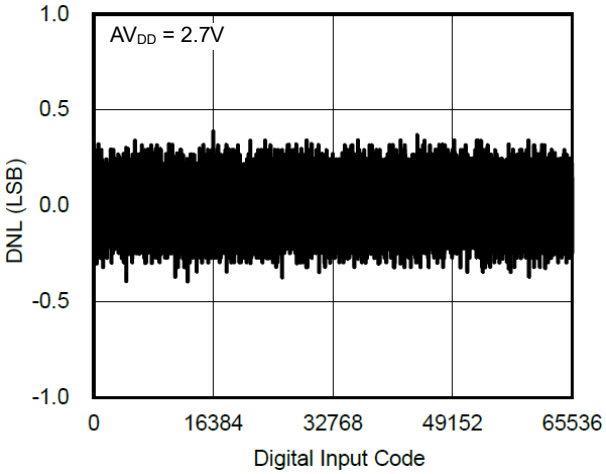
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, unless otherwise noted.

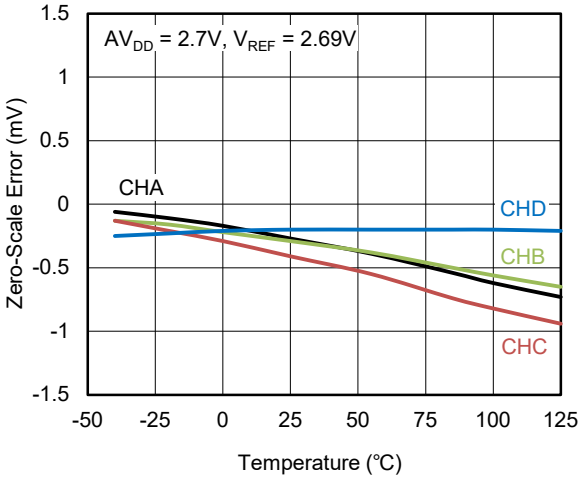
INL vs. Digital Input Code (Channel D)



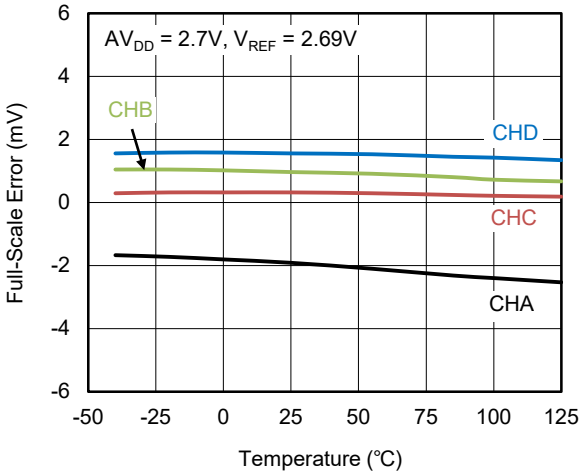
DNL vs. Digital Input Code (Channel D)



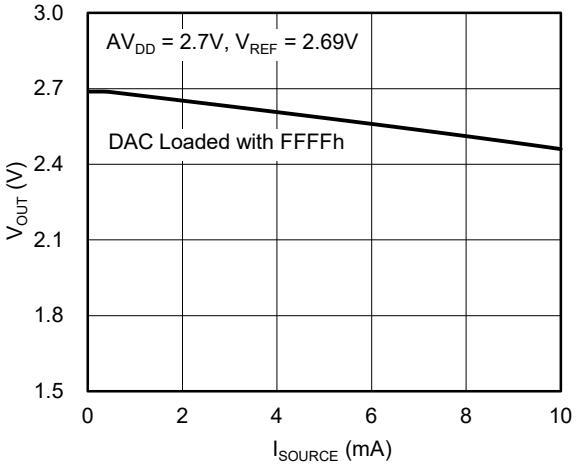
Zero-Scale Error vs. Temperature



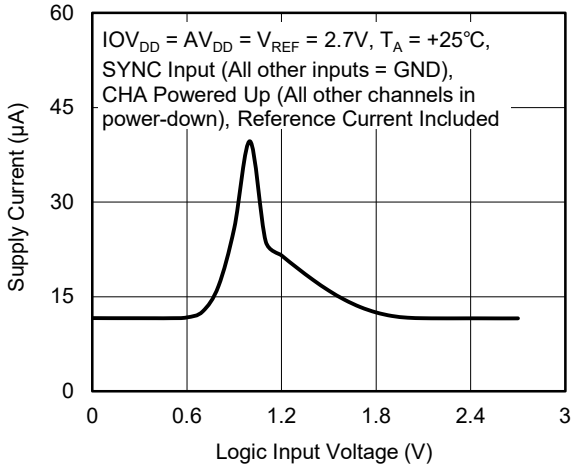
Full-Scale Error vs. Temperature



Source Current Capability (All Channels)



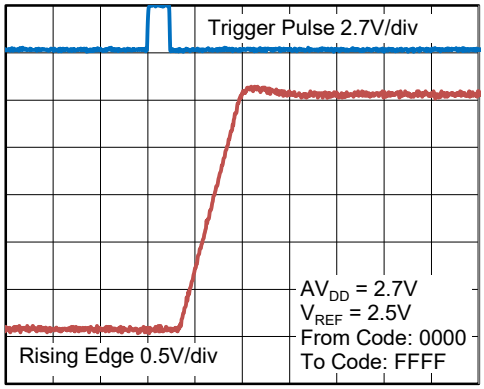
Supply Current vs. Logic Input Voltage



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

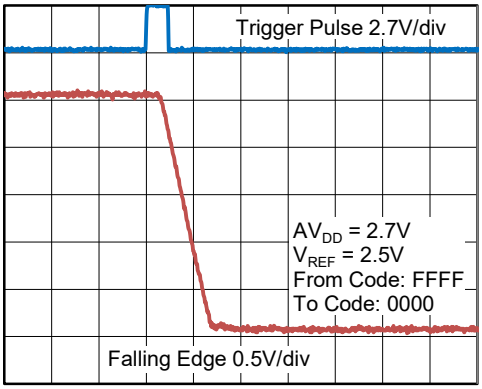
T_A = +25℃, unless otherwise noted.

Full-Scale Settling Time: 2.7V Rising Edge



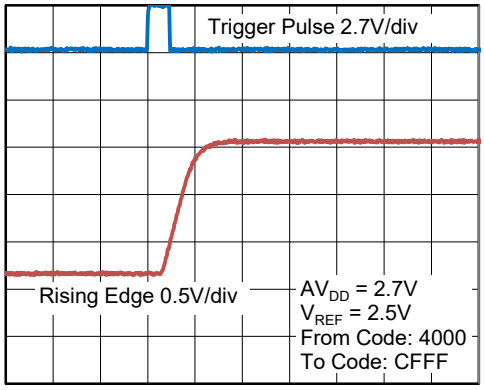
Time (2μs/div)

Full-Scale Settling Time: 2.7V Falling Edge



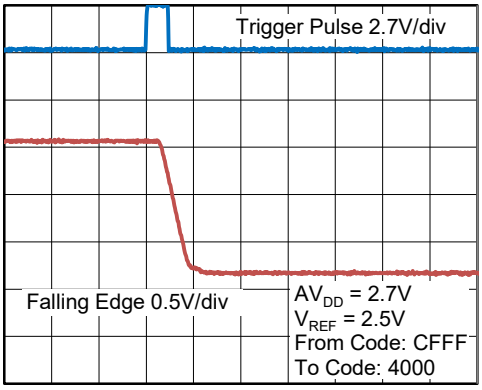
Time (2μs/div)

Half-Scale Settling Time: 2.7V Rising Edge



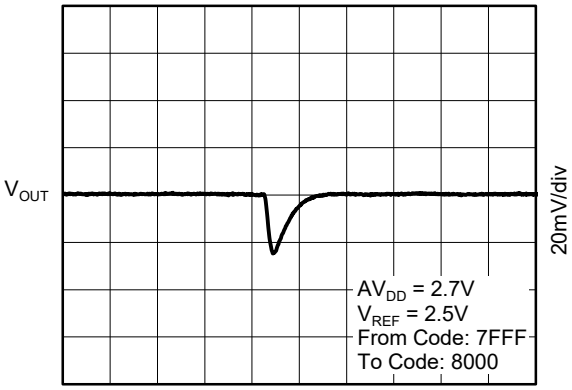
Time (2μs/div)

Half-Scale Settling Time: 2.7V Falling Edge



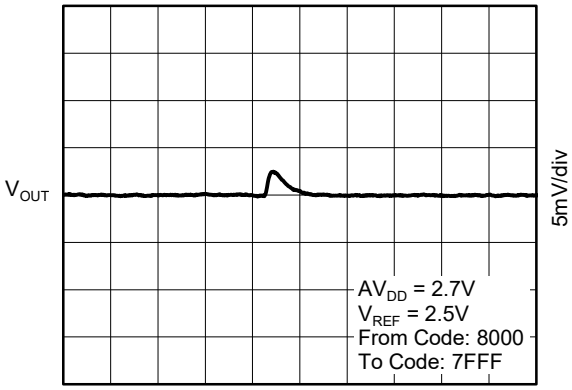
Time (2μs/div)

Glitch Energy: 2.7V, 1LSB Step, Rising Edge



Time (2μs/div)

Glitch Energy: 2.7V, 1LSB Step, Falling Edge

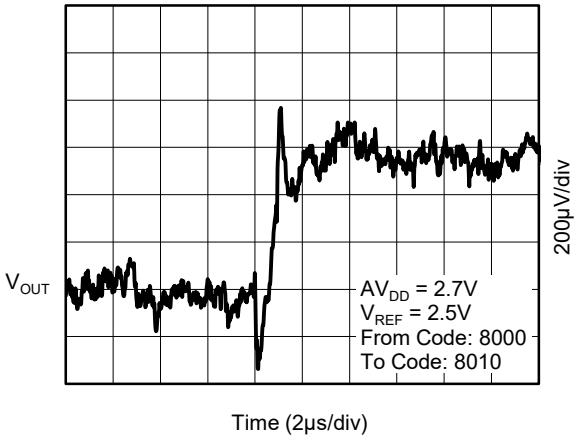


Time (2μs/div)

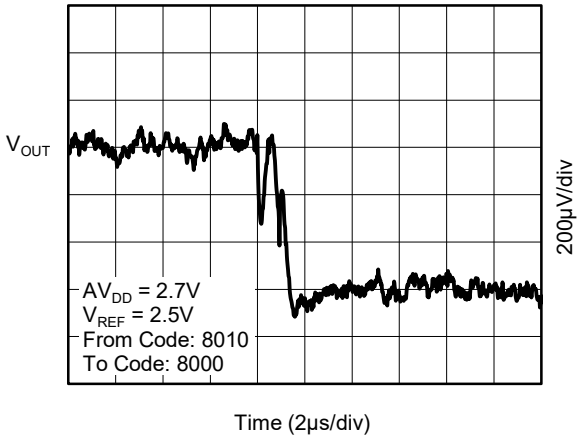
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, unless otherwise noted.

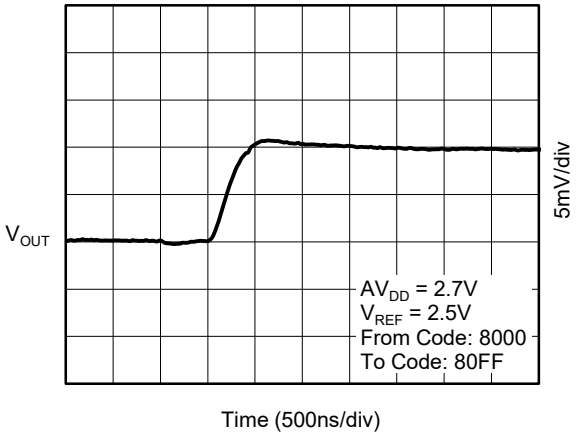
Glitch Energy: 2.7V, 16LSB Step, Rising Edge



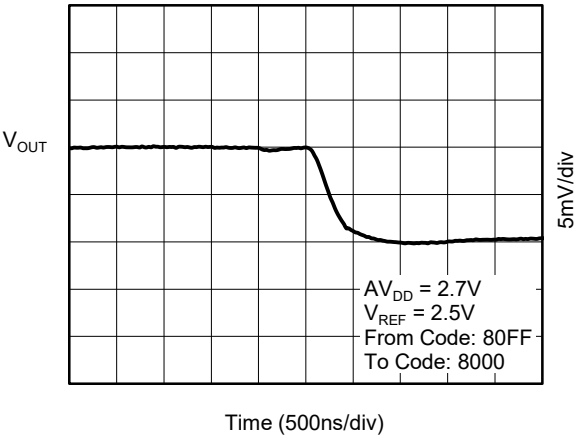
Glitch Energy: 2.7V, 16LSB Step, Falling Edge



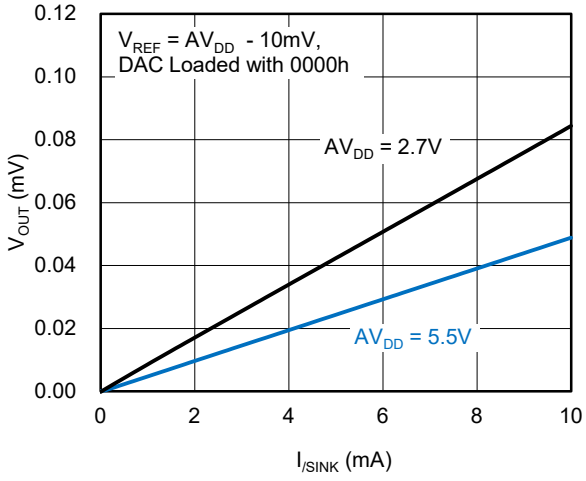
Glitch Energy: 2.7V, 256LSB Step, Rising Edge



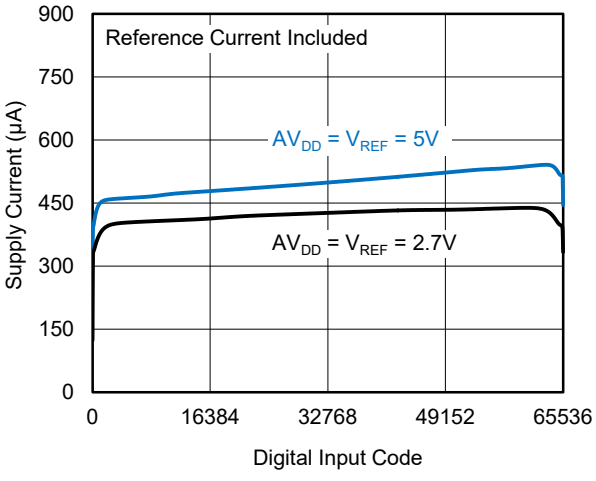
Glitch Energy: 2.7V, 256LSB Step, Falling Edge



Sink Current Capability (All Channels)



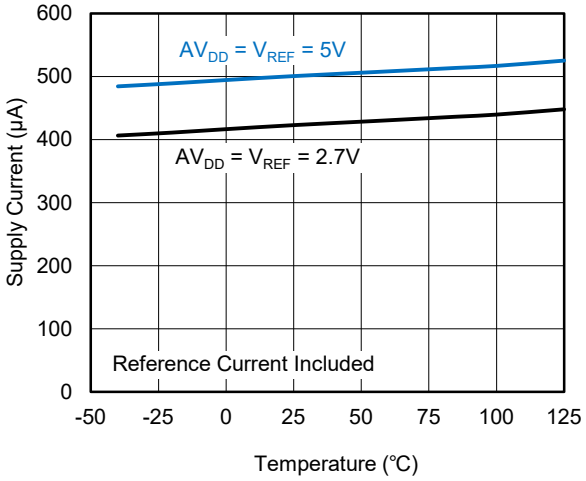
Supply Current vs. Digital Input Code



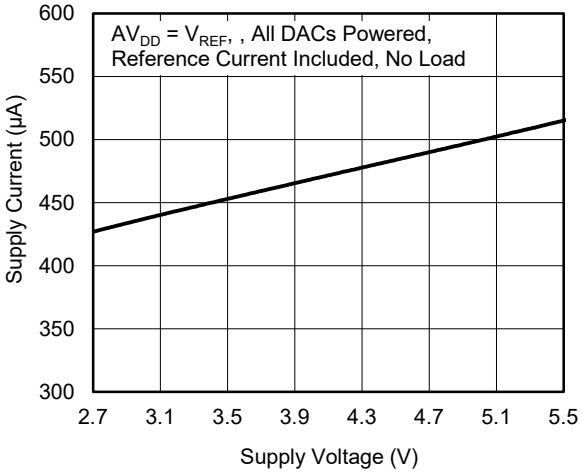
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, unless otherwise noted.

Supply Current vs. Temperature



Supply Current vs. Supply Voltage



FUNCTIONAL BLOCK DIAGRAM

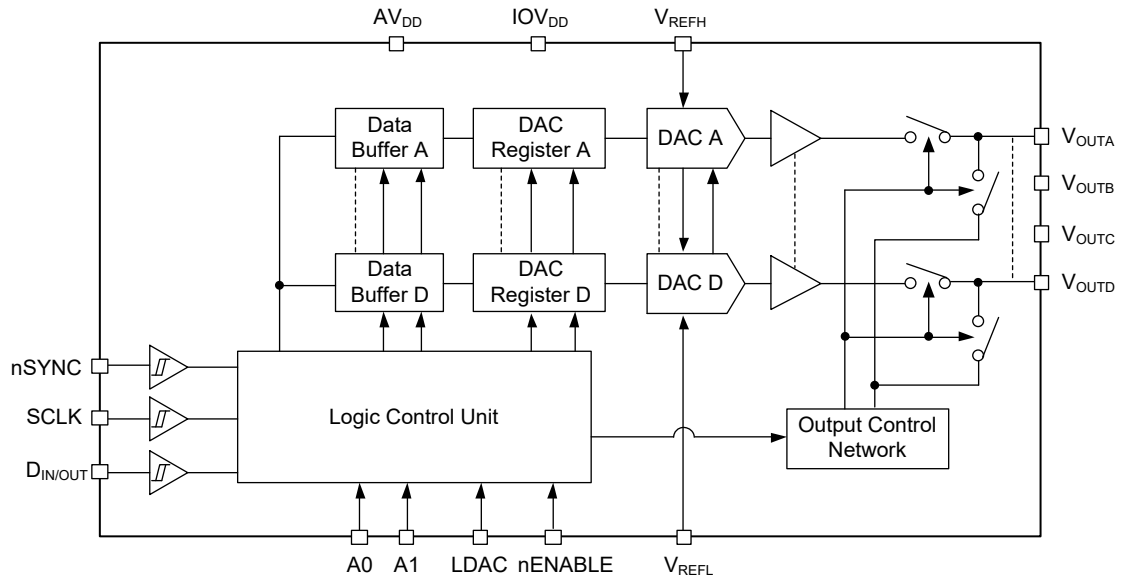


Figure 3. Block Diagram

DETAILED DESCRIPTION

DAC Section

The SGM5352-16 is a 16-bit resistor string DAC, and it has output buffer amplifier. The input code is unipolar straight binary, so the ideal output voltage can be calculated based on the following equation:

$$V_{OUTX} = (V_{REFH} - V_{REFL}) \times \frac{D_{IN}}{65536} \quad (1)$$

Where:

D_{IN} = Decimal equivalent of the binary code, which is loaded to the DAC register. The range is 0 to 65535.

Serial Interface

The 3-wire serial interface (nSYNC, SCLK, and $D_{IN/OUT}$) is compatible with SPI interface standard. The SGM5352-16 supports 3-wire SPI read and write operation. See Figure 1 for an example of a write sequence, and see Figure 2 for an example of a read sequence.

Input Shift Register

Data input register is shown in Figure 4. DB[23:22] are chip address bits, and they must be matched by the setting of hardware address pins A1 and A0. If there is no match, the operation command is ignored. Address matching can be overridden by the broadcast update. DB[19] is write/read selection bit. When DB[19] = 0, it means this is a write operation. When DB[19] = 1, it means this is a read operation. DB[18:17] are DAC channel select bits. See more details in Table 2 and Table 3.

Table 1. Power-Down Modes

PD2 (DB[16])	PD1 (DB[15])	PD0 (DB[14])	Operating Mode
1	0	0	Output high-impedance
1	0	1	Output typically 1kΩ to GND
1	1	0	Output typically 100kΩ to GND
1	1	1	Output high-impedance

DB[23]	DB[22]	DB[21]	DB[20]	DB[19]	DB[18]	DB[17]	DB[16]	DB[15]	DB[14]	DB[13]	DB[12]	DB[11]	DB[10]	DB[9]	DB[8]	DB[7]	DB[6]	DB[5]	DB[4]	DB[3]	DB[2]	DB[1]	DB[0]
Address				R/$\overline{W}$	Channel Selection		Power-Down	MSB															LSB
A1	A0	LD1	LD0	RW	DAC_S[1:0]		PD2	D15/ PD1	D14/ PD0	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Figure 4. Data Input Register Format

Table 2. Input Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT
DB[23]	A1	Address Bit 1	A1 must be matched with the hardware address pin 14.
DB[22]	A0	Address Bit 0	A0 must be matched with the hardware address pin 13.
DB[21:20]	LD[1:0]	Output Load Selection Configuration Bits 00 = Write to DAC buffer and don't load DAC output 01 = Write to DAC buffer and load selected channel DAC output 10 = Write to DAC buffer and load all channels DACs outputs simultaneously 11 = Broadcast modes, see Table 3	
DB[19]	RW	Read or Write Operation Selection Bit 0 = It's a write operation to chip 1 = It's a read operation to chip	When DB[21:20] = "00" and "01", chip corresponds to DB[19] setting to do write or read operation. When DB[21:20] = "10" and "11", the operation is only write command ignoring the DB[19].
DB[18:17]	DAC_S[1:0]	DAC Channel Selection Bits 00 = DAC channel A 01 = DAC channel B 10 = DAC channel C 11 = DAC channel D	When there is a broadcast command (DB[21:20] = "11"), these bits are not for DAC channel selection. Details see Table 3.
DB[16]	PD2	Power-Down Control Bit 0 = Not power-down 1 = Power-down	When there is a broadcast command (DB[21:20] = "11"), this bit is not dedicated for power-down. Details see Table 3.
DB[15:0]	Data[15:0]		DB[15] is Most Significant Bit (MSB). DB[0] is Least Significant Bit (LSB). When DB[16] = 1, DB[15:14] meanings see Table 1.

DETAILED DESCRIPTION (continued)

Table 3. Broadcast Modes Description

DB[23]	DB[22]	DB[21]	DB[20]	DB[19]	DB[18]	DB[17]	DB[16]	DB[15:0]			Description
X	X	1	1	X	0	X	0	X			Simultaneously update all channels of all devices in the system with data stored in each channels temporary register.
X	X	1	1	X	1	X	0	Data			Write to all devices and load all DACs with shifted in data.
X	X	1	1	X	1	X	1	DB[15:14]		0	Write to all devices and load all DACs with power-down command in DB[16:14]. See details in Table 1.
X	X	1	1	X	0	X	1	1	X	X	Enable SPI output function.
X	X	1	1	X	0	X	1	0	X	X	Disable SPI output function.

nSYNC Interrupt

In a normal write/read sequence, the nSYNC line must be kept low for at least 24 falling edges of SCLK and the DAC is updated on the 24th falling edge. However, if nSYNC goes high before the 24th falling edge, this write/read operation is invalid and ignored. An example is shown in Figure 5.

Power-On Reset

The SGM5352-16 has a power-on reset circuit, which can control the output voltage during power-up. On power-up, the DAC output voltages are 0V.

Power-Down Modes

The SGM5352-16 provides flexible power-down modes. It can be a broadcast power-down command to all the DAC channels, or it can power down a selected channel and still update data on other channels. When a channel data is updated, it exits power-down automatically. Please see Table 2 and Table 3 for power-down operation details.

LDAC Functionality

The SGM5352-16 provides two update functions: software update mode and hardware update mode.

In software update mode, the LDAC pin must be connected to GND. The SGM5352-16 data updates are synchronized with the falling edge of the 24th SCLK cycle (there is a corresponded LD[1:0] setting), which follows a falling edge of nSYNC.

In hardware update mode, the LDAC pin is used as a positive edge triggered signal for DAC updates. With a low-to-high LDAC transition, all DACs are updated with corresponding DAC register data.

nENABLE Pin

In normal operation, the enable pin must be set low. When the enable pin goes high, the SGM5352-16 is not response to any operation.

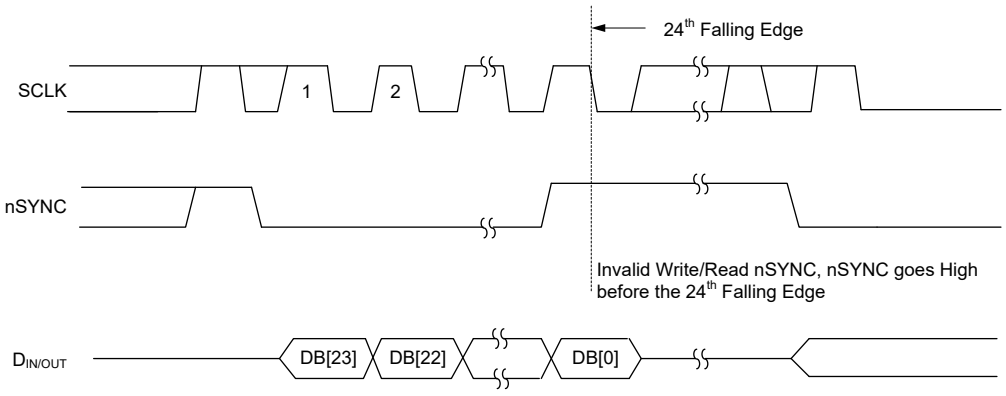


Figure 5. An Example of Invalid Write/Read nSYNC Timing

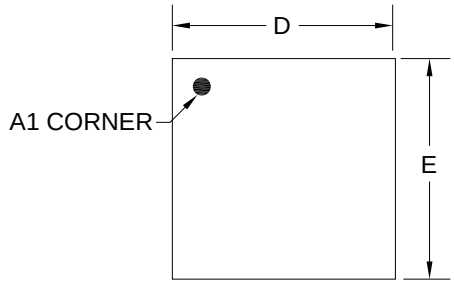
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

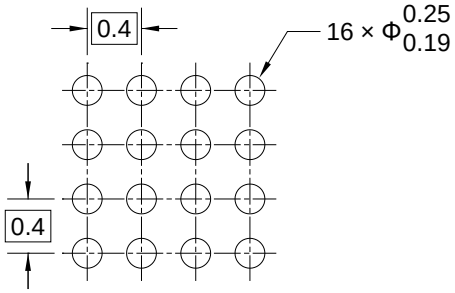
Changes from Original (DECEMBER 2021) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

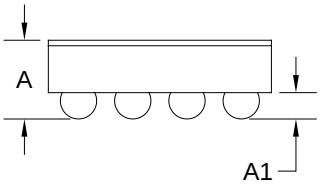
WLCSP-1.64×1.62-16B



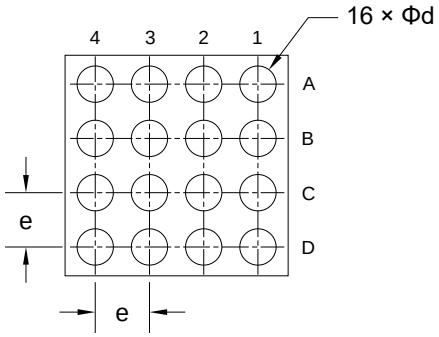
TOP VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



SIDE VIEW



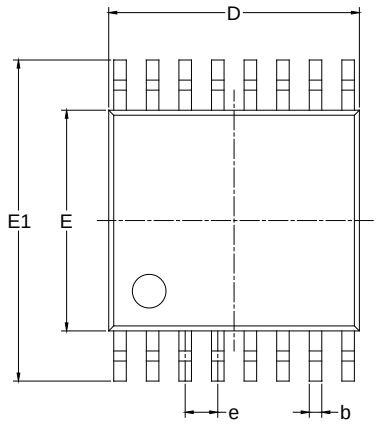
BOTTOM VIEW

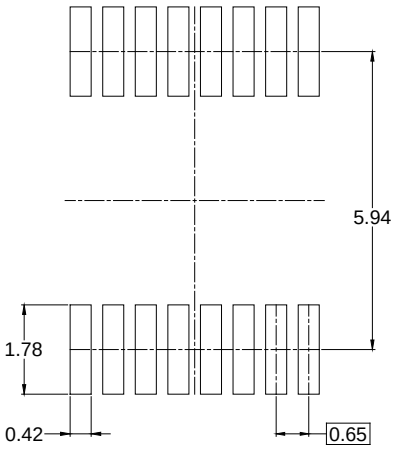
Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	0.542	0.580	0.618
A1	0.174	0.194	0.214
D	1.620	1.645	1.670
E	1.600	1.625	1.650
d	0.248	0.268	0.288
e	0.400 BSC		

NOTE: This drawing is subject to change without notice.

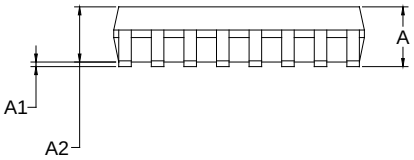
PACKAGE OUTLINE DIMENSIONS

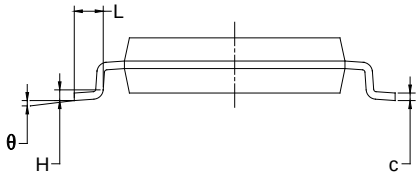
TSSOP-16





RECOMMENDED LAND PATTERN (Unit: mm)



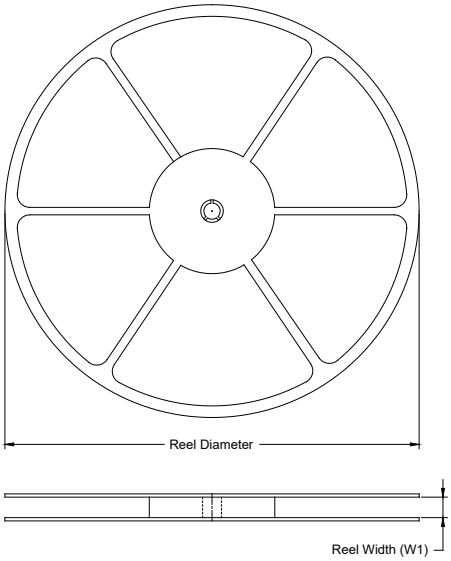


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A		1.200		0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	4.860	5.100	0.191	0.201
E	4.300	4.500	0.169	0.177
E1	6.200	6.600	0.244	0.260
e	0.650 BSC		0.026 BSC	
L	0.500	0.700	0.02	0.028
H	0.25 TYP		0.01 TYP	
θ	1°	7°	1°	7°

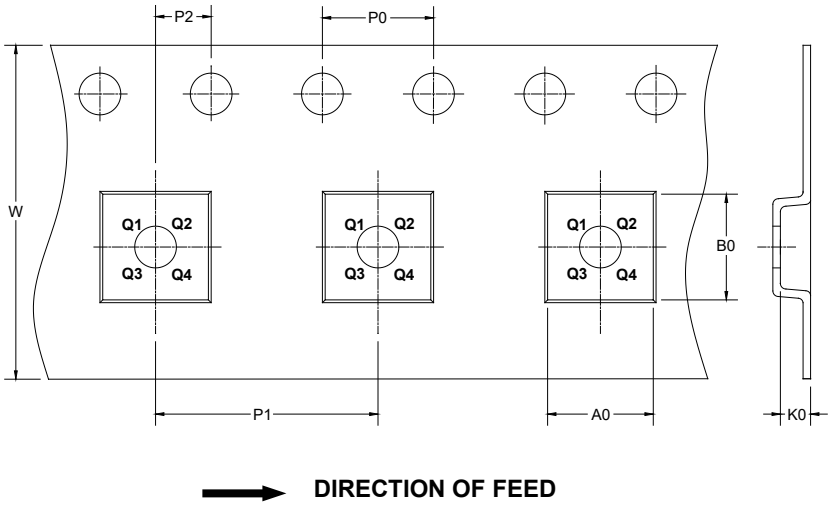
NOTES:
1. Body dimensions do not include mode flash or protrusion.
2. This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



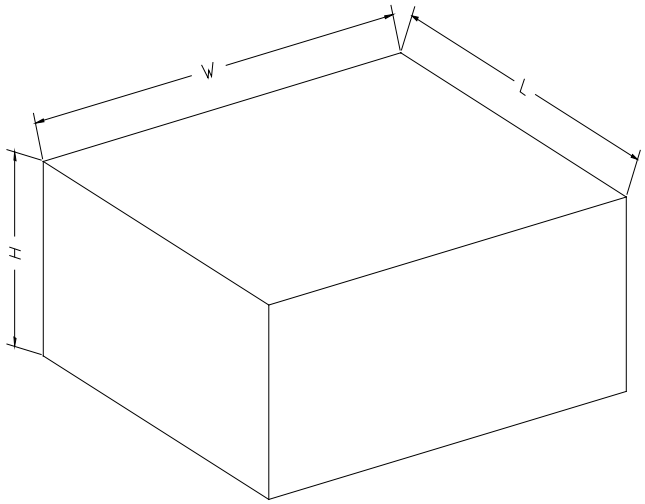
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
WLCSP-1.64×1.62-16B	7″	9.5	1.81	1.81	0.76	4.0	4.0	2.0	8.0	Q1
TSSOP-16	13″	12.4	6.90	5.60	1.20	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18
13″	386	280	370	5

DD0002