SGM8139
Low Power, Low Voltage PIR and Vibration Sensor AFE

GENERAL DESCRIPTION

The SGM8139 is a low voltage low power analog front end designed for PIR and vibration sensors. This part integrates two high input impedance operational amplifiers, window comparator, state control logic, a delay timer, a latch timer, a voltage reference and high current output stages. It can be used in various sensors, delay controllers as well as wake-up circuit in low power consumption systems.

Many industrial and building automation systems use motion detectors to control different functions based on human presence. Using SGM8139 with proper PIR sensor, it is easy to build a compact passive infrared detection system. The output stage of SGM8139 can easily drive different types of lights, buzzers, automatic doors, fans and white goods with programmable timers.

It is especially suitable for office buildings, hotels, shopping malls or automatic lighting and alarm systems, as well as intrusion detection. SGM8139 can be used for motion detection and room monitors in a smart home system as an ultra-low power wake-up block. SGM8139 can be used to condition the vibration sensor, providing a trigger signal to system.

SGM8139 is specifically designed to operate over a wide range of supply voltage from 1.4V to 5.5V. SGM8139 draws only 6μA supply current. It is ideal for applications powered by single cell or dual cell alkaline battery.

With two operational amplifiers, window comparators, and delay/lockout timers adjustable through external RCs, SGM8139 can both process the PIR output signal effectively and provide good anti-interference performance.

The SGM8139 is specified for the -40℃ to +85℃ industrial temperature range. The SGM8139 is available in Green SOIC-16 and TQFN-2.5×2.5-16L packages. The TQFN package makes it ideal for portable electronic products with area constrained PC boards.

FEATURES

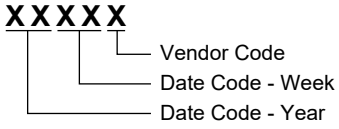
- **Operating Voltage Range: 1.4V to 5.5V**
- **Average Quiescent Current: 6.5μA (TYP)**
- **Two Integrated High Input Impedance Operational Amplifiers**
- **Integrated Bi-directional Amplitude Discriminator**
- **Adjustable Delay/Lockout Timers With External R and C**
- **Integrated Voltage Reference**
- **Available in Green SOIC-16 and TQFN-2.5×2.5-16L Packages**

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM8139	SOIC-16	-40℃ to +85℃	SGM8139YS16G/TR	SGM8139YS16 XXXXX	Tape and Reel, 2500
	TQFN-2.5×2.5-16L	-40℃ to +85℃	SGM8139YTQB16G/TR	8139 XXXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range (V_{SS} = 0V) ..... 1.4V to 6V
Signal Input Terminals, Voltage (V_{DD} = 6V, V_{SS} = 0V) ..... -0.3V to 5.5V
Signal Input Terminals, Current (V_{DD} = 5V, V_{SS} = 0V) ..... ±10mA
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 4000V
MM 400V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Operating Temperature Range ..... -40℃ to +85℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

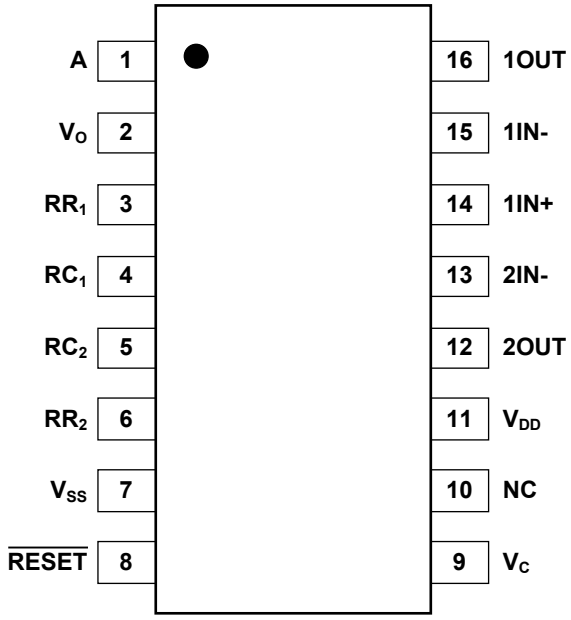
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

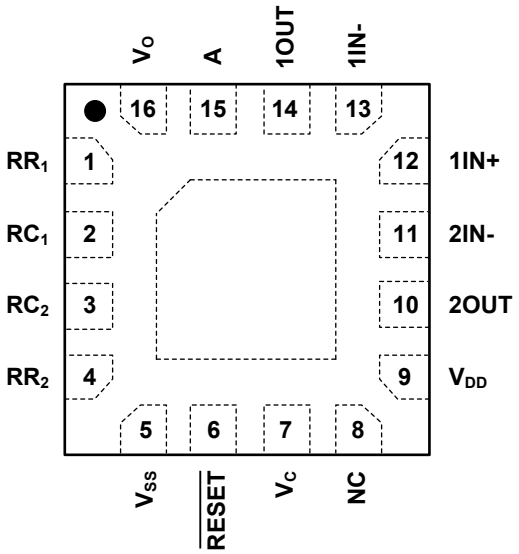
PIN CONFIGURATIONS

SGM8139 (TOP VIEW)



SOIC-16

SGM8139 (TOP VIEW)



TQFN-2.5×2.5-16L

PIN DESCRIPTION

PIN		NAME	FUNCTION
SOIC-16	TQFN-2.5×2.5-16L		
1	15	A	Repeatable Trigger Mode and Non-Repeatable Trigger Mode. When A = "1", repeatable trigger mode is active; when A = "0", non-repeatable trigger mode is active.
2	16	V_O	Output Terminal. Triggered by V_S rising edge, and kept low in t_X and t_i period.
3	1	RR_1	Set up the output delay time tx. $t_x \approx 28672R_1C_1$. The recommended resistor value is more than 3kΩ for RR_1.
4	2	RC_1	Set up the output delay time tx. $t_x \approx 28672R_1C_1$.
5	3	RC_2	Set up the trigger latch time ti. $t_i \approx 28R_2C_2$.
6	4	RR_2	Set up the trigger latch time ti. $t_i \approx 28R_2C_2$. The recommended resistor value is more than 3kΩ for RR_2.
7	5	V_{SS}	Negative Power Supply. It is normally connected to ground.
8	6	$\overline{RESET}$	Chip Reset Input. It is normally connected to V_{DD}. Active low.
9	7	V_C	Trigger Inactive Terminal. When $V_C < V_R$, Trigger inactive; when $V_C > V_R$, Trigger active. $V_R \approx 0.2V_{DD}$.
10	8	NC	No Connection.
11	9	V_{DD}	Positive Power Supply.
12	10	2OUT	The Output of OP2.
13	11	2IN-	The Inverting Input of OP2.
14	12	1IN+	The Non-inverting Input of OP1.
15	13	1IN-	The Inverting Input of OP1.
16	14	1OUT	The Output of OP1.
—	Exposed Pad	—	It should be connected to V_{SS} or left floating.

ELECTRICAL CHARACTERISTICS

(V_{SS} = 0V, V_{DD} = 5V, T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{DD}		1.4		5.5	V
Output Current	I_{OUT}	V_{DD} = 5V		50		mA
V_C (High Level)	V_{RH}	V_{DD} = 3.3V	0.76			V
V_C (Low Level)	V_{RL}	V_{DD} = 3.3V			0.56	V
A (High Level)	V_{AH}	V_{DD} = 3.3V	2.57			V
A (Low Level)	V_{AL}	V_{DD} = 3.3V			0.99	V
V_O (High Level)	V_{OH}	V_{DD} = 5V, I_O = 50mA		0.9	1.2	V
V_O (Low Level)	V_{OL}	V_{DD} = 5V, I_O = 50mA		0.38	0.46	V
Window Comparator Threshold V_H	V_H			0.7V_{DD}		
Window Comparator Threshold V_L	V_L			0.25V_{DD}		
OPA Bias Reference V_M	V_M			0.5V_{DD}		
V_C Input Reference V_R	V_R			0.2V_{DD}		

Operational Amplifiers

(V_{DD} = 1.4V, V_{SS} = 0V, T_A = +25℃, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, R_L = 1MΩ connected to V_{DD}/2, unless otherwise noted.)

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC Performance							
Input Offset Voltage		V_{OS}	V_{CM} = V_{DD}/2		0.3	1.7	mV
			-40℃ ≤ T_A ≤ +85℃			2.2	
Input Common Mode Voltage Range		V_{CMR}		V_{SS} - 0.1		V_{DD} + 0.1	V
Large-Signal Voltage Gain		A_{VO}	V_{CM} = V_{DD}/2, R_L = 10kΩ	72	77		dB
			-40℃ ≤ T_A ≤ +85℃	63			
Output Voltage Swing From Rail		V_{OH}	V_{CM} = V_{DD}/2, R_L = 10kΩ to V_{DD}/2		5	12	mV
			-40℃ ≤ T_A ≤ +85℃			14	
		V_{OL}	V_{CM} = V_{DD}/2, R_L = 10kΩ to V_{DD}/2		5	12	mV
			-40℃ ≤ T_A ≤ +85℃			14	
Power Supply Rejection Ratio		PSRR	V_{DD} = 1.4V to 5.5V	75	84		dB
			-40℃ ≤ T_A ≤ +85℃	69			
Operating Voltage Range				1.4		5.5	V
Quiescent Current		I_Q	V_{CM} = V_{DD}/2, I_O = 0		4.8	8.8	μA
			-40℃ ≤ T_A ≤ +85℃			11.0	
AC Performance							
Slew Rate	UP	SR	f = 100Hz, V_{OUT} = 1V_{PP} Step, A_V = 1		5		V/ms
	DOWN				2.8		
Gain-Bandwidth Product		GBP	R_F = 100kΩ, R_G = 10kΩ, R_L = 1MΩ, A_V = 10		8		kHz
Phase Margin			R_F = 100kΩ, R_G = 10kΩ, R_L = 1MΩ, A_V = 10		70		°
Input Voltage Noise			f = 0.1Hz to 10Hz		4.8		μV_{PP}
Input Voltage Noise Density		e_n	f = 1kHz, V_{CM} = V_{DD}/2		240		nV/$\sqrt{HZ}$

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3.3V, V_{SS} = 0V, T_A = +25℃, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, R_L = 1MΩ connected to V_{DD}/2, unless otherwise noted.)

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC Performance							
Input Offset Voltage		V_{OS}	V_{CM} = V_{DD}/2		0.3	1.6	mV
			-40℃ ≤ T_A ≤ +85℃			1.7	
Input Common Mode Voltage Range		V_{CMR}		V_{SS} - 0.1		V_{DD} + 0.1	V
Common Mode Rejection Ratio		CMRR	V_{CM} = -0.1V to V_{DD} - 1.5V	62	76		dB
			-40℃ ≤ T_A ≤ +85℃	61			
Large-Signal Voltage Gain		A_{VO}	V_{CM} = V_{DD}/2, R_L = 10kΩ	84	89		dB
			-40℃ ≤ T_A ≤ +85℃	77			
Output Voltage Swing From Rail		V_{OH}	V_{CM} = V_{DD}/2, R_L = 10kΩ to V_{DD}/2		4	12	mV
			-40℃ ≤ T_A ≤ +85℃			14	
		V_{OL}	V_{CM} = V_{DD}/2, R_L = 10kΩ to V_{DD}/2		4	12	mV
			-40℃ ≤ T_A ≤ +85℃			14	
Output Short Circuit Current		I_{SOURCE}	V_{CM} = V_{DD}/2, R_L = 10Ω to V_{DD}/2	9	11		mA
		I_{SINK}	V_{CM} = V_{DD}/2, R_L = 10Ω to V_{DD}/2	9	11		mA
Power Supply Rejection Ratio		PSRR	V_{DD} = 1.4V to 5.5V	75	84		dB
			-40℃ ≤ T_A ≤ +85℃	69			
Operating Voltage Range				1.4		5.5	V
Quiescent Current		I_Q	V_{CM} = V_{DD}/2, I_O = 0		5.8	10.5	μA
			-40℃ ≤ T_A ≤ +85℃			12.5	
AC Performance (V_{DD} = 3V)							
Slew Rate	UP	SR	f = 100Hz, V_{OUT} = 1V_{PP} Step, A_V = 1		5		V/ms
	DOWN				3		
Gain-Bandwidth Product		GBP	R_F = 100kΩ, R_G = 10kΩ, R_L = 1MΩ, A_V = 10		11		kHz
Phase Margin			R_F = 100kΩ, R_G = 10kΩ, R_L = 1MΩ, A_V = 10		70		°
Input Voltage Noise			f = 0.1Hz to 10Hz		4.8		μV_{PP}
Input Voltage Noise Density		e_n	f = 1kHz, V_{CM} = V_{DD}/2		260		nV/$\sqrt{HZ}$

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 5V, V_{SS} = 0V, T_A = +25℃, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, R_L = 1MΩ connected to V_{DD}/2, unless otherwise noted.)

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC Performance							
Input Offset Voltage		V_{OS}	V_{CM} = V_{DD}/2		0.3	1.6	mV
			-40℃ ≤ T_A ≤ +85℃			1.7	
Input Common Mode Voltage Range		V_{CMR}		V_{SS} - 0.1		V_{DD} + 0.1	V
Common Mode Rejection Ratio		CMRR	V_{CM} = -0.1V to V_{DD} - 1.5V	65	78		dB
			-40℃ ≤ T_A ≤ +85℃	63			
Large-Signal Voltage Gain		A_{VO}	V_{CM} = V_{DD}/2, R_L = 10kΩ	87	92		dB
			-40℃ ≤ T_A ≤ +85℃	80			
Output Voltage Swing From Rail		V_{OH}	V_{CM} = V_{DD}/2, R_L = 10kΩ to V_{DD}/2		4	12	mV
			-40℃ ≤ T_A ≤ +85℃			14	
		V_{OL}	V_{CM} = V_{DD}/2, R_L = 10kΩ to V_{DD}/2		4	12	mV
			-40℃ ≤ T_A ≤ +85℃			14	
Output Short Circuit Current		I_{SOURCE}	V_{CM} = V_{DD}/2, R_L = 10Ω to V_{DD}/2	19	24		mA
			-40℃ ≤ T_A ≤ +85℃	15			
		I_{SINK}	V_{CM} = V_{DD}/2, R_L = 10Ω to V_{DD}/2	19	24		mA
			-40℃ ≤ T_A ≤ +85℃	14			
Power Supply Rejection Ratio		PSRR	V_{DD} = 1.4V to 5.5V	75	84		dB
			-40℃ ≤ T_A ≤ +85℃	69			
Operating Voltage Range				1.4		5.5	V
Quiescent Current		I_Q	V_{CM} = V_{DD}/2, I_O = 0		6.5	12.5	μA
			-40℃ ≤ T_A ≤ +85℃			14.5	
AC Performance							
Slew Rate	UP	SR	f = 100Hz, V_{OUT} = 1V_{PP} Step, A_V = 1		5.8		V/ms
	DOWN				3		
Gain-Bandwidth Product		GBP	R_F = 100kΩ, R_G = 10kΩ, R_L = 1MΩ, A_V = 10		11		kHz
Phase Margin			R_F = 100kΩ, R_G = 10kΩ, R_L = 1MΩ, A_V = 10		68		°
Input Voltage Noise			f = 0.1Hz to 10Hz		4.8		μV_{PP}
Input Voltage Noise Density		e_n	f = 1kHz, V_{CM} = V_{DD}/2		200		nV/$\sqrt{HZ}$

FUNCTIONAL BLOCK DIAGRAM

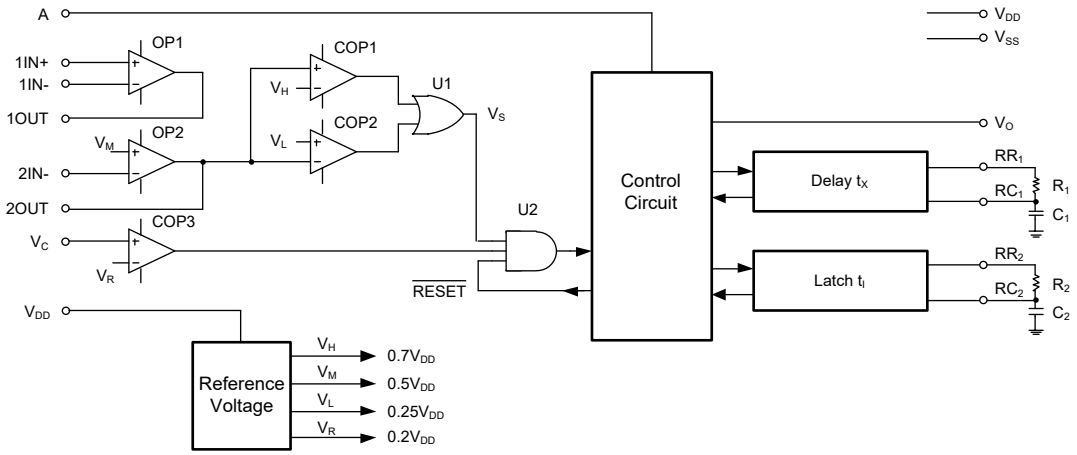


Figure 1. Functional Block Diagram

FUNCTIONAL DESCRIPTION

As shown in Figure 1, SGM8139 integrates operational amplifiers, bi-directional phase detector, status controller, delay timer, latch timer and voltage reference. SGM8139 supports two different working modes. One is non-repeatable trigger mode, and the other is repeatable trigger mode. In Figure 2, the waveforms of each pin show how SGM8139 works in non-repeatable trigger mode.

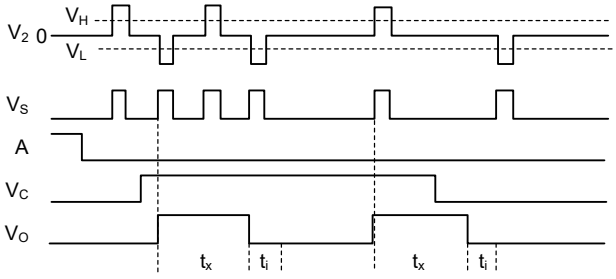


Figure 2. Non-repeatable Trigger Mode

First of all, with proper setup OP1 amplifies the output signal of PIR sensor, as the second stage OP2 conditions the signal from OP1 to an appropriate level, while the DC voltage is biased to VM ($\approx 0.5V_{DD}$). COP1 together with COP2 form a bi-directional amplitude detector after which the effective trigger signal V_S will be detected. Since $V_H \approx 0.7V_{DD}$ and $V_L \approx 0.25V_{DD}$, when V_{DD} = 5V, this circuit is immune to +/-1V noise interference, improving the system reliability. COP3 is a voltage comparator. When $V_C < V_R$ ($\approx 0.2V_{DD}$), COP3 output is low, setting AND gate U2 inactive. When $V_C > V_R$, COP3 output is high, and U2 is active. Meanwhile, the rising edge of V_S turns on the delay timer, while output of Vo keeps high during t_x period. When A is 0, any changes in V2 will be ignored in the t_x period. It is called non-repeatable trigger mode. When t_x ends, V_O drops to 0, and at the same time, the latch timer works. In the t_i period, any changes in V2 could not set V_O active. This setup can improve the anti-interference performance when switching loads.

Figure 3 shows how SGM8139 works in repeatable trigger mode.

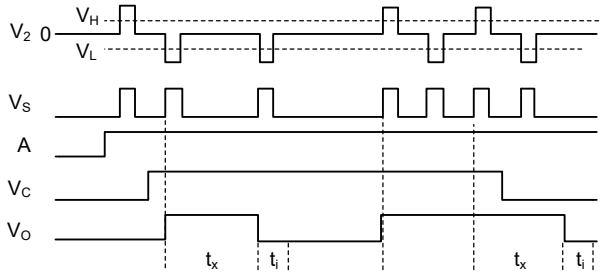


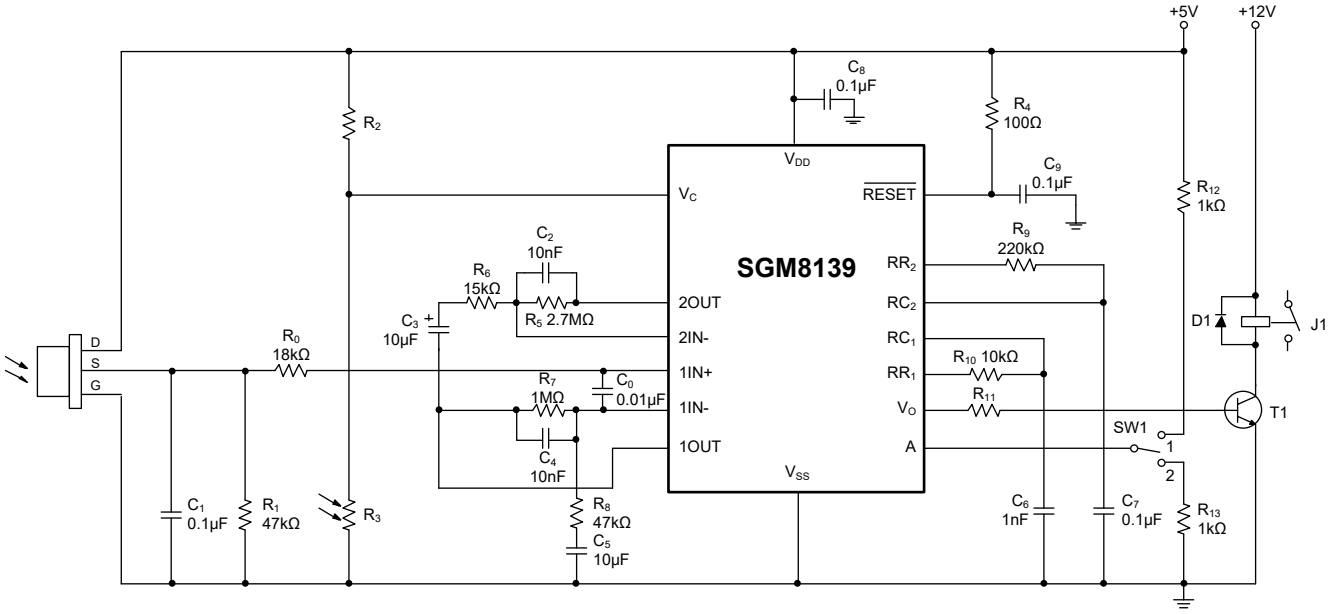
Figure 3. Repeatable Trigger Mode

When V_C = 0 and A = 0, any changes in V_S could not set V_O active. When V_C = 1 and A = 1, changing V_S could set V_O active and maintain active during t_x period. V_O will continue to delay another t_x period if any V_S rising edge occurs. If V_S is set to high, V_O keeps active. If V_S is set to low, V_O will be inactive after the t_x period ends, and V_O will keep inactive during t_i period while any changes in V_S could not trigger V_O to active mode.

APPLICATION CIRCUIT

In Figure 4, V_O can drive the transistor T1 to connect the supply and the load. R_3 is a photoresistance which detects the ambient light illumination. If it is in the day time, the value of R_3 decreases, thus V_C will drop to low level, and any trigger signal will be latched, saving electricity. This function can be bypassed by connecting V_C to V_{DD} directly when used in other application.

SW1 is a mode selection switch. When SW1 is connected to 1, the system is in repeatable trigger mode. When SW1 is connected to 2, the system is in non-repeatable trigger mode.



NOTES:

1. $A_{V1} = 1 + R_7/R_8 = 1 + 1000/47 \approx 22.27$
2. $A_{V2} = -R_5/R_6 = -2700/15 = -180$

Figure 4. Schematic for PIR I_{AMP} Switch Application

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

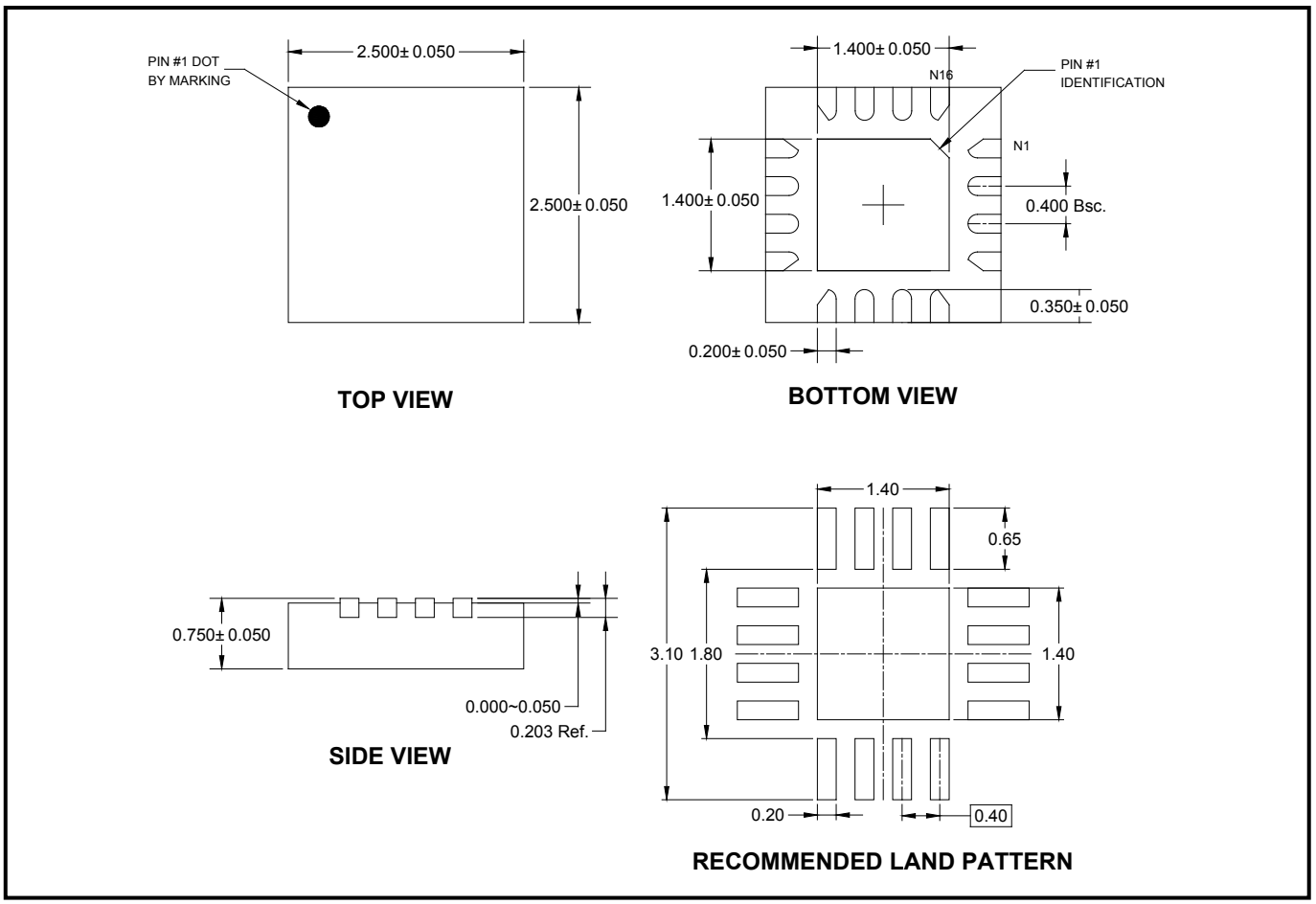
JANUARY 2018 – REV.A.1 to REV.A.2	**Page**
Added notes to Figure 4	8

MARCH 2017 – REV.A to REV.A.1	**Page**
Changed Pin Description section	3
Changed Application Circuit section	8

Changes from Original (DECEMBER 2016) to REV.A	**Page**
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

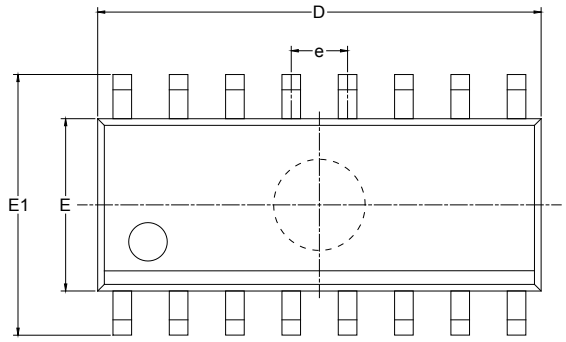
TQFN-2.5×2.5-16L

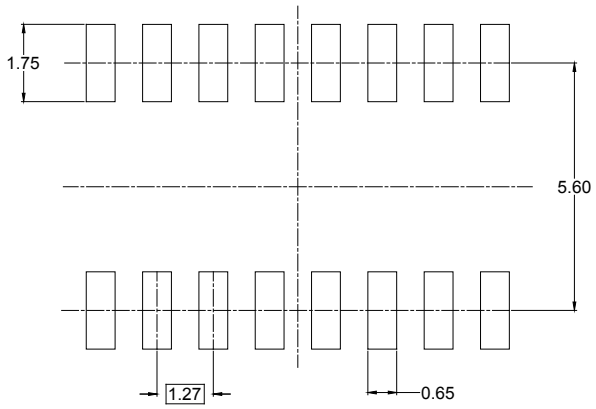


NOTE: All linear dimensions are in millimeters.

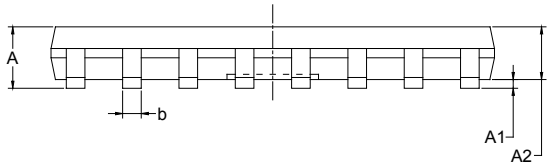
PACKAGE OUTLINE DIMENSIONS

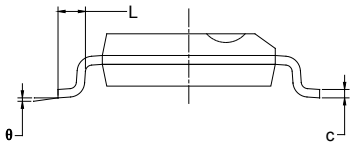
SOIC-16





RECOMMENDED LAND PATTERN (Unit: mm)

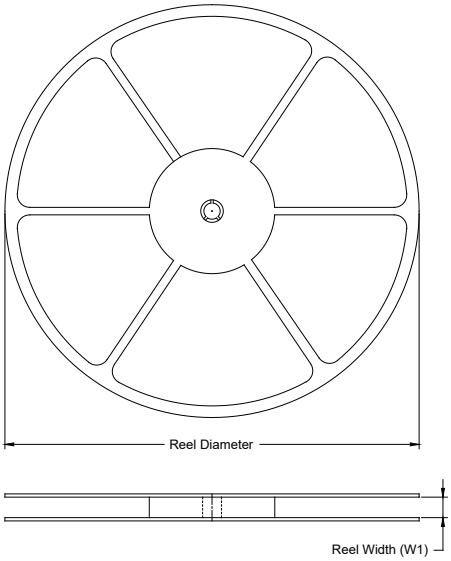




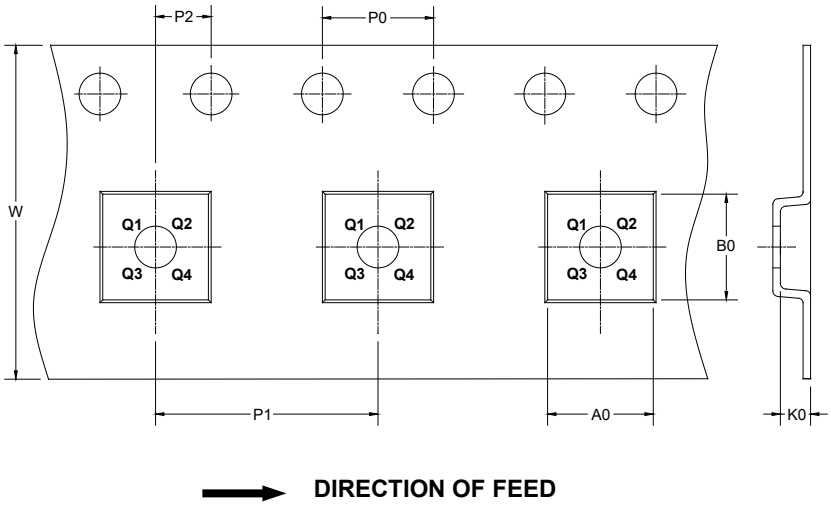
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	9.800	10.200	0.386	0.402
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.27 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



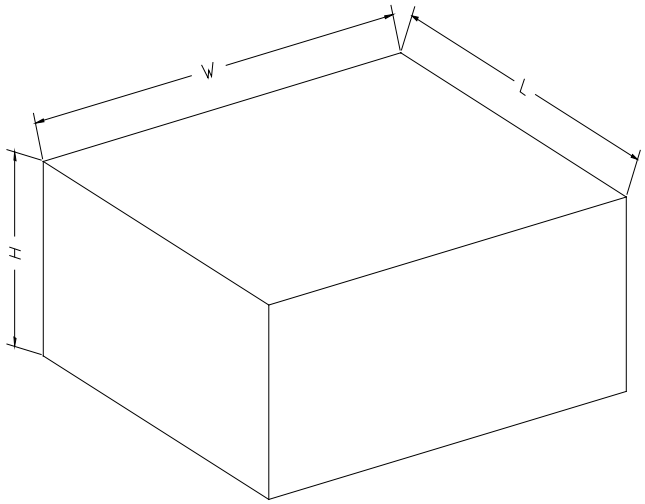
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-2.5×2.5-16L	7″	13.0	2.80	2.80	1.10	4.0	4.0	2.0	12.0	Q1
SOIC-16	13″	16.4	6.50	10.30	2.10	4.0	8.0	2.0	16.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18
13″	386	280	370	5

DD0002