SGM836
Microprocessor Supervisory Circuit with Programmable Delay Time

GENERAL DESCRIPTION

The SGM836 family can monitor system voltages from 0.4V to 5V. When the detection voltage falls below the preset threshold (V_{ITL}) or the manual reset (nMR) pin is driven low, the open-drain nRESET output is asserted. After the detection voltage and nMR voltage return higher than their respective thresholds, the nRESET output remains low within the user-adjustable delay time.

The SGM836 uses a precision reference to achieve 1% threshold accuracy. The fixed reset timeout period can be set to 20ms by leaving the C_T pin open and can be set to 300ms by connecting the C_T pin to V_{DD} through a resistor. The programmable reset timeout period can be set from 1.25ms to 10s through an external capacitor connected to the C_T pin. Low quiescent current makes the SGM836 very suitable for battery-powered applications.

The SGM836 is available in Green SOT-23-6 and TDFN-2×2-6AL packages.

FEATURES

- **Adjustable Reset Timeout Period: 1.25ms to 10s**
- **Low Quiescent Current: 0.6μA (TYP)**
- **High Threshold Accuracy: 1% (TYP)**
- **Factory-Set Detection Voltages: 0.9V to 5V**
- **Adjustable Detection Voltage Down to 0.4V**
- **Manual Reset (nMR) Input**
- **Open-Drain nRESET Output**
- **Available in Green SOT-23-6 and TDFN-2×2-6AL Packages**

APPLICATIONS

Computers
Portable Equipment
Intelligent Instruments
Microprocessor Systems
Critical μP Power Monitoring

TYPICAL APPLICATION

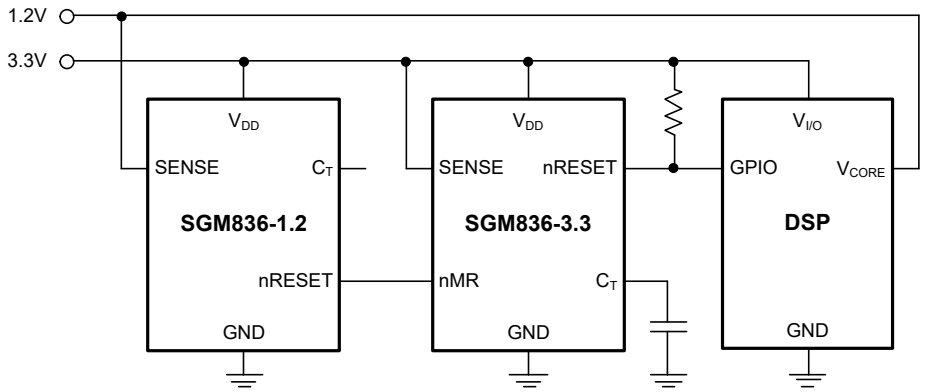


Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	THRESHOLD VOLTAGE (V_{ITL}) (V)	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM836-0.9	0.84	SOT-23-6	-40℃ to +125℃	SGM836-0.9XN6G/TR	R6AXX	Tape and Reel, 3000
		TDFN-2×2-6AL	-40℃ to +125℃	SGM836-0.9XTDI6G/TR	R18 XXXX	Tape and Reel, 3000
SGM836-1.2	1.12	SOT-23-6	-40℃ to +125℃	SGM836-1.2XN6G/TR	R6BXX	Tape and Reel, 3000
		TDFN-2×2-6AL	-40℃ to +125℃	SGM836-1.2XTDI6G/TR	R19 XXXX	Tape and Reel, 3000
SGM836-1.25	1.16	SOT-23-6	-40℃ to +125℃	SGM836-1.25XN6G/TR	R6CXX	Tape and Reel, 3000
		TDFN-2×2-6AL	-40℃ to +125℃	SGM836-1.25XTDI6G/TR	R1A XXXX	Tape and Reel, 3000
SGM836-1.5	1.40	SOT-23-6	-40℃ to +125℃	SGM836-1.5XN6G/TR	R6EXX	Tape and Reel, 3000
		TDFN-2×2-6AL	-40℃ to +125℃	SGM836-1.5XTDI6G/TR	R1B XXXX	Tape and Reel, 3000
SGM836-1.8	1.67	SOT-23-6	-40℃ to +125℃	SGM836-1.8XN6G/TR	R71XX	Tape and Reel, 3000
		TDFN-2×2-6AL	-40℃ to +125℃	SGM836-1.8XTDI6G/TR	R1C XXXX	Tape and Reel, 3000
SGM836-1.9	1.77	SOT-23-6	-40℃ to +125℃	SGM836-1.9XN6G/TR	R73XX	Tape and Reel, 3000
		TDFN-2×2-6AL	-40℃ to +125℃	SGM836-1.9XTDI6G/TR	R1D XXXX	Tape and Reel, 3000
SGM836-2.5	2.33	SOT-23-6	-40℃ to +125℃	SGM836-2.5XN6G/TR	R76XX	Tape and Reel, 3000
		TDFN-2×2-6AL	-40℃ to +125℃	SGM836-2.5XTDI6G/TR	R1E XXXX	Tape and Reel, 3000
SGM836-2.7	2.52	SOT-23-6	-40℃ to +125℃	SGM836-2.7XN6G/TR	R78XX	Tape and Reel, 3000
		TDFN-2×2-6AL	-40℃ to +125℃	SGM836-2.7XTDI6G/TR	R1F XXXX	Tape and Reel, 3000
SGM836-2.9	2.7	SOT-23-6	-40℃ to +125℃	SGM836-2.9XN6G/TR	R7AXX	Tape and Reel, 3000
		TDFN-2×2-6AL	-40℃ to +125℃	SGM836-2.9XTDI6G/TR	R20 XXXX	Tape and Reel, 3000
SGM836-3.0	2.79	SOT-23-6	-40℃ to +125℃	SGM836-3.0XN6G/TR	R3DXX	Tape and Reel, 3000
		TDFN-2×2-6AL	-40℃ to +125℃	SGM836-3.0XTDI6G/TR	R21 XXXX	Tape and Reel, 3000
SGM836-3.3	3.07	SOT-23-6	-40℃ to +125℃	SGM836-3.3XN6G/TR	R7CXX	Tape and Reel, 3000
		TDFN-2×2-6AL	-40℃ to +125℃	SGM836-3.3XTDI6G/TR	R22 XXXX	Tape and Reel, 3000
SGM836-3.7	3.45	SOT-23-6	-40℃ to +125℃	SGM836-3.7XN6G/TR	R7EXX	Tape and Reel, 3000
		TDFN-2×2-6AL	-40℃ to +125℃	SGM836-3.7XTDI6G/TR	R23 XXXX	Tape and Reel, 3000
SGM836-4.0	3.73	SOT-23-6	-40℃ to +125℃	SGM836-4.0XN6G/TR	R80XX	Tape and Reel, 3000
		TDFN-2×2-6AL	-40℃ to +125℃	SGM836-4.0XTDI6G/TR	R24 XXXX	Tape and Reel, 3000
SGM836-4.5	4.2	SOT-23-6	-40℃ to +125℃	SGM836-4.5XN6G/TR	R82XX	Tape and Reel, 3000
		TDFN-2×2-6AL	-40℃ to +125℃	SGM836-4.5XTDI6G/TR	R25 XXXX	Tape and Reel, 3000

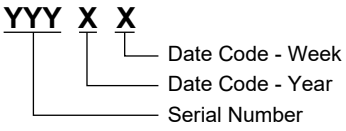
PACKAGE/ORDERING INFORMATION (continued)

MODEL	THRESHOLD VOLTAGE (V_{ITL}) (V)	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM836-5.0	4.65	SOT-23-6	-40℃ to +125℃	SGM836-5.0XN6G/TR	R84XX	Tape and Reel, 3000
		TDFN-2×2-6AL	-40℃ to +125℃	SGM836-5.0XTDI6G/TR	R26 XXXX	Tape and Reel, 3000
SGM836-ADJ	0.405	SOT-23-6	-40℃ to +125℃	SGM836-ADJXN6G/TR	R85XX	Tape and Reel, 3000
		TDFN-2×2-6AL	-40℃ to +125℃	SGM836-ADJXTDI6G/TR	R27 XXXX	Tape and Reel, 3000

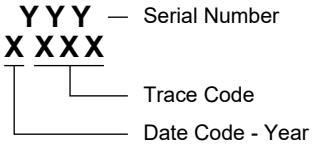
MARKING INFORMATION

NOTE: XX = Date Code. XXXX = Date Code and Trace Code.

SOT-23-6



TDFN-2×2-6AL



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND ..... -0.3V to 7V
C_T to GND ..... -0.3V to V_{DD} + 0.3V
nRESET, nMR, SENSE to GND ..... -0.3V to 7V
nRESET Pin Current ..... ±5mA
Package Thermal Resistance
SOT-23-6, θ_{JA} ..... 243℃/W
TDFN-2×2-6AL, θ_{JA} ..... 124℃/W
TDFN-2×2-6AL, $\theta_{JC(TOP)}$ ..... 129℃/W
TDFN-2×2-6AL, $\theta_{JC(BOT)}$ ..... 33℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 4000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Input Supply Voltage Range, V_{DD} ..... 1.65V to 6.5V
SENSE Pin Voltage, V_{SENSE} ..... 0V to 6.5V
C_T Pin Voltage, V_{CT} ..... V_{DD} (MAX)
nMR Pin Voltage, V_{nMR} ..... 0V to 6.5V
nRESET Pin Voltage, V_{nRESET} ..... 0V to 6.5V
nRESET Pin Current, I_{nRESET} ..... 0.0003mA to 5mA
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

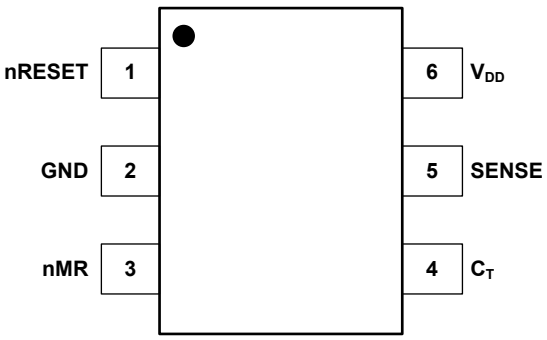
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

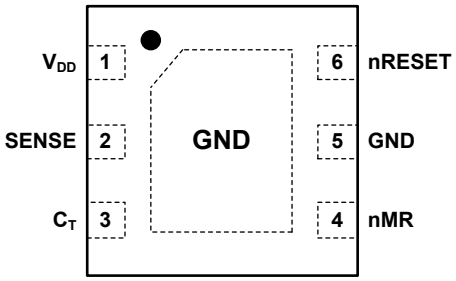
PIN CONFIGURATIONS

(TOP VIEW)



SOT-23-6

(TOP VIEW)



TDFN-2×2-6AL

PIN DESCRIPTION

PIN		NAME	I/O	FUNCTION
SOT-23-6	TDFN-2×2-6AL			
1	6	nRESET	O	Active-Low Reset Output Pin. nRESET remains low if the SENSE input is below V_{ITL} or nMR is logic low. It goes (or remains) low for the reset timeout period after the SENSE voltage exceeds V_{ITL} and nMR pin is driven high. It is recommended to connect a 10kΩ to 1MΩ pull-up resistor to this pin which enables the reset voltages greater than V_{DD}.
2	5	GND	—	Ground.
3	4	nMR	I	Manual Reset Input Pin. Pulling this pin (nMR) low will assert nRESET. nMR is internally pulled up to V_{DD} by a 100kΩ resistor.
4	3	C_T	I	Reset Timeout Delay Programming Pin. The fixed delay time can be set by connecting a 40kΩ to 200kΩ resistor between C_T pin and V_{DD} or leaving it open. And the programmable delay time can be set by connecting a capacitor no less than 100pF to the ground.
5	2	SENSE	I	The Dedicated Voltage Monitor Pin. If the SENSE voltage falls below V_{ITL}, the nRESET will be asserted.
6	1	V_{DD}	I	Supply Voltage.
—	Exposed Pad	GND	—	Exposed Pad. Connect it to the ground.

NOTE: I: input, O: output.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 1.65V to 6.5V, R_{LRESET} = 100kΩ (1), T_J = -40℃ to +125℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply Range	V_{DD}		1.65		6.5	V
Supply Current (Current into V_{DD} Pin)	I_{DD}	V_{DD} = 3.3V, nRESET not asserted, nMR, nRESET, C_T open		0.6	1.5	μA
		V_{DD} = 6.5V, nRESET not asserted, nMR, nRESET, C_T open		0.9	2	
Low-Level Output Voltage	V_{OL}	1.3V ≤ V_{DD} < 1.8V, I_{OL} = 0.4mA			0.2	V
		1.8V ≤ V_{DD} ≤ 6.5V, I_{OL} = 1mA			0.3	
Power-Up Reset Voltage (2)	V_{POR}	V_{OL} (MAX) = 0.2V, I_{nRESET} = 15μA			0.8	V
Negative-Going Input Threshold Accuracy	V_{ITL}	All versions, T_J = +25℃	-1.0		1.0	%
		V_{ITL} ≤ 3.3V	-1.5		1.5	
		3.3V < V_{ITL} ≤ 5.0V	-1.8		1.8	
		V_{ITL} ≤ 3.3V, T_J = -40℃ to +85℃	-1.25		1.25	
		3.3V < V_{ITL} ≤ 5.0V, T_J = -40℃ to +85℃	-1.3		1.3	
Positive-Going Input Threshold Accuracy	V_{ITH}	All versions			3.5	%
Hysteresis On V_{ITL}	V_{HYS}	All versions			3.5	%
nMR Internal Pull-Up Resistance	R_{nMR}		50	100		kΩ
Input Current at SENSE Pin	I_{SENSE}	SGM836-ADJ, V_{SENSE} = V_{ITL}	-25		25	nA
		Fixed versions, V_{SENSE} = 6.5V		235		
nRESET Leakage Current	I_{OH}	V_{nRESET} = 6.5V, nRESET not asserted			1	μA
Input Capacitance, Any Pin	C_{IN}	C_T pin, V_{IN} = 0V to V_{DD}		5		pF
		Other pins, V_{IN} = 0V to 6.5V		5		
nMR Input	V_{IL}	Logic Low	0		0.3 × V_{DD}	V
	V_{IH}	Logic High	0.7 × V_{DD}		V_{DD}	
Input Pulse Width to nRESET	t_{SENSE}	V_{IH} = 1.05 × V_{ITL}, V_{IL} = 0.95 × V_{ITL}		25		μs
	t_{nMR}	V_{IH} = 0.7 × V_{DD}, V_{IL} = 0.3 × V_{DD}		100		ns
C_T Source Threshold Voltage	$V_{TH-RAMP}$			1.206		V
nRESET Delay Time	t_D	C_T = Open	12	20	28	ms
		C_T = V_{DD}	180	300	420	
		C_T = 100pF	0.8	1.3	1.8	
Propagation Delay	t_{MR}	nMR to nRESET		250		ns
High-to-Low Level nRESET Delay	t_{RP0}	SENSE to nRESET		100		μs

NOTE:

1. R_{LRESET} is the resistor connected to the nRESET pin.

TIMING DIAGRAM

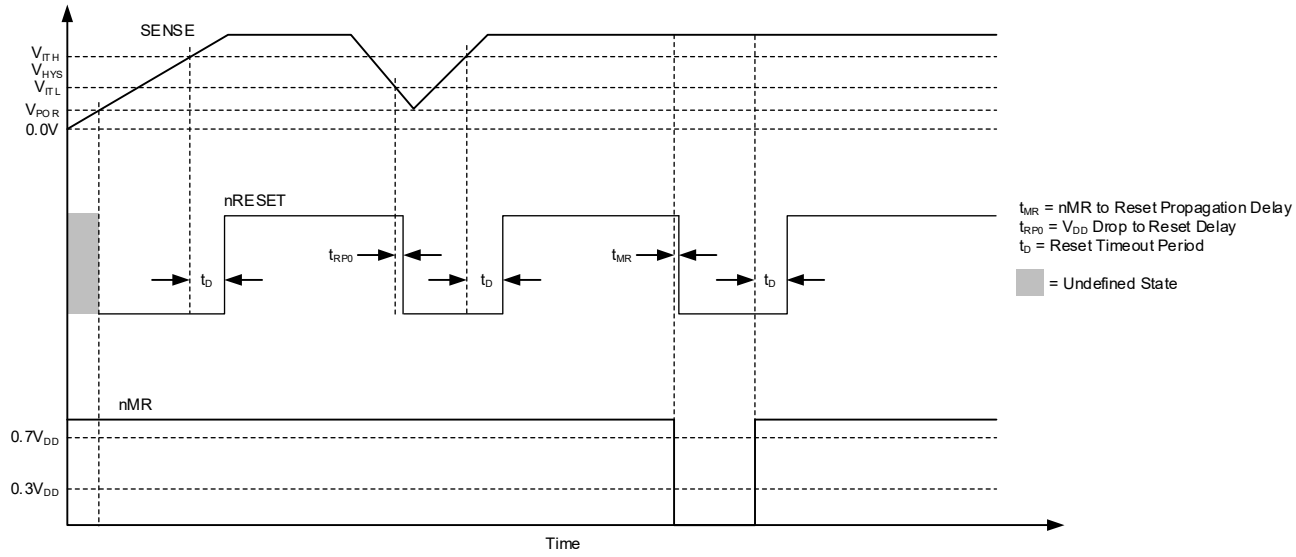
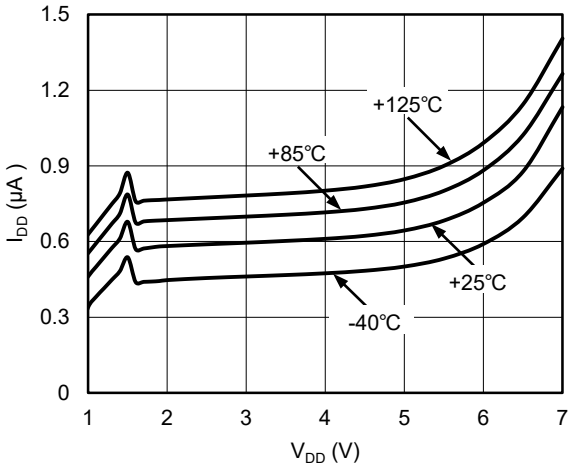


Figure 2. SGM836 Timing Diagram Showing nMR and SENSE Reset Timing

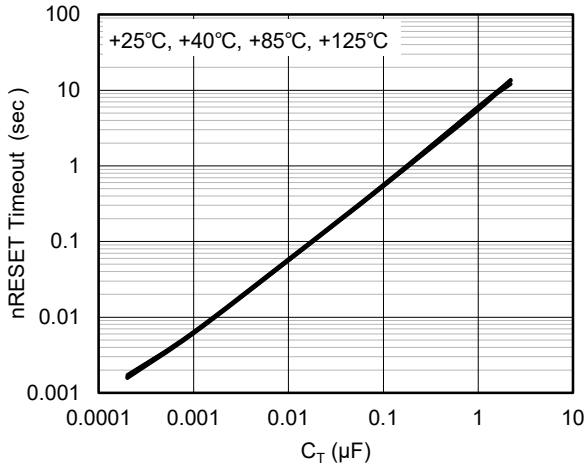
TYPICAL PERFORMANCE CHARACTERISTICS

T_J = +25℃, V_{DD} = 3.3V and R_{LRESET} = 100kΩ, unless otherwise noted.

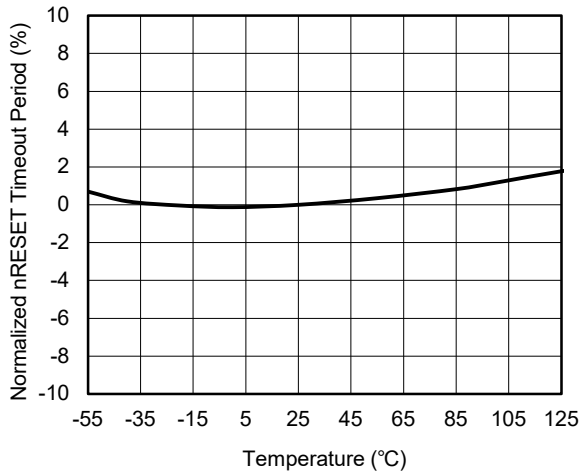
Supply Current vs. Supply Voltage



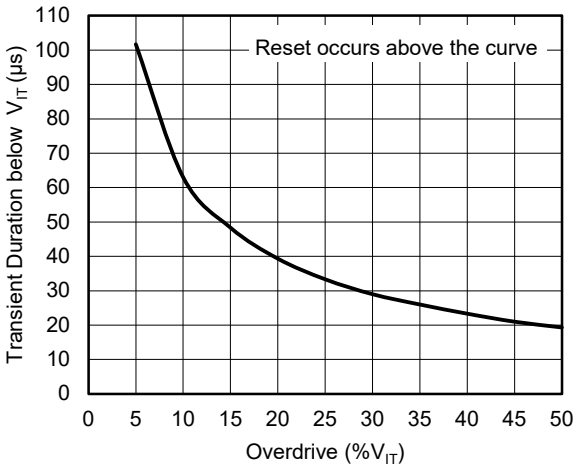
nRESET Timeout Period vs. C_T



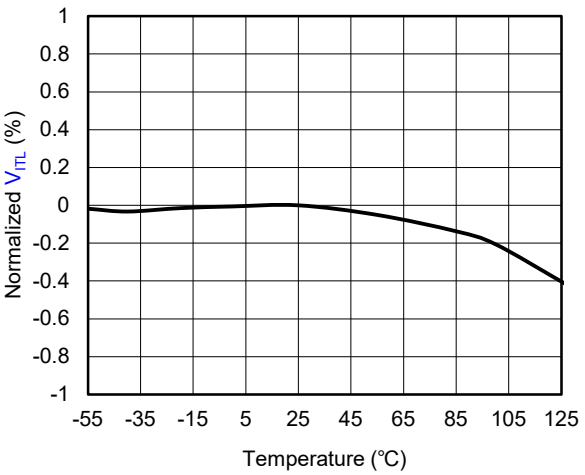
Normalized nRESET Delay Time vs. Temperature
(C_T = Open, C_T = V_{DD}, C_T = Any)



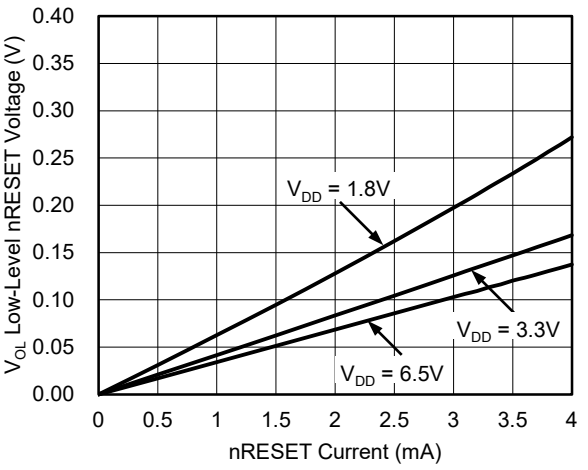
Maximum Transient Duration at SENSE vs. SENSE Threshold Overdrive Voltage



Normalized SENSE Threshold Voltage (V_{ITL}) vs. Temperature



Low-Level nRESET Voltage vs. nRESET Current



FUNCTIONAL BLOCK DIAGRAM

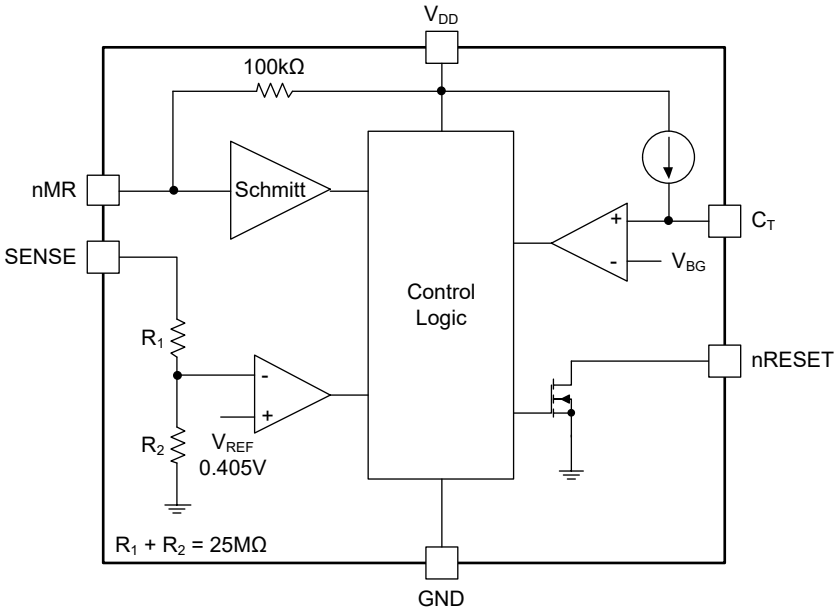


Figure 3. Fixed Voltage Version Block Diagram

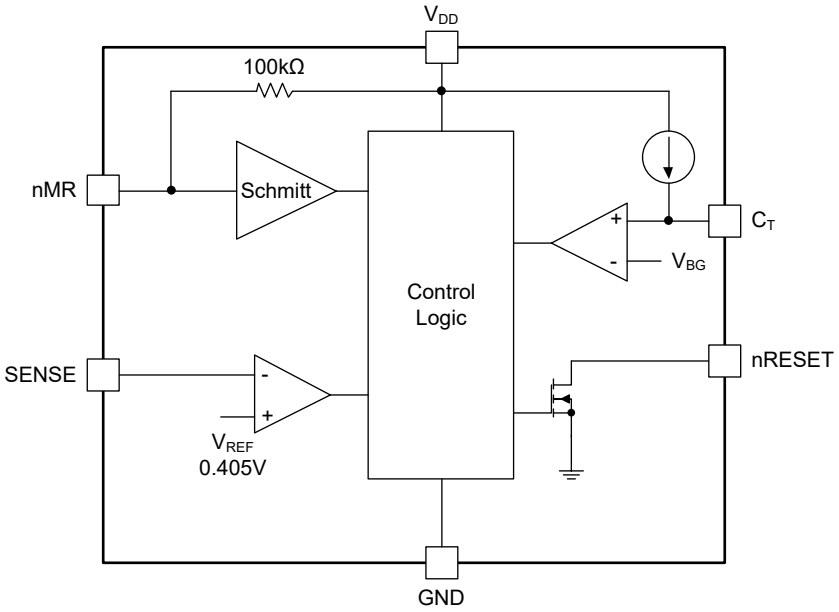


Figure 4. Adjustable Voltage Version Block Diagram

DETAILED DESCRIPTION

When the SENSE voltage falls below V_{ITL} or the nMR pin is driven low, the open-drain nRESET output is asserted. After the SENSE and nMR voltages exceed their respective thresholds, the nRESET output remains low within the user-adjustable delay time.

Feature Description

The SGM836 device has a reset delay time adjustment function and a wide range of detection thresholds, so it can be widely used in various applications. The detection threshold voltages are factory-set from 0.9V to 5V, while the SGM836-ADJ detection threshold voltages must be set above 0.405V through an external resistance divider. The fixed 20ms reset timeout period can be set by leaving the C_T pin open, and it also can be set to 300ms by connecting the C_T pin to V_{DD} through a resistor. The reset timeout period can be set from 1.25ms to 10s through programming an external capacitor which is connected to the C_T pin.

SENSE Input

The SENSE pin is dedicated for voltage monitor. The nRESET will be asserted if the SENSE voltage falls below V_{ITL}. The internal comparator has built-in hysteresis to ensure smooth nRESET. It is recommended to connect a bypass capacitor from 1nF to 10nF at the SENSE pin to reduce the sensitivity to voltage transient and PCB layout parasitic. The SGM836 immunes to short negative transients on the SENSE pin. Sensitivity to transients is dependent on the voltage overdrive on this pin. The SGM836-ADJ typical circuit shown in Figure 5, it can monitor any voltage rail as low as 0.405V.

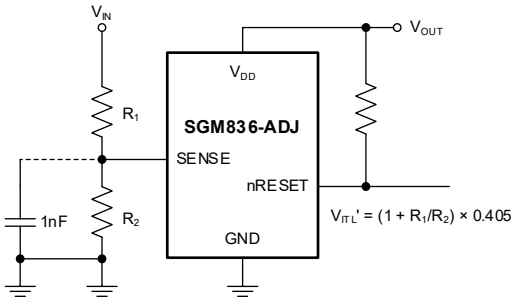


Figure 5. The SGM836-ADJ is used to monitor a User-Defined Threshold Voltage

Setting the Reset Delay Time

There are 3 typical applications to set the reset timeout delay in Figure 6, Figure 6 (a) shows the C_T pin is connected to V_{DD} through a resistor (from 40kΩ to 200kΩ must be used) to configure for a fixed 300ms delay time. Figure 6 (b) shows leaving the C_T pin open to set a fixed 20ms delay time. Figure 6 (c) shows that the user-defined time can be set through programming the capacitor between the C_T pin and the ground. t_D is always between 1.25ms and 10s.

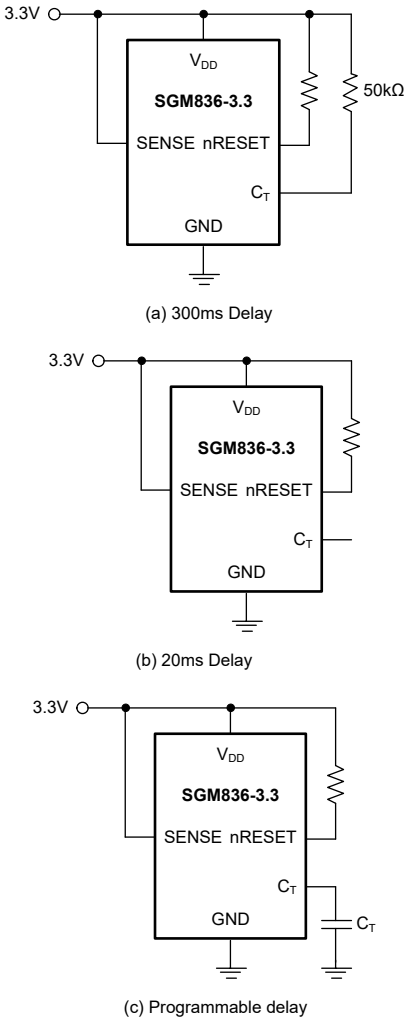


Figure 6. Different Setting methods of the nRESET Delay Time

The nominal value of C_T should be at least 100pF, so that the SGM836 can identify the presence of the capacitor. The reset timeout delay can be calculated by using Equation 1:

$$t_D\ (\mu s) = (5.58 \times 10^6) \times C_T\ (\mu F) + 520\mu s \quad (1)$$

DETAILED DESCRIPTION (continued)

Internally there is a precise 216nA current source, which charges the external capacitor C_T to 1.206V threshold, and this charge time will determine the reset timeout delay.

The capacitor will be discharged if nRESET is asserted. After clearing the nRESET condition, the internal current source will be enabled and the external capacitor will be recharged. When the voltage on the capacitor reaches 1.206V, nRESET is set to invalid. It is recommended to use low leakage capacitors such as ceramics, and the stray capacitance around the pins may cause errors in the reset delay time.

Manual Reset (nMR) Input

The manual reset (nMR) input allows the operator, test technician, or external logic circuit to initiate a reset. A logic low (0.3 × V_{DD}) on nMR forces the nRESET low. After nMR returns to a logic high and the SENSE voltage rises above its reset threshold, nRESET is deasserted after a reset delay time period (t_D). nMR is pulled up to V_{DD} with an internal 100kΩ resistor. This pin can be left floating if nMR is not used.

Figure 7 shows how to use nMR to monitor multiple system voltages. If the logic signal does not drive nMR fully to V_{DD}, some extra current will flow into V_{DD} due to the pull-up resistor on nMR. Figure 8 shows how to use an external FET to minimize the current draw.

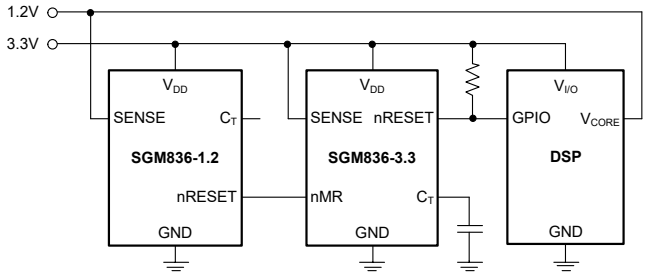


Figure 7. Monitor Multiple System Voltages Using the nMR Pin

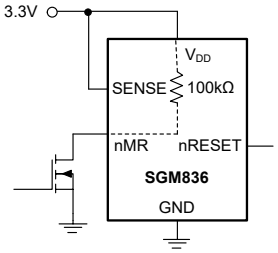


Figure 8. An External MOSFET is used to Minimize I_{DD}

nRESET Output

As long as SENSE voltage exceeds V_{ITL} and the nMR is logic high, nRESET remains high (deasserted). Either V_{SENSE} is lower than V_{ITL} or nMR is set low, nRESET will be low (asserted).

If nMR returns to logic high again and SENSE voltage exceeds V_{ITH} (V_{ITL} + V_{HYS}), nRESET will remain low for a fixed reset delay time due to the delay circuit function. As soon as the reset delay has expired, the nRESET turns into logic high. The pull-up resistor between nRESET and V_{DD} can be used to reset the microprocessor signal to obtain a voltage above V_{DD} voltage. The pull-up resistor should be no less than 10kΩ due to the limited nRESET pull-down ability.

Device Functional Modes

Table 1. Matrices of the nRESET Output

nMR	SENSE > V_{ITL}	nRESET
L	0	L
L	1	L
H	0	L
H	1	H

Normal Operation (V_{DD} > V_{DD_MIN})

When the V_{DD} voltage is higher than V_{DD_MIN}, the logic state of nRESET is determined by V_{SENSE} and the logic state of nMR.

• nMR high: When V_{DD} voltage is higher than 1.65V for a selected time (t_D), the nRESET logic state corresponds to V_{SENSE} relative to V_{ITL}.

• nMR low: nRESET is held low regardless of V_{SENSE} in this mode.

Above Power-On Reset but Lower than V_{DD_MIN} (V_{POR} < V_{DD} < V_{DD_MIN})

When the V_{DD} voltage is lower than V_{DD_MIN} and higher than the power-on reset voltage (V_{POR}), the nRESET is asserted and driven to a low-impedance state.

Below Power-On Reset (V_{DD} < V_{POR})

When the V_{DD} voltage is lower than the required voltage (V_{POR}), the nRESET voltage is undefined. In the case of nRESET pulling up to V_{DD} through a 100kΩ resistor, nRESET voltage is equal to or lower than V_{DD} voltage.

APPLICATION INFORMATION

The SGM836 requires a voltage supply within 1.65V and 6.5V. Figure 9 shows a typical application of the SGM836-2.5 used with a 2.5V microprocessor. Normally, the nRESET output is connected to the nRESET input of the microprocessor. It is necessary to connect a 1MΩ pull-up resistor between nRESET and V_{DD} to keep the nRESET logic high if it is not asserted.

The reset delay time can be set by C_T while it depends on the requirement of microprocessor. If left it open, a typical 20ms of reset delay time is set.

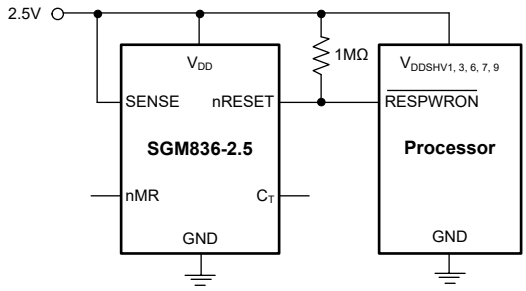


Figure 9. SGM836 Typical Application circuit with a Microprocessor

Voltage Transient on SENSE Pin

The short negative transient on the SENSE pin of the SGM836 can be relatively immune. The sensitivity to voltage transients depends on the value of threshold overdrive. The larger the overdrive is, the faster the nRESET responses. V_{ITL} is the threshold voltage in Equation 2. Use the percent of the sense voltage threshold to calculate the threshold overdrive.

$$\text{Overdrive} = | (V_{SENSE} / V_{ITL} - 1) \times 100\% | \quad (2)$$

Layout Guide

It is recommended to connect a 0.1μF ceramic capacitor to the V_{DD} pin as close as possible. If there is no connection capacitor, minimize the parasitic capacitor to avoid a significant impact on the nRESET delay time.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

APRIL 2023 – REV.A.2 to REV.A.3	Page
Updated Electrical Characteristics section	5

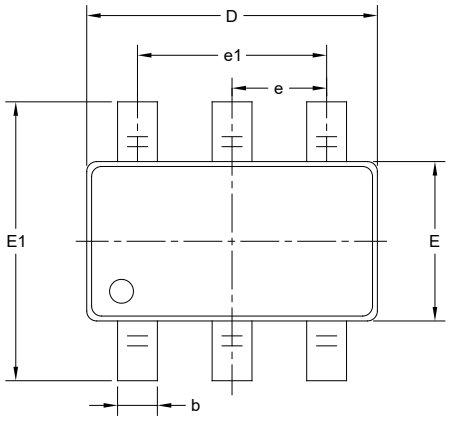
AUGUST 2022 – REV.A.1 to REV.A.2	Page
Updated Detail Description section	9-11
Added Application Information section	12
Updated Tape and Reel Information section	16

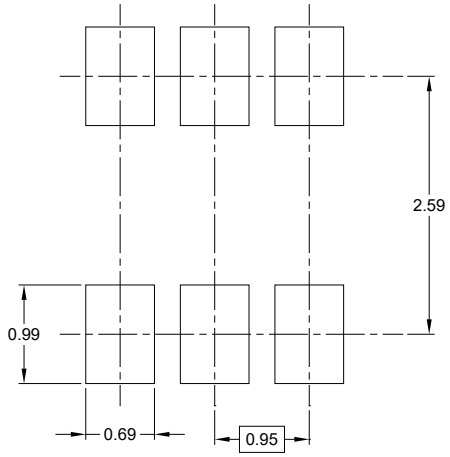
MAY 2022 – REV.A to REV.A.1	Page
Updated General Description section	1
Updated Detail Description section	9
Updated Tape and Reel Information section	12

Changes from Original (JANUARY 2021) to REV.A	Page
Changed from product preview to production data	All

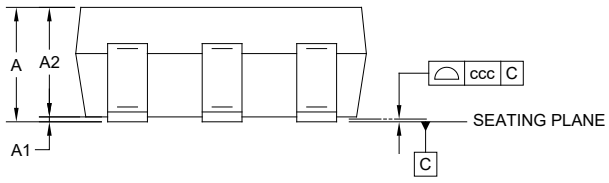
PACKAGE OUTLINE DIMENSIONS

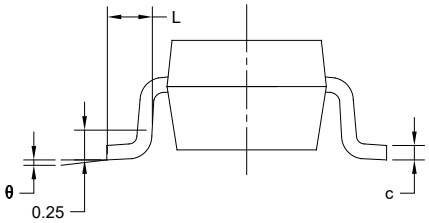
SOT-23-6





RECOMMENDED LAND PATTERN (Unit: mm)



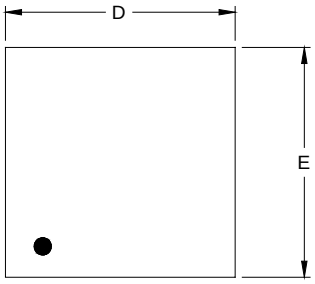


Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	-	-	1.450
A1	0.000	-	0.150
A2	0.900	-	1.300
b	0.300	-	0.500
c	0.080	-	0.220
D	2.750	-	3.050
E	1.450	-	1.750
E1	2.600	-	3.000
e	0.950 BSC		
e1	1.900 BSC		
L	0.300	-	0.600
θ	0°	-	8°
ccc	0.100		

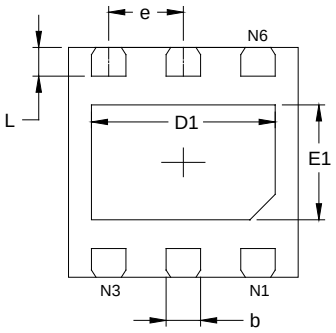
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-178.

PACKAGE OUTLINE DIMENSIONS

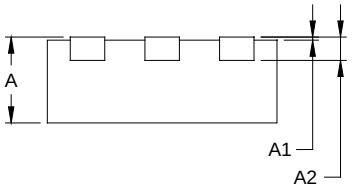
TDFN-2×2-6AL



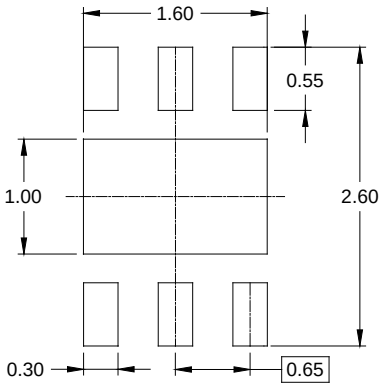
TOP VIEW



BOTTOM VIEW



SIDE VIEW



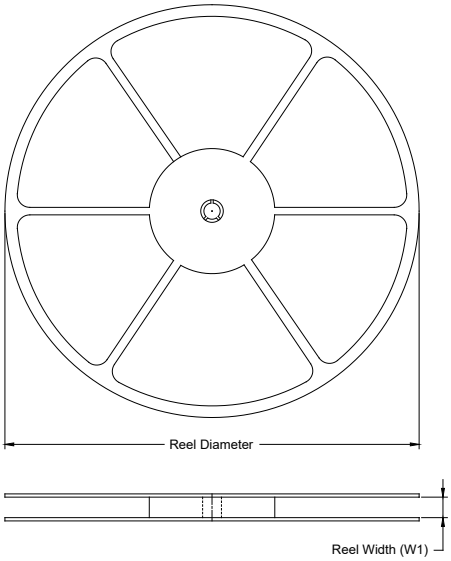
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
D	1.900	2.100	0.075	0.083
D1	1.500	1.700	0.059	0.067
E	1.900	2.100	0.075	0.083
E1	0.900	1.100	0.035	0.043
b	0.250	0.350	0.010	0.014
e	0.650 BSC		0.026 BSC	
L	0.174	0.326	0.007	0.013

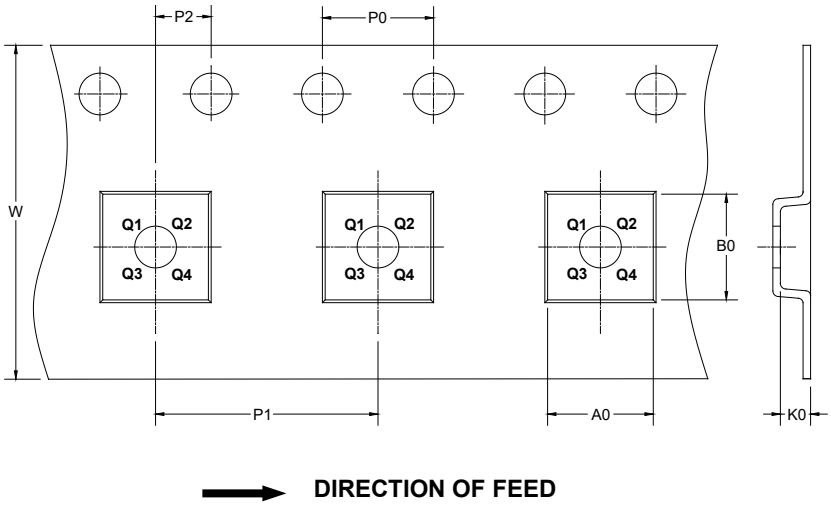
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



DIRECTION OF FEED

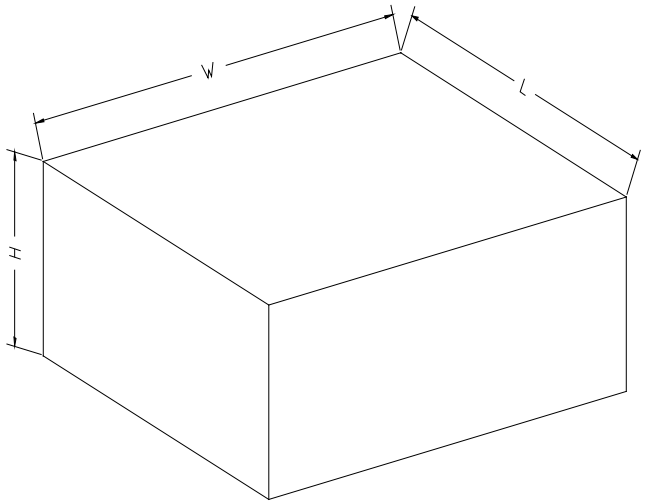
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOT-23-6	7″	9.5	3.23	3.17	1.37	4.0	4.0	2.0	8.0	Q3
TDFN-2×2-6AL	7″	9.5	2.30	2.30	1.10	4.0	4.0	2.0	8.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002