

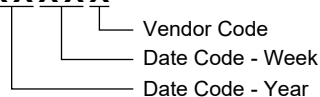
PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM38042-0	WLCSP-1.51×2.10-15B	-40°C to +85°C	SGM38042-0YG/TR	XXXXX GA8YG	Tape and Reel, 3000
SGM38042-1	WLCSP-1.51×2.10-15B	-40°C to +85°C	SGM38042-1YG/TR	XXXXX GA9YG	Tape and Reel, 3000
SGM38042-2	WLCSP-1.51×2.10-15B	-40°C to +85°C	SGM38042-2YG/TR	XXXXX GAAYG	Tape and Reel, 3000
SGM38042-3	WLCSP-1.51×2.10-15B	-40°C to +85°C	SGM38042-3YG/TR	XXXXX GABYG	Tape and Reel, 3000
SGM38042-4	WLCSP-1.51×2.10-15B	-40°C to +85°C	SGM38042-4YG/TR	XXXXX GACYG	Tape and Reel, 3000
SGM38042-5	WLCSP-1.51×2.10-15B	-40°C to +85°C	SGM38042-5YG/TR	XXXXX GADYG	Tape and Reel, 3000
SGM38042-6	WLCSP-1.51×2.10-15B	-40°C to +85°C	SGM38042-6YG/TR	XXXXX GAEYG	Tape and Reel, 3000
SGM38042-7	WLCSP-1.51×2.10-15B	-40°C to +85°C	SGM38042-7YG/TR	XXXXX GAFYG	Tape and Reel, 3000
SGM38042-8	WLCSP-1.51×2.10-15B	-40°C to +85°C	SGM38042-8YG/TR	XXXXX GB0YG	Tape and Reel, 3000
SGM38042-9	WLCSP-1.51×2.10-15B	-40°C to +85°C	SGM38042-9YG/TR	XXXXX GB1YG	Tape and Reel, 3000
SGM38042-10	WLCSP-1.51×2.10-15B	-40°C to +85°C	SGM38042-10YG/TR	XXXXX GB2YG	Tape and Reel, 3000
SGM38042-11	WLCSP-1.51×2.10-15B	-40°C to +85°C	SGM38042-11YG/TR	XXXXX GB3YG	Tape and Reel, 3000
SGM38042-12	WLCSP-1.51×2.10-15B	-40°C to +85°C	SGM38042-12YG/TR	XXXXX GF8YG	Tape and Reel, 3000

MARKING INFORMATION

XXXXXX = Date Code and Vendor Code.

XXXXXX



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

VIN, CVO_EN, P2N, 1W, DISP, DISN Voltages -0.3V to 6V
 CVO Voltage -0.3V to VIN + 0.3V
 SWN Voltage -6.7V to 6V
 SWN Voltage (Transient: 10ns, 1.6MHz) -8V to 8V
 NO, CNO Voltages -6.7V to 0.3V
 SWP, PO, CPO Voltages -0.3V to 6.7V
 SWP Voltage (Transient: 10ns, 1.6MHz) -2V to 8V
 Junction Temperature +150°C
 Storage Temperature Range -65°C to +150°C
 Lead Temperature (Soldering, 10s) +260°C
 ESD Susceptibility
 HBM 4000V
 MM 400V
 CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range 2.7V to 5.5V
 Operating Ambient Temperature Range -40°C to +85°C
 Operating Junction Temperature Range -40°C to +125°C

SELECTABLE MODEL

MODEL	DEFAULT OUTPUTS
SGM38042-0	VCPO = +5.4V/VCNO = -5.4V/VCVO = 2.8V
SGM38042-1	VCPO = +4.6V/VCNO = -3.5V/VCVO = 2.8V
SGM38042-2	VCPO = +5.0V/VCNO = -5.0V/VCVO = 2.8V
SGM38042-3	VCPO = +4.6V/VCNO = -2.4V/VCVO = 2.8V
SGM38042-4	VCPO = +6.4V/VCNO = -6.4V/VCVO = 2.8V
SGM38042-5	VCPO = +3.3V/VCNO = -3.0V/VCVO = 2.8V
SGM38042-6	VCPO = +5.4V/VCNO = -5.4V/VCVO = 1.8V
SGM38042-7	VCPO = +4.6V/VCNO = -3.5V/VCVO = 1.8V
SGM38042-8	VCPO = +5.0V/VCNO = -5.0V/VCVO = 1.8V
SGM38042-9	VCPO = +4.6V/VCNO = -2.4V/VCVO = 1.8V
SGM38042-10	VCPO = +6.4V/VCNO = -6.4V/VCVO = 1.8V
SGM38042-11	VCPO = +3.3V/VCNO = -3.0V/VCVO = 1.8V
SGM38042-12	VCPO = +4.6V/VCNO = -3.0V/VCVO = 2.8V

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

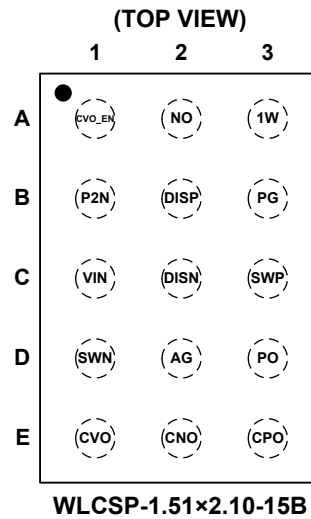
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



PIN DESCRIPTION

PIN	NAME	I/O	FUNCTION
A1	CVO_EN	I	Enable for CVO. 0: Disable the LDO; 1: Enable the LDO.
A2	NO	O	Converter Negative Output.
A3	1W	I	1-Wire Interface Input.
B1	P2N	I	Conditioned Positive and Negative Output Startup Sequence. Connected to VIN for starting conditioned positive output first; connected to AG for starting conditioned negative output first; connected to 1W for starting conditioned positive and negative outputs simultaneously.
B2	DISP	I	0: Disable Conditioned Positive Output Discharge; 1: Enable Conditioned Positive Output Discharge.
B3	PG	–	Power Ground.
C1	VIN	–	Supply Input.
C2	DISN	I	0: Disable Conditioned Negative Output Discharge; 1: Enable Conditioned Negative Output Discharge.
C3	SWP	O	Switch Node for Powering the Positive-Rail. Connect this pin to one end of power inductor.
D1	SWN	O	Switch Node for Powering the Negative-Rail. Connect this pin to the other end of power inductor.
D2	AG	–	Analog Ground.
D3	PO	O	Converter Positive Output.
E1	CVO	O	Output of the Linear Regulator.
E2	CNO	O	Conditioned Negative Output.
E3	CPO	O	Conditioned Positive Output.

ELECTRICAL CHARACTERISTICS(Tested at $T_A = +25^\circ\text{C}$, $V_{IN} = 3.7\text{V}$, $CVO_EN = 1\text{W} = P2N = V_{IN}$, Full = -40°C to $+85^\circ\text{C}$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
General Features							
Input Voltage Range	V_{IN}		$+25^\circ\text{C}$	2.7		5.5	V
Under-Voltage Lockout Threshold	V_{UVLO}	V_{IN} falling	$+25^\circ\text{C}$		2.2	2.65	V
Supply Current with No Load	I_Q	$V_{IN} = 3.7\text{V}$, no switching	$+25^\circ\text{C}$		0.5	0.7	mA
Shutdown Current	I_{OFF}	$V_{IN} = 3.7\text{V}$, $CVO_EN = 1\text{W} = P2N = \text{GND}$	$+25^\circ\text{C}$		0.4	1	μA
Power-On Blanking Time	t_{BLANK}	$V_{IN} = 3.7\text{V}$	$+25^\circ\text{C}$		40		ms
Switching Frequency	f_{SW}	$V_{IN} = 3.7\text{V}$	$+25^\circ\text{C}$	1.5	1.6	1.7	MHz
Inductor Peak Current	I_{PEAK}	$V_{IN} = 3.7\text{V}$	$+25^\circ\text{C}$	1.25	1.55	1.9	A
Conditioned Positive Output Voltage Range	V_{CPO}		$+25^\circ\text{C}$	2.4		6.4	V
Conditioned Positive Output Voltage Accuracy	$V_{CPO_ACC_46}$	$V_{IN} = 3.7\text{V}$, $V_{CPO} = +4.6\text{V}$	$+25^\circ\text{C}$	-45		+45	mV
	$V_{CPO_ACC_35}$	$V_{IN} = 3.7\text{V}$, $V_{CPO} = +3.5\text{V}$	$+25^\circ\text{C}$	-60		+60	mV
Discharge Resistor of Conditioned Positive Output	R_{DP}		$+25^\circ\text{C}$		50		Ω
Discharge Time of Conditioned Positive Output	t_{DISP}		$+25^\circ\text{C}$		10		ms
Conditioned Negative Output Voltage Range	V_{CNO}		$+25^\circ\text{C}$	-6.4		-2.4	V
Conditioned Negative Output Voltage Accuracy	$V_{CNO_ACC_24}$	$V_{IN} = 3.7\text{V}$, $V_{CNO} = -2.4\text{V}$	$+25^\circ\text{C}$	-45		+45	mV
	$V_{CNO_ACC_35}$	$V_{IN} = 3.7\text{V}$, $V_{CNO} = -3.5\text{V}$	$+25^\circ\text{C}$	-55		+55	mV
Discharge Resistor of Conditioned Negative Output	R_{DN}		$+25^\circ\text{C}$		50		Ω
Discharge Time of Conditioned Negative Output	t_{DISN}		$+25^\circ\text{C}$		10		ms
Linear Regulator Output Voltage Accuracy	$V_{CVO_ACC_28}$	$V_{IN} = 3.7\text{V}$, $V_{CVO} = +2.8\text{V}$	$+25^\circ\text{C}$	-100		+100	mV
	$V_{CVO_ACC_18}$	$V_{IN} = 3.7\text{V}$, $V_{CVO} = +1.8\text{V}$	$+25^\circ\text{C}$	-45		+45	mV
Logic CVO_EN, P2N, 1W							
Low Level Input Voltage	V_{IL}	$V_{IN} = 2.7\text{V}$ to 5.5V	Full			0.35	V
High Level Input Voltage	V_{IH}	$V_{IN} = 2.7\text{V}$ to 5.5V	Full	1.05			V
CVO_EN and P2N Pull-Down Resistors	R_{EN}		$+25^\circ\text{C}$		200		$\text{k}\Omega$
Thermal Shutdown							
Thermal Shutdown Threshold	T_{SHDN}				150		$^\circ\text{C}$
Thermal Shutdown Hysteresis	T_{HYS}				15		$^\circ\text{C}$

1-WIRE INTERFACE TIMING CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
1-Wire Initial Time	t_{IH}		0.2		ms
Soft-Start Time by 1-Wire Enable	t_{SS}		1.2		ms
1-Wire High Level Pulse Time	t_{SH}	2	20	75	μ s
1-Wire Low Level Pulse Time	t_{SL}	2	20	75	μ s
1-Wire Signal Stop Indication Time	t_{STOP}		300	400	μ s
V_{OUT} Turn-Off Delay by 1-Wire	$t_{VO_OFF_DLY}$		10		ms
t_{WAIT} after Data	t_{WAIT}		0		μ s
1-Wire Turn-Off Detection Time	t_{OFF_DLY}		350	450	μ s

1-WIRE PROTOCOL

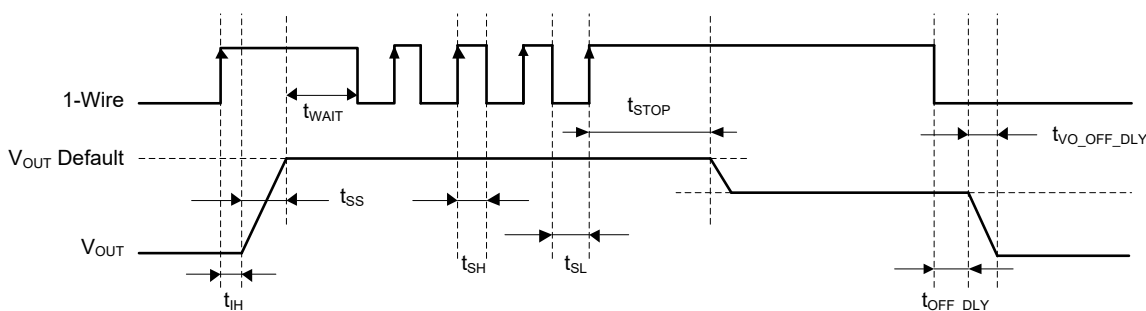


Figure 2. 1-Wire Protocol

1-WIRE PROGRAMMING

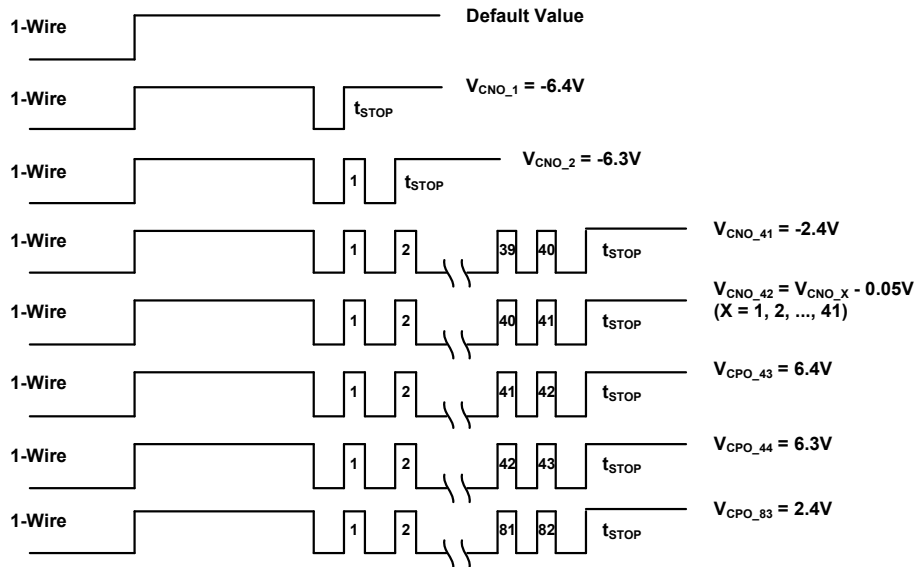


Figure 3. 1-Wire Programming

1-WIRE COUNTS TO VOLTAGE VALUE MAPPING

COUNTS	V _{CNO} (V)	V _{CPO} (V) ⁽¹⁾	COUNTS	V _{CNO} (V)	V _{CPO} (V)	COUNTS	V _{CNO} (V)	V _{CPO} (V)
1(43) ⁽¹⁾	-6.4	6.4	15(57)	-5.0	5.0	29(71)	-3.6	3.6
2(44)	-6.3	6.3	16(58)	-4.9	4.9	30(72)	-3.5	3.5
3(45)	-6.2	6.2	17(59)	-4.8	4.8	31(73)	-3.4	3.4
4(46)	-6.1	6.1	18(60)	-4.7	4.7	32(74)	-3.3	3.3
5(47)	-6.0	6.0	19(61)	-4.6	4.6	33(75)	-3.2	3.2
6(48)	-5.9	5.9	20(62)	-4.5	4.5	34(76)	-3.1	3.1
7(49)	-5.8	5.8	21(63)	-4.4	4.4	35(77)	-3.0	3.0
8(50)	-5.7	5.7	22(64)	-4.3	4.3	36(78)	-2.9	2.9
9(51)	-5.6	5.6	23(65)	-4.2	4.2	37(79)	-2.8	2.8
10(52)	-5.5	5.5	24(66)	-4.1	4.1	38(80)	-2.7	2.7
11(53)	-5.4	5.4	25(67)	-4.0	4.0	39(81)	-2.6	2.6
12(54)	-5.3	5.3	26(68)	-3.9	3.9	40(82)	-2.5	2.5
13(55)	-5.2	5.2	27(69)	-3.8	3.8	41(83)	-2.4	2.4
14(56)	-5.1	5.1	28(70)	-3.7	3.7	42	V _{CNO_X} - 0.05V	

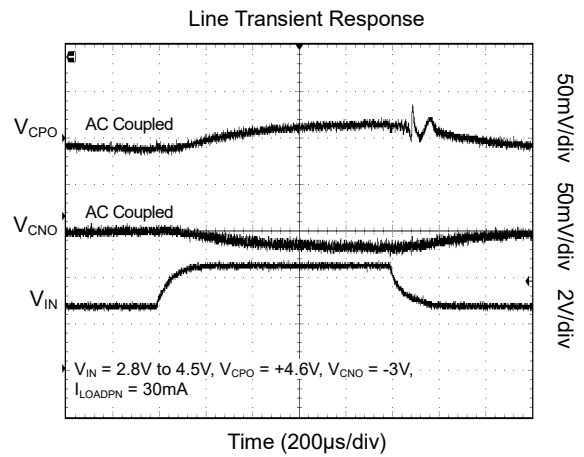
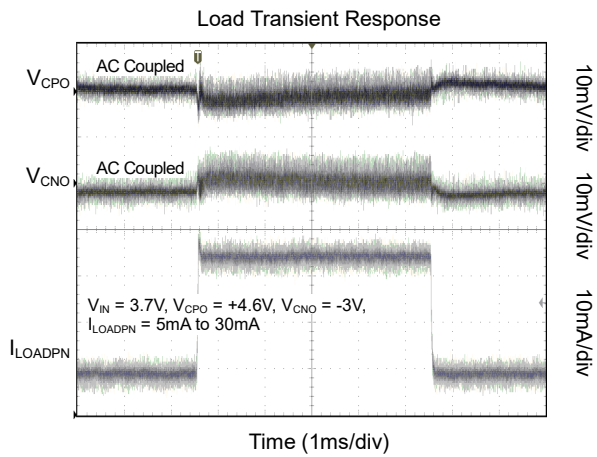
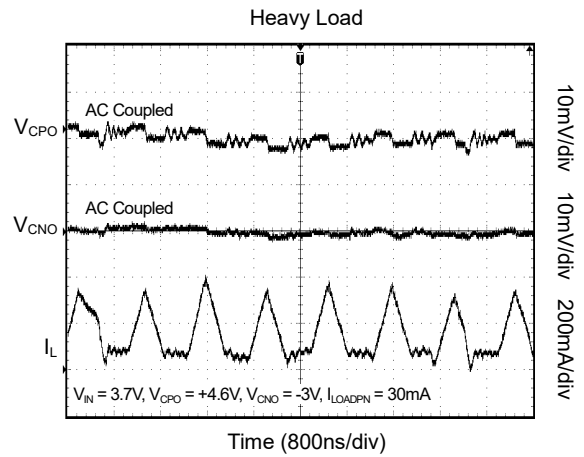
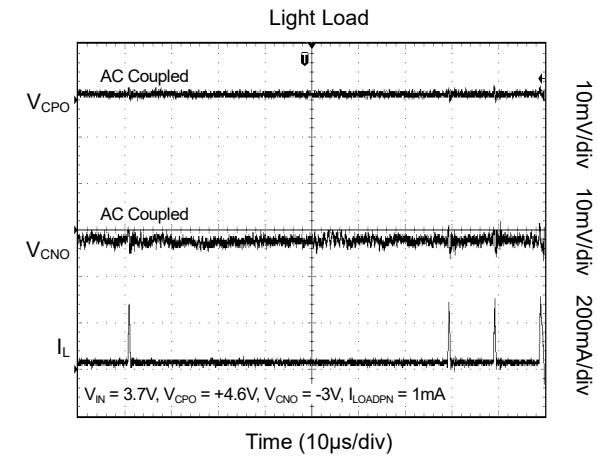
NOTE: 1. Conditioned negative voltage is programmed with counts 1 ~ 42. Conditioned positive voltage is programmed with counts 43 ~ 83, which are listed between parentheses.

RECOMMENDED COMPONENTS OF TEST CIRCUITS

COMPONENT		COMPONENT	
INDUCTOR	4.7μH/SLF7055T-4R7N3R1-3PF	CAPACITOR	10μF/08055C106KAT2A

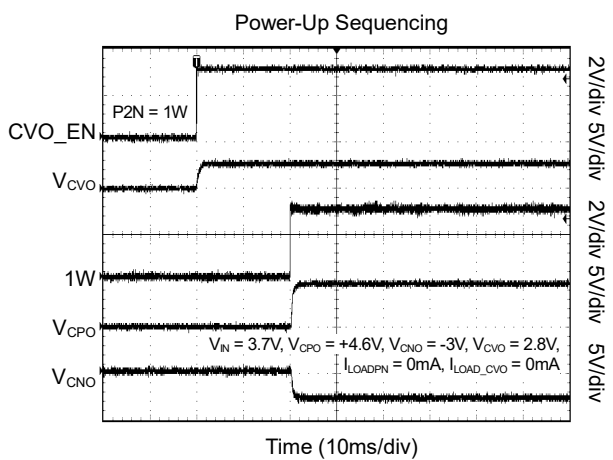
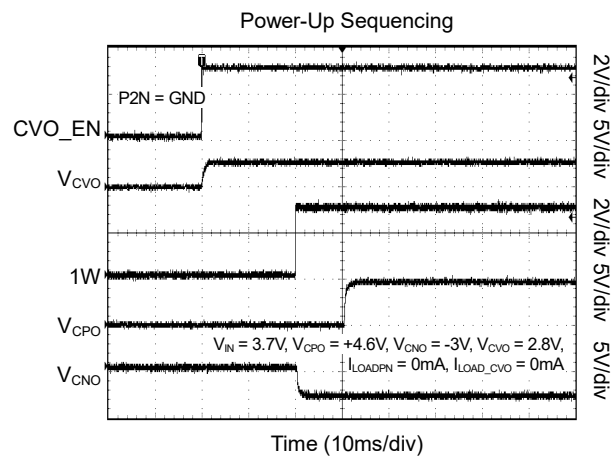
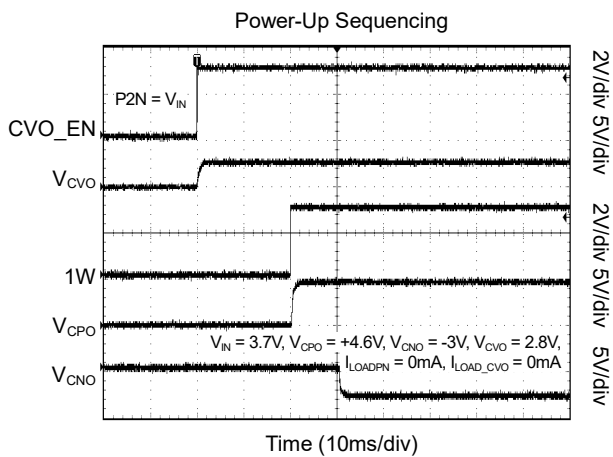
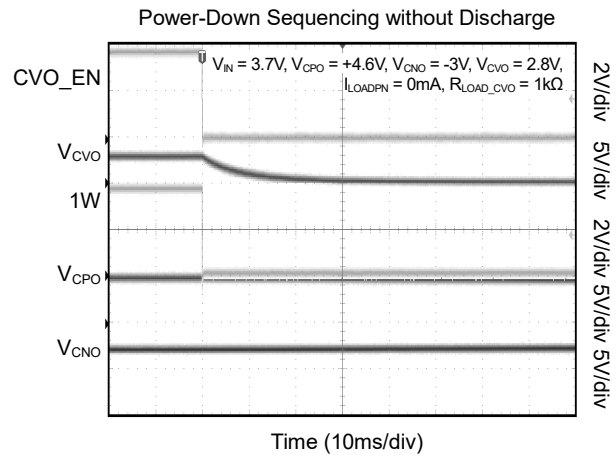
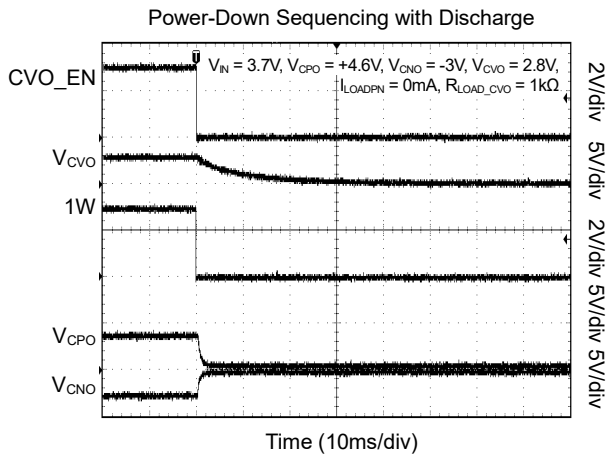
TYPICAL PERFORMANCE CHARACTERISTICS

Tested at $T_A = +25^{\circ}\text{C}$, $V_{IN} = 3.7\text{V}$, $CVO_EN = 1\text{W} = \text{P2N} = V_{IN}$, unless otherwise noted.



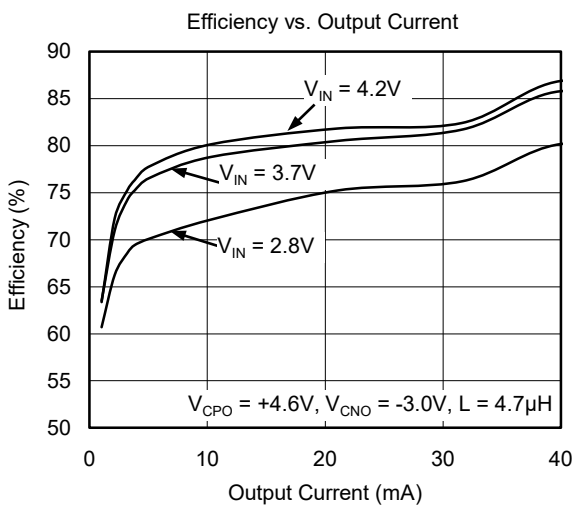
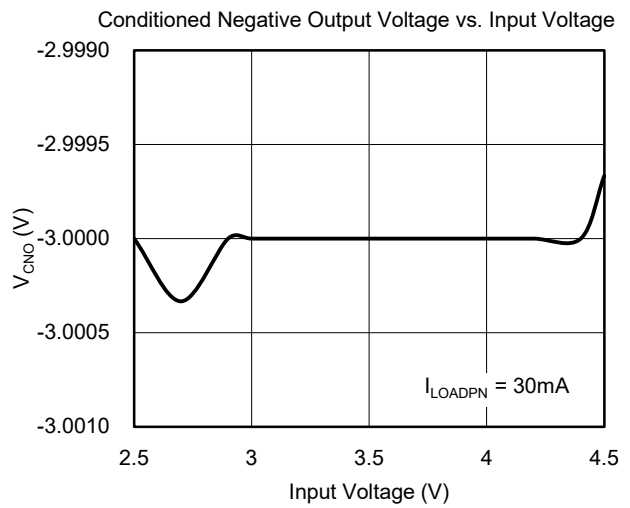
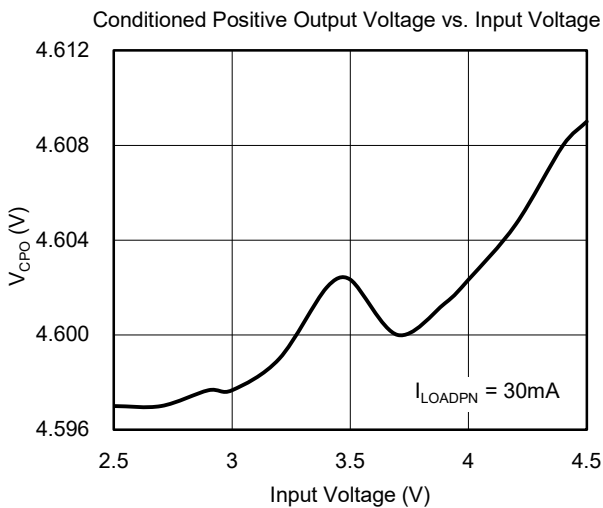
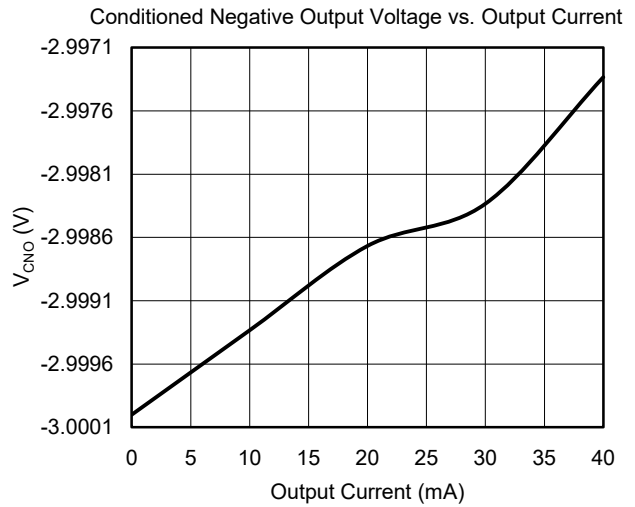
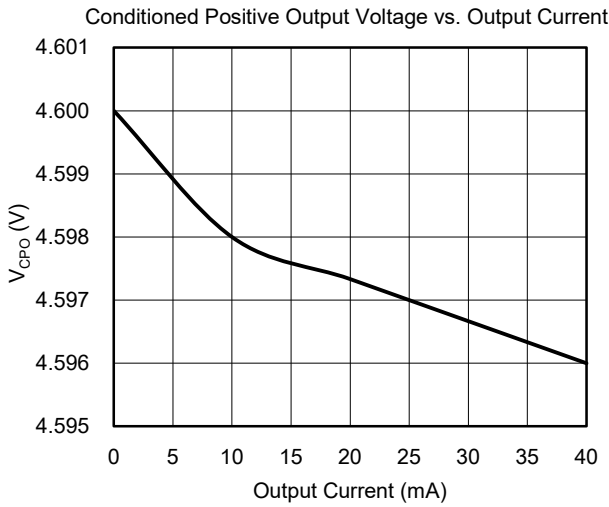
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Tested at $T_A = +25^\circ\text{C}$, $V_{IN} = 3.7\text{V}$, $CVO_EN = 1\text{W} = P2N = V_{IN}$, unless otherwise noted.



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Tested at $T_A = +25^\circ\text{C}$, $V_{IN} = 3.7\text{V}$, $CVO_EN = 1\text{W} = P2N = V_{IN}$, unless otherwise noted.



FUNCTIONAL BLOCK DIAGRAM

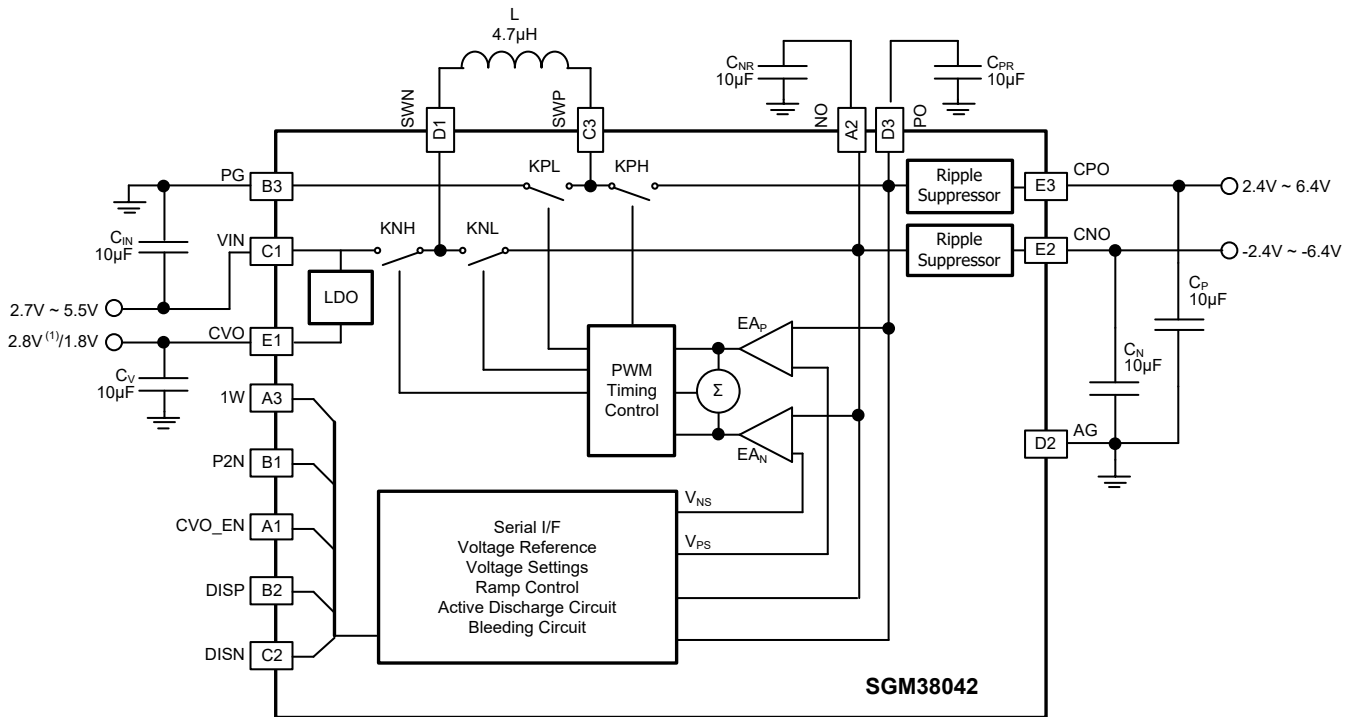


Figure 4. Functional Block Diagram

NOTE: 1. When $V_{IN} \geq 3.0V$, $V_{CVO} = 2.8V$.

FUNCTION, OPERATION AND APPLICATION

This device is a dedicated approach for providing triple outputs for AMOLED display panels. A unique control scheme is developed for suppressing the loading cross interference between two rails, which is considered as a common drawback when using single inductor to generate two rails. The circuit maintains regulation on both rails without compromising performance in either boost-inverter operation with any loading condition or buck-inverter operation with almost any loading condition. A linear regulator capable of 50mA output current is also integrated.

Soft-Start

The SGM38042 uses an internal soft-start feature to avoid high inrush currents during step-up.

Over-Temperature Protection (OTP)

The SGM38042 includes an OTP feature to prevent excessive power dissipation from overheating the device. The OTP will shut down switching operation when junction temperature exceeds +150°C. Once the junction temperature cools down by approximately 15°C, the converter resumes operation.

Over-Current Protection (OCP)

The SGM38042 includes a current sensing circuitry which monitors the inductor current during each ON period. If the current value becomes greater than the current limit, the switch charging the inductor will turn off, forcing the inductor to discharge.

Short Circuit Protection (SCP)

The SGM38042 has an advanced short circuit protection mechanism which prevents damage to the device from unexpected applications. When the output becomes shorted to ground, the current limit will decrease to 500mA and the switching frequency will fold back to 300kHz.

Under-Voltage Lockout

The SGM38042 integrates an under-voltage lockout block (UVLO) that enables the device once the voltage on VIN pin exceeds the UVLO rising threshold. No output voltage will however be generated as long as the enable signals are not pulled high. The device will be disabled as soon as the VIN voltage falls below the UVLO falling threshold.

A 40ms delay is starting as soon as the UVLO rising threshold is reached. This delay is implemented to prevent the device from being disabled or enabled by an unwanted VIN voltage spike. Once this delay has passed, the output rails can be enabled or disabled as desired with the enable signals without any delay.

Active Discharge

An active discharge of the conditioned positive output and/or the conditioned negative output can be controlled by DISP and DISN pin. If DISP and/or DISN are/is forced to be high, the discharge will occur at power-down. The discharge switch will be turned off after the 10ms discharge time.

Output Voltage

The output voltages of the converter are automatically adjusted depending on the programmed V_{CPO} and V_{CNO} voltages.

EMI and Acoustic Interference

Switching noise propagating along wire connections commonly dominates the EMI from the device operation, which may degrade receiver sensitivities by injecting interference into its carrier band or interim band through inter-modulation in its down converters. Inserting a ferrite bead into input power path and making short and straightforward path always work well in practice.

The device limits its lowest pulse skip frequency to be higher than audible frequency range for acoustic interference free operation.

Component and Parameter Selection

C_{IN} , C_V , C_{PR} , C_{NR} , C_P and C_N can be any capacitance in the range of 4.7 μ F ~ 47 μ F, and low loss Z5U, X7R and X5R dielectric capacitors are recommended for better performance. A 4.7 μ H inductor is recommended for the best efficiency.

Sequence

The 1W pin and P2N pin are used for generating the startup sequence of the conditioned positive and negative outputs. When the P2N pin is connected to VIN pin, the conditioned positive output will start first. When the P2N pin is connected to AG pin, the conditioned negative output will start first. When the P2N pin is connected to 1W pin, the conditioned positive and negative outputs will start simultaneously.

FUNCTION, OPERATION AND APPLICATION (continued)

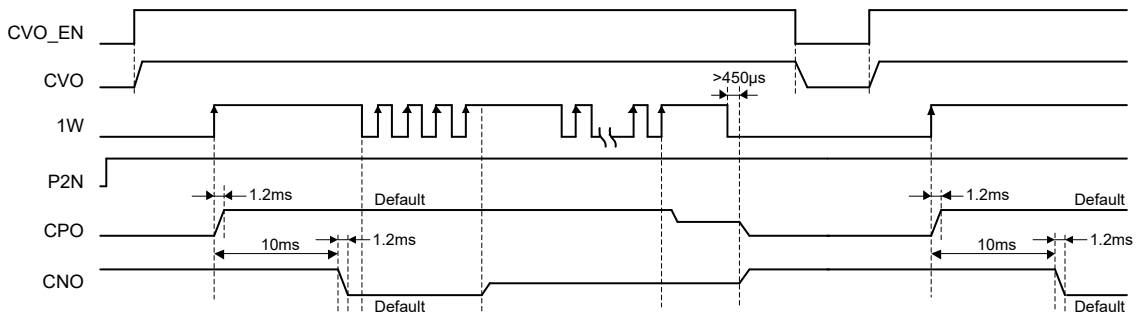


Figure 5. Startup Sequencing when P2N is Connected to VIN or Forced High

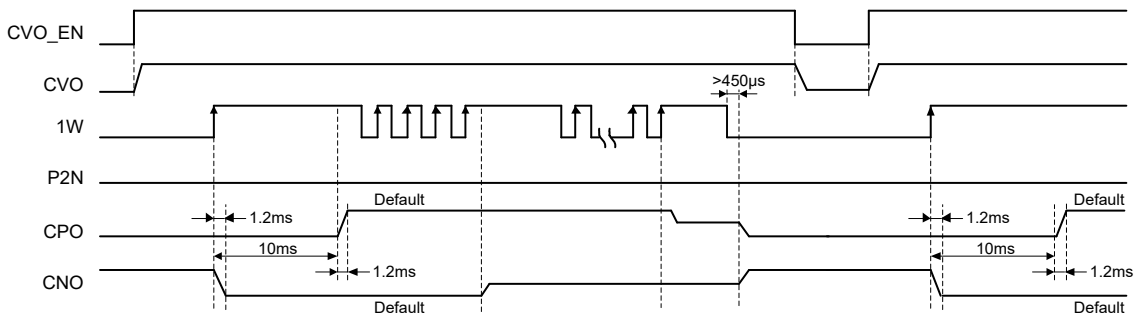


Figure 6. Startup Sequencing when P2N is Connected to GND or Forced Low

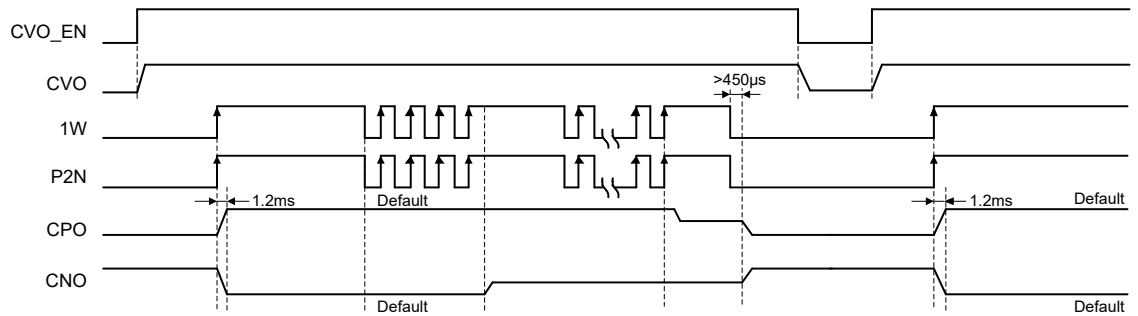


Figure 7. Startup Sequencing when P2N is Connected to 1W Pin

FUNCTION, OPERATION AND APPLICATION (continued)

PCB Layout Guidelines

PCB layout is an important task in the power supply design. Good PCB layout minimizes EMI and allows very good output voltage regulation. For the SGM38042 the following PCB layout guidelines are recommended.

- Keep the power ground plane on the top layer (all capacitor grounds and PG pins must be connected together with one uninterrupted ground plane).
- AG and PG must be connected together on the same ground plane.
- Always avoid vias when possible. They have high inductance and resistance. If vias are necessary, always use more than one in parallel to decrease parasitics especially for power lines.
- For high dv/dt signals (switch pin traces): keep copper to a minimum to prevent making unintentional parallel plate capacitors with other traces or to a ground plane. Best to route signal and return on same layer.
- For high di/dt signals: keep traces short, wide and closely spaced. This will reduce stray inductance and decrease the current loop area to help prevent EMI.
- Keep input capacitor close to the IC with low inductance traces.
- Keep trace from switching node pin to inductor short if possible: it reduces EMI emissions and noise that may couple into other portions of the converter.
- Isolate analog signal paths from power paths.

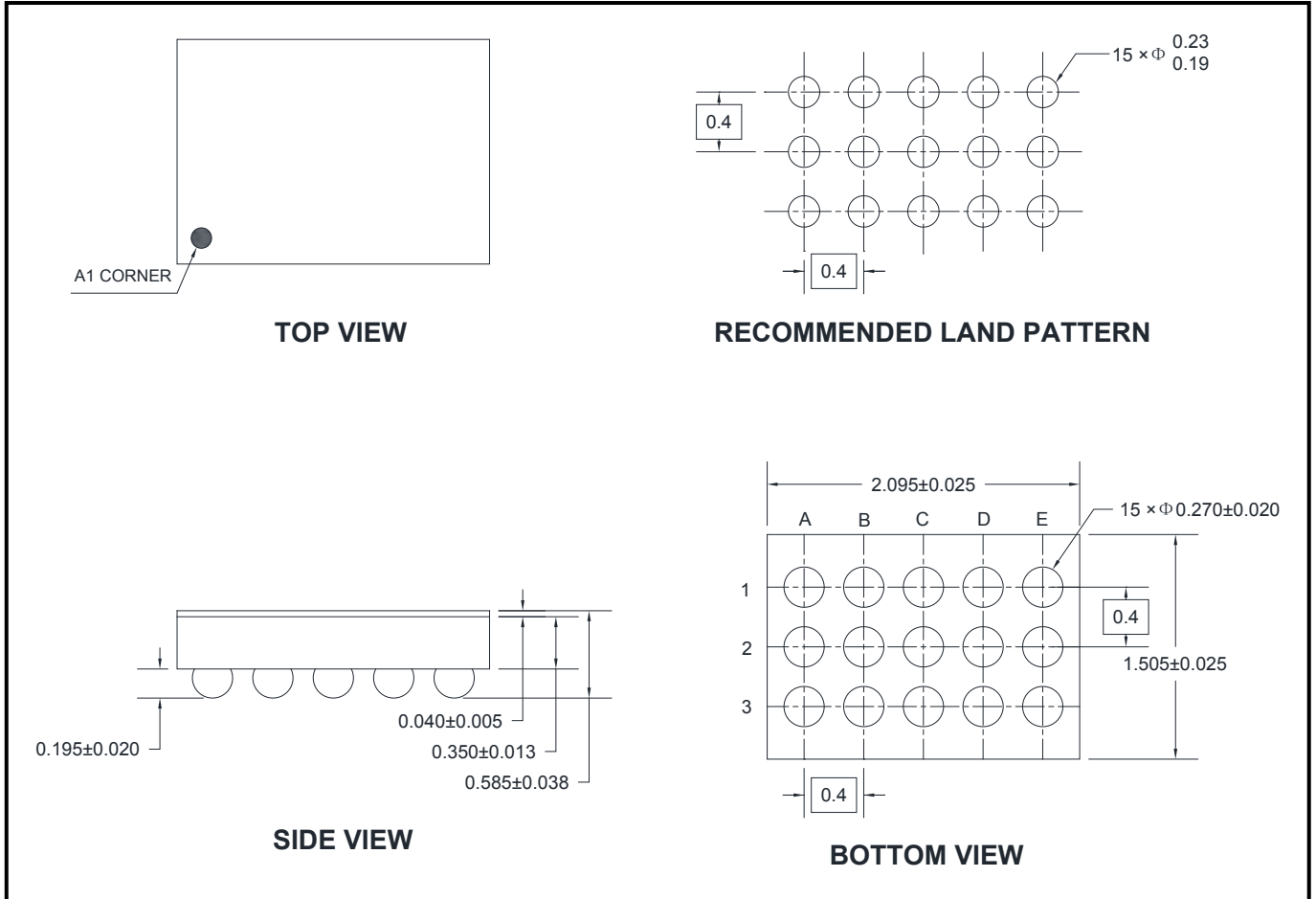
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

JANUARY 2021 – REV.A.2 to REV.A.3	Page
Updated Absolute Maximum Ratings.....	3
OCTOBER 2018 – REV.A.1 to REV.A.2	Page
Updated Absolute Maximum Ratings.....	3
MARCH 2018 – REV.A to REV.A.1	Page
Updated General Description.....	1
Changes from Original (DECEMBER 2017) to REV.A	Page
Changed from product preview to production data.....	All

PACKAGE OUTLINE DIMENSIONS

WLCSP-1.51×2.10-15B



NOTE: All linear dimensions are in millimeters.

PACKAGE INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
WLCSP-1.51×2.10-15B	7"	9.0	1.61	2.21	0.70	4.0	4.0	2.0	8.0	Q1

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PACKAGE INFORMATION

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7" (Option)	368	227	224	8
7"	442	410	224	18

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单击下面可查看定价，库存，交付和生命周期等信息

[>>SGMICRO\(圣邦微电子\)](#)