SGM51242R2/SGM51242R4/SGM51242R8 2-Channel, 4-Channel, 8-Channel, 12-Bit ADCs with On-Chip Reference, SPI Interface

GENERAL DESCRIPTION

The SGM51242R2, SGM51242R4, and SGM51242R8 are 12-bit ADCs, which have an analog multiplexer of 2-channel/4-channel/8-channel input, respectively. The input range of the ADC is 0V to V_{REF} or 0V to 2 × V_{REF}. The ADC has a total throughput rate of 250kSPS.

The SGM51242R2, SGM51242R4, and SGM51242R8 have an integrated 2.5V, 10ppm/℃ (TYP) reference, which is turned off by default, and an integrated temperature sensor, which gives an indication of the die temperature. The temperature value is read back as part of an ADC read sequence.

The SGM51242R2 is available in a Green TQFN-3×3-16BL. The SGM51242R4 and SGM51242R8 are available in Green TQFN-3×3-16BL and TSSOP-16 packages. They operate over an ambient temperature range of -40℃ to +125℃.

FEATURES

- **SGM51242R2: 2-Channel, 12-Bit ADC**
- **SGM51242R4: 4-Channel, 12-Bit ADC**
- **SGM51242R8: 8-Channel, 12-Bit ADC**
- **On-Chip Temperature Sensor**
- **Supply Monitor**
- **SPI Interface**
- **Available in Green TSSOP-16 and TQFN-3×3-16BL Packages**

APPLICATIONS

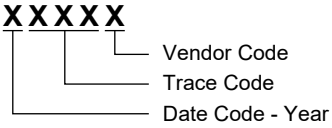
Control and Monitoring
General-Purpose Analog and Digital I/O

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM51242R2	TQFN-3×3-16BL	-40℃ to +125℃	SGM51242R2XTSK16G/TR	035SK XXXXX	Tape and Reel, 4000
SGM51242R4	TQFN-3×3-16BL	-40℃ to +125℃	SGM51242R4XTSK16G/TR	036SK XXXXX	Tape and Reel, 4000
	TSSOP-16	-40℃ to +125℃	SGM51242R4XTS16G/TR	SGM038 XTS16 XXXXX	Tape and Reel, 4000
SGM51242R8	TQFN-3×3-16BL	-40℃ to +125℃	SGM51242R8XTSK16G/TR	037SK XXXXX	Tape and Reel, 4000
	TSSOP-16	-40℃ to +125℃	SGM51242R8XTS16G/TR	SGM039 XTS16 XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Voltage Range (with Respect to GND)
V_{DD} (1) ..... -0.3V to 6V
V_{LOGIC} (1) ..... -0.3V to 6V
Analog Input Voltage ..... -0.3V to V_{DD} + 0.3V
Digital Input Voltage ..... -0.3V to V_{LOGIC} + 0.3V
Digital Output Voltage ..... -0.3V to V_{LOGIC} + 0.3V
V_{REF} ..... -0.3V to V_{DD} + 0.3V
Package Thermal Resistance
TQFN-3×3-16BL, θ_{JA} ..... 96.7℃/W
TSSOP-16, θ_{JA} ..... 115.3℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 1500V
CDM 500V

NOTE:
1. V_{DD} is powered up first, and the V_{DD} voltage must be higher than or equal to the V_{LOGIC} voltage.

RECOMMENDED OPERATING CONDITIONS

Operating Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

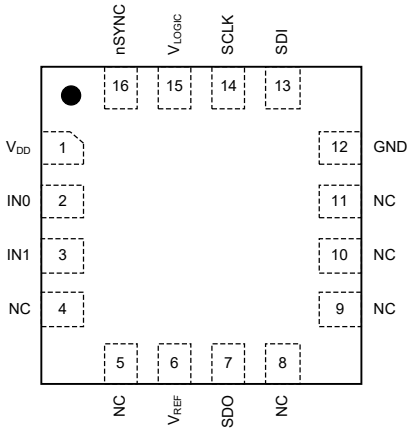
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

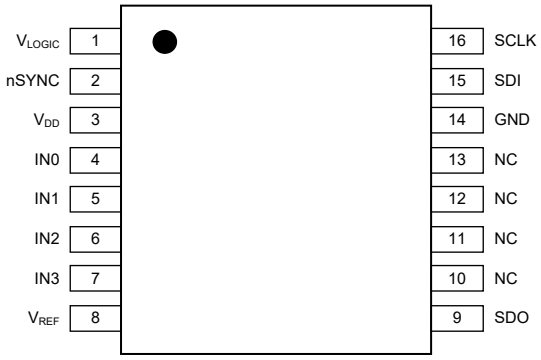
PIN CONFIGURATIONS

SGM51242R2 (TOP VIEW)



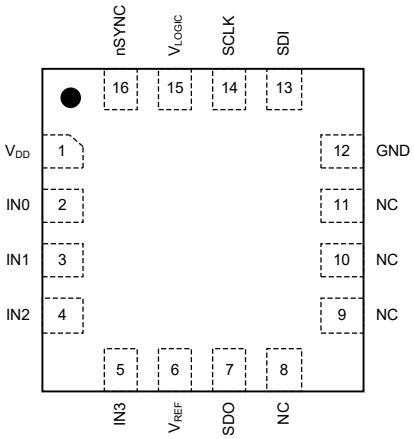
TQFN-3×3-16BL

SGM51242R4 (TOP VIEW)



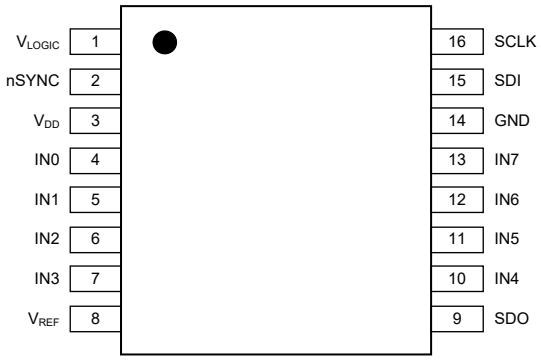
TSSOP-16

SGM51242R4 (TOP VIEW)



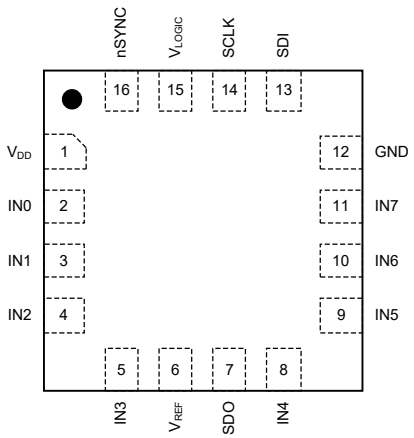
TQFN-3×3-16BL

SGM51242R8 (TOP VIEW)



TSSOP-16

SGM51242R8 (TOP VIEW)



TQFN-3×3-16BL

PIN DESCRIPTION

PIN		NAME	FUNCTION
TSSOP-16	TQFN-3×3-16BL		
1	15	V_{LOGIC}	Interface Power Supply Pin. The voltage range is from 1.7V to 5.5V.
2	16	nSYNC	Frame Synchronization Input Pin. Active low. When this pin goes low, the data frame is shifted on the falling edges of the next 16 clocks.
3	1	V_{DD}	Power Supply Pin. It can be operated from 2.7V to 5.5V. It needs a 0.1μF decoupled capacitor to GND.
4, 5, 6, 7, 10, 11, 12, 13	2, 3, 4, 5, 8, 9, 10, 11	IN0 to IN7 (1)	Analog Inputs for Channel 0 to Channel 7.
8	6	V_{REF}	Reference Input/Output Pin.
9	7	SDO	Data Output Pin. Logic output.
14	12	GND	Ground.
15	13	SDI	Data Input Pin. Logic input.
16	14	SCLK	Serial Clock Input Pin.
–	4, 5, 8, 9, 10, 11	NC	No Connection. (SGM51242R2 only)
10, 11, 12, 13	8, 9, 10, 11		No Connection. (SGM51242R4 only)

NOTE:
1. The SGM51242R2 has IN0 and IN1 pins, the SGM51242R4 has IN0 to IN3 pins, and the SGM51242R8 has IN0 to IN7 pins.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 2.7V to 5.5V, V_{REF} = 2.5V (internal), T_A = -40℃ to +125℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADC Performance (f_{IN} = 1kHz Sine Wave)						
Resolution				12		Bits
Input Range			0		V_{REF}	V
			0		2 × V_{REF}	
Integral Nonlinearity	INL		-1.58		1.78	LSB
Differential Nonlinearity	DNL		-1		1	LSB
Offset Error	E_O		-11		9	mV
Gain Error	E_G		-0.19		0.24	%FSR
Throughput Rate (2)					250	kSPS
Track Time (2)	t_{TRACK}		500			ns
Conversion Time (2)	t_{CONV}				2	μs
Signal-to-Noise Ratio	SNR	V_{DD} = 2.7V, input range = 0V to V_{REF}		70		dB
		V_{DD} = 3.3V, input range = 0V to V_{REF}		69		
		V_{DD} = 5.5V, input range = 0V to 2 × V_{REF}		68		
Signal-to-Noise + Distortion	SINAD	V_{DD} = 2.7V, input range = 0V to V_{REF}		70		dB
		V_{DD} = 3.3V, input range = 0V to V_{REF}		69		
		V_{DD} = 5.5V, input range = 0V to 2 × V_{REF}		68		
Total Harmonic Distortion	THD	V_{DD} = 2.7V, input range = 0V to V_{REF}		-95		dB
		V_{DD} = 3.3V, input range = 0V to V_{REF}		-92		
		V_{DD} = 5.5V, input range = 0V to 2 × V_{REF}		-88		
Spurious Free Dynamic Range	SFDR	V_{DD} = 2.7V, input range = 0V to V_{REF}		96		dB
		V_{DD} = 3.3V, input range = 0V to V_{REF}		92		
		V_{DD} = 5.5V, input range = 0V to 2 × V_{REF}		88		
Channel-to-Channel Isolation		f_{IN} = 1kHz		-95		dB
Input Capacitance (2)				25		pF
Full Power Bandwidth		At -3dB		22		MHz
		At -0.1dB		3		
Reference Output						
V_{REF} Output Voltage		At ambient	2.484	2.5	2.516	V
		Factory precision	2.498	2.5	2.502	
V_{REF} Temperature Coefficient				10		ppm/℃
Capacitive Load Stability		R_L = 2kΩ		5		μF
Output Impedance (2)		V_{DD} = 2.7V		0.15		Ω
		V_{DD} = 5V		0.25		Ω
Output Voltage Noise		0.1Hz to 10Hz		25		μVp-p
Output Voltage Noise Density		At ambient, f = 1kHz, C_L = 1μF		210		nV/√Hz
Output Current Load Capability		V_{DD} ≥ 3V		±5		mA

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 2.7V to 5.5V, V_{REF} = 2.5V (internal), T_A = -40℃ to +125℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Logic Input							
High Input Voltage	V_{INH}			0.7 × V_{LOGIC}			V
Low Input Voltage	V_{INL}					0.3 × V_{LOGIC}	V
Input Current	I_{IN}				±1		μA
Input Capacitance (2)	C_{IN}				10		pF
Logic Output (SDO)							
Output High Voltage	V_{OH}	I_{SOURCE} = 200μA	V_{DD} = 2.7V, V_{LOGIC} = 1.7V	1.5			V
			V_{DD} = 5.5V, V_{LOGIC} = 5.5V	5.3			
Output Low Voltage	V_{OL}	I_{SINK} = 200μA	V_{DD} = 2.7V, V_{LOGIC} = 1.7V			0.4	V
			V_{DD} = 5.5V, V_{LOGIC} = 5.5V			0.4	
Floating-State Output Capacitance (2)					10		pF
Temperature Sensor (2)							
Resolution					12		Bits
Operating Temperature Range				-40		125	℃
Accuracy					±3		℃
Track Time (2)	t_{TRACK}	ADC buffer enabled			2		μs
		ADC buffer disabled			2		
Supply Monitor Accuracy					0.5		%
Power Requirements							
Analog Supply Voltage	V_{DD}			2.7		5.5	V
Analog Supply Current	I_{DD}	Internal reference on, ADC auxiliary buffer on				3.5	mA
		Power-down mode				340	μA
		Normal mode	V_{DD} = 5V, gain = 2, internal reference		1.94		mA
			V_{DD} = 5V, gain = 2, external reference		1.75		
			V_{DD} = 3V, gain = 1, internal reference		1.7		
			V_{DD} = 3V, gain = 1, external reference		1.56		
Digital I/O Supply Voltage	V_{LOGIC}			1.7		V_{DD}	V
Digital I/O Supply Current	I_{LOGIC}					11	μA

NOTES:

1. All specifications are tested with an input signal at 0.5dB below full-scale, unless otherwise noted. All available input ranges are described in full-scale input range (FSR), but not performance guaranteed.
2. Guaranteed by design and characterization. Not production tested.

TIMING CHARACTERISTICS

(All input signals are specified with $t_R = t_F$ = 5ns (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$, T_A = -40℃ to +125℃, unless otherwise noted.) (1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SCLK Cycle Time	t_1	Write operation	1.7V ≤ V_{LOGIC} < 3V	33			ns
			3V ≤ V_{LOGIC} ≤ 5.5V	20			
		Read operation	1.7V ≤ V_{LOGIC} < 3V	65			
			3V ≤ V_{LOGIC} ≤ 5.5V	50			
SCLK High Time	t_2	1.7V ≤ V_{LOGIC} < 3V		16			ns
		3V ≤ V_{LOGIC} ≤ 5.5V		10			
SCLK Low Time	t_3	1.7V ≤ V_{LOGIC} < 3V		16			ns
		3V ≤ V_{LOGIC} ≤ 5.5V		10			
nSYNC Falling Edge to SCLK Falling Edge Setup Time (2)	t_4	1.7V ≤ V_{LOGIC} < 3V		1.7			μs
		3V ≤ V_{LOGIC} ≤ 5.5V		1.7			
Data Setup Time	t_5	1.7V ≤ V_{LOGIC} < 3V		7			ns
		3V ≤ V_{LOGIC} ≤ 5.5V		7			
Data Hold Time	t_6	1.7V ≤ V_{LOGIC} < 3V		5			ns
		3V ≤ V_{LOGIC} ≤ 5.5V		5			
SCLK Falling Edge to nSYNC Rising Edge	t_7	1.7V ≤ V_{LOGIC} < 3V		15			ns
		3V ≤ V_{LOGIC} ≤ 5.5V		10			
Minimum nSYNC High Time for Register Write Operation	t_8	1.7V ≤ V_{LOGIC} < 3V		30			ns
		3V ≤ V_{LOGIC} ≤ 5.5V		30			
Minimum nSYNC High Time for Register Read Operation		1.7V ≤ V_{LOGIC} < 3V		60			ns
		3V ≤ V_{LOGIC} ≤ 5.5V		60			
SCLK Rising Edge to SDO Valid	t_9	1.7V ≤ V_{LOGIC} < 3V				56	ns
		3V ≤ V_{LOGIC} ≤ 5.5V				25	

NOTES:

1. Guaranteed by design and characterization. Not production tested.

2. For high-speed applications, the SGM51242R2/SGM51242R4/SGM51242R8 support the minimum t_4 value of 30ns. In this case, the ADC maximum throughput rate can be up to 400kSPS, and the typical SNR is 60dB. The 400kSPS throughput rate and 60dB SNR are guaranteed only by the characteristic test results with limited samples. For the best ADC performance, t_4 > 1.7μs and t_8 > 500ns are required. Otherwise, t_4 > 30ns and t_8 > 500ns are required for reading ADC, t_4 > 30ns and t_8 > 60ns are required for reading registers, and t_4 > 30ns and t_8 > 30ns are required for writing registers.

TIMING DIAGRAM

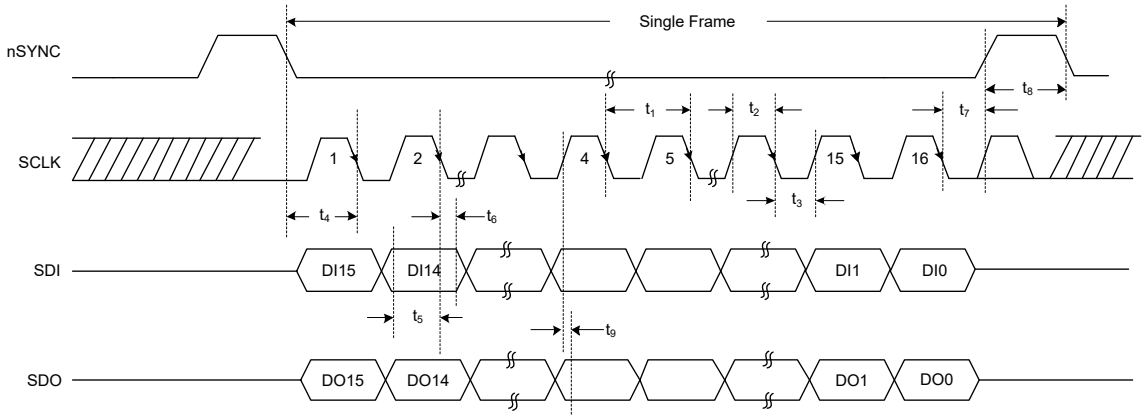
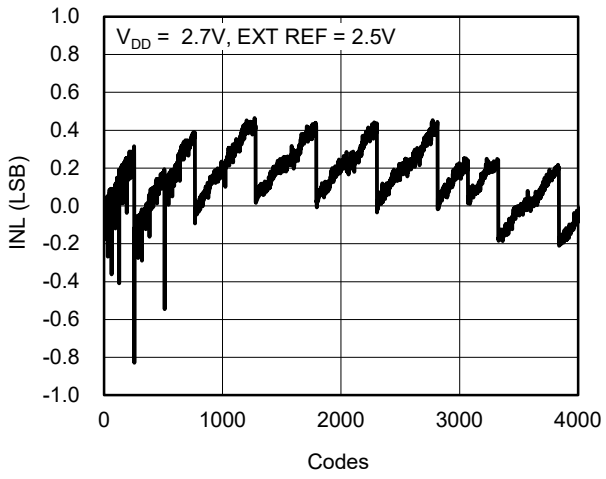


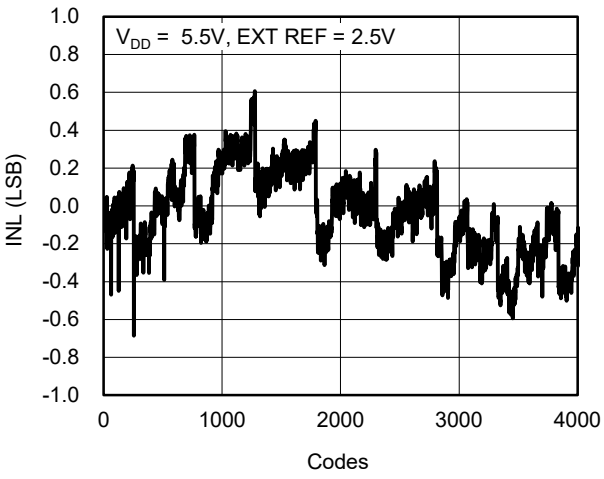
Figure 1. Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

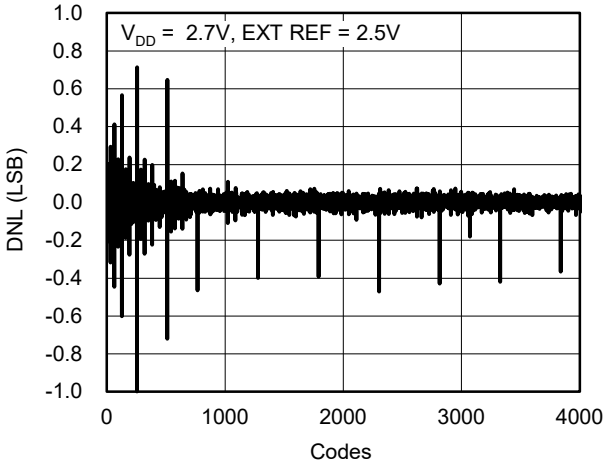
INL (V_{DD} = 2.7V)



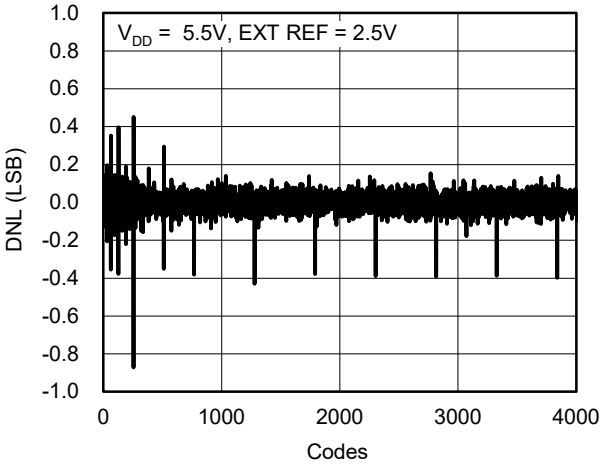
INL (V_{DD} = 5.5V)



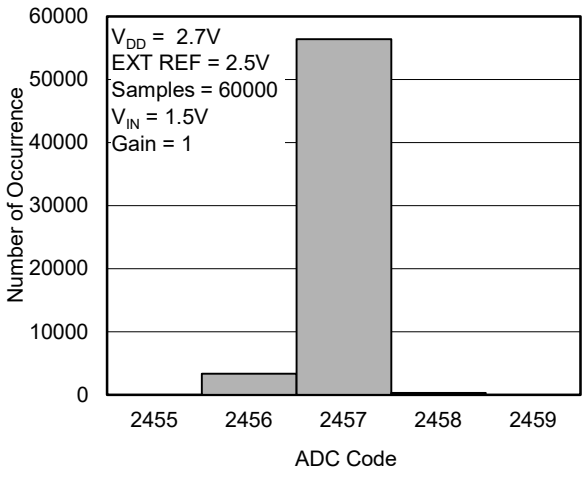
DNL (V_{DD} = 2.7V)



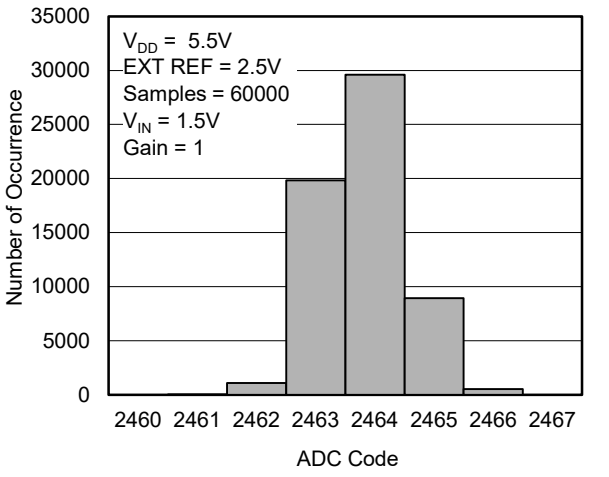
DNL (V_{DD} = 5.5V)



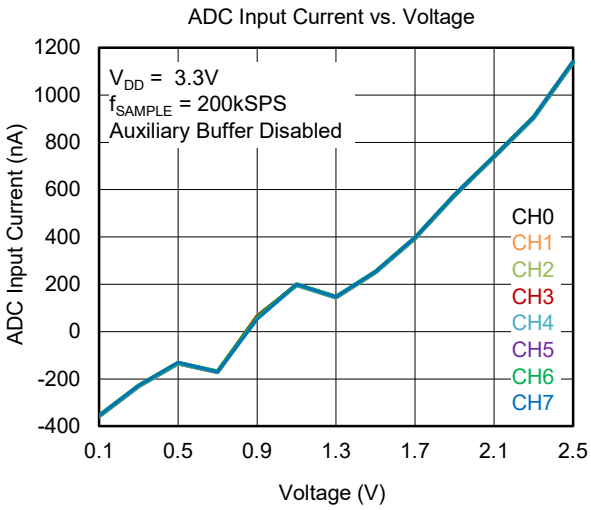
Histogram of ADC Codes (V_{DD} = 2.7V)

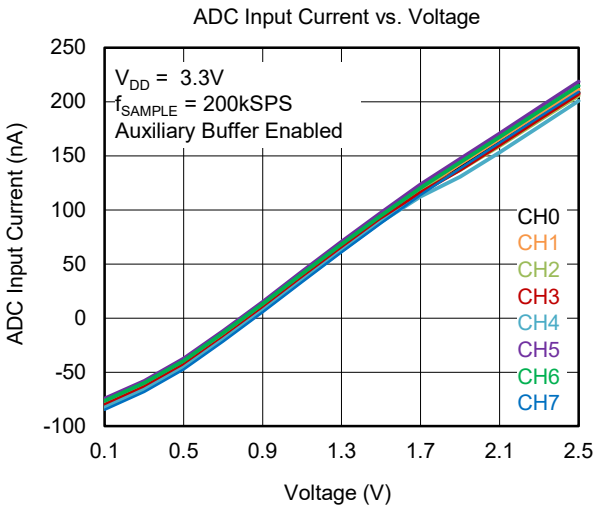


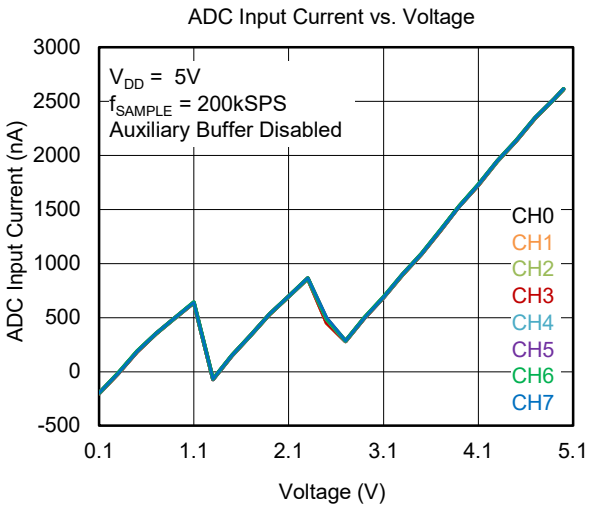
Histogram of ADC Codes (V_{DD} = 5.5V)

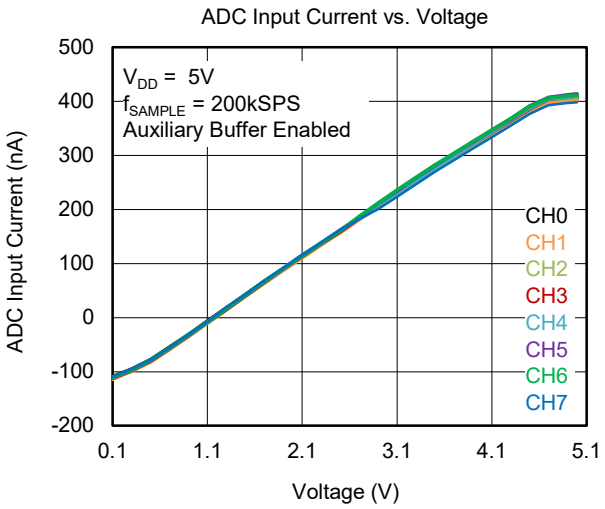


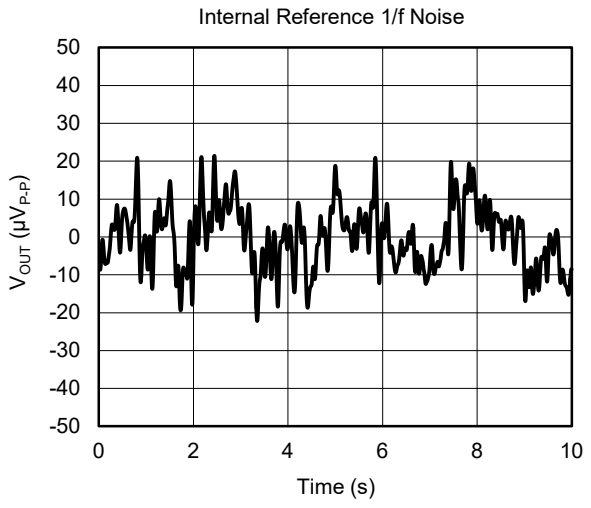
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

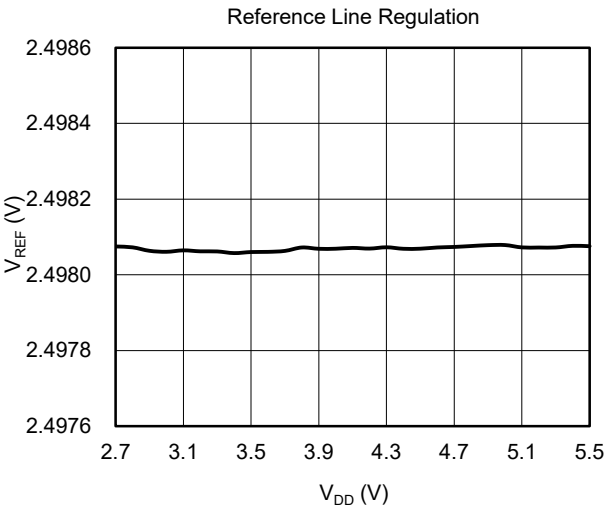






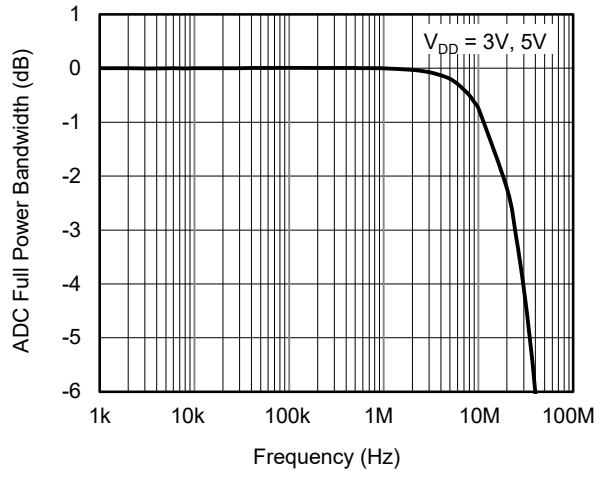




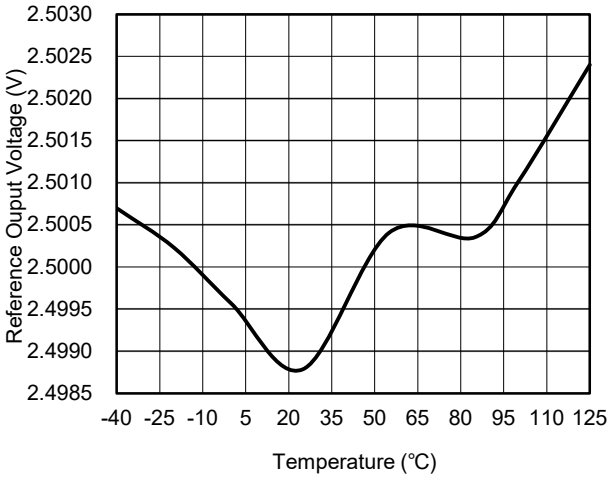


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

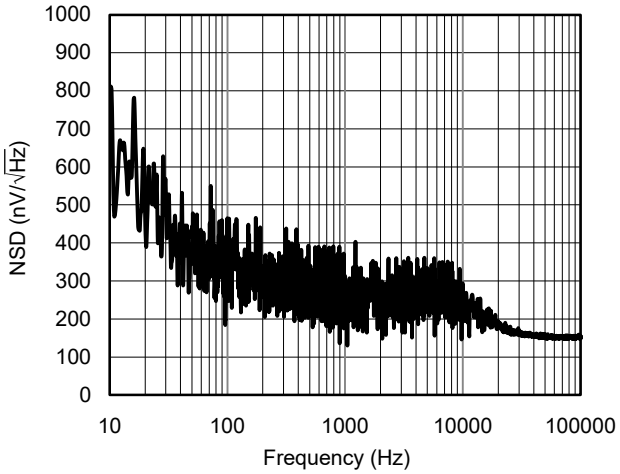
ADC Full Power Bandwidth vs. Frequency



Reference Output Voltage vs. Temperature



Reference Noise Spectral Density (NSD)



FUNCTIONAL BLOCK DIAGRAM

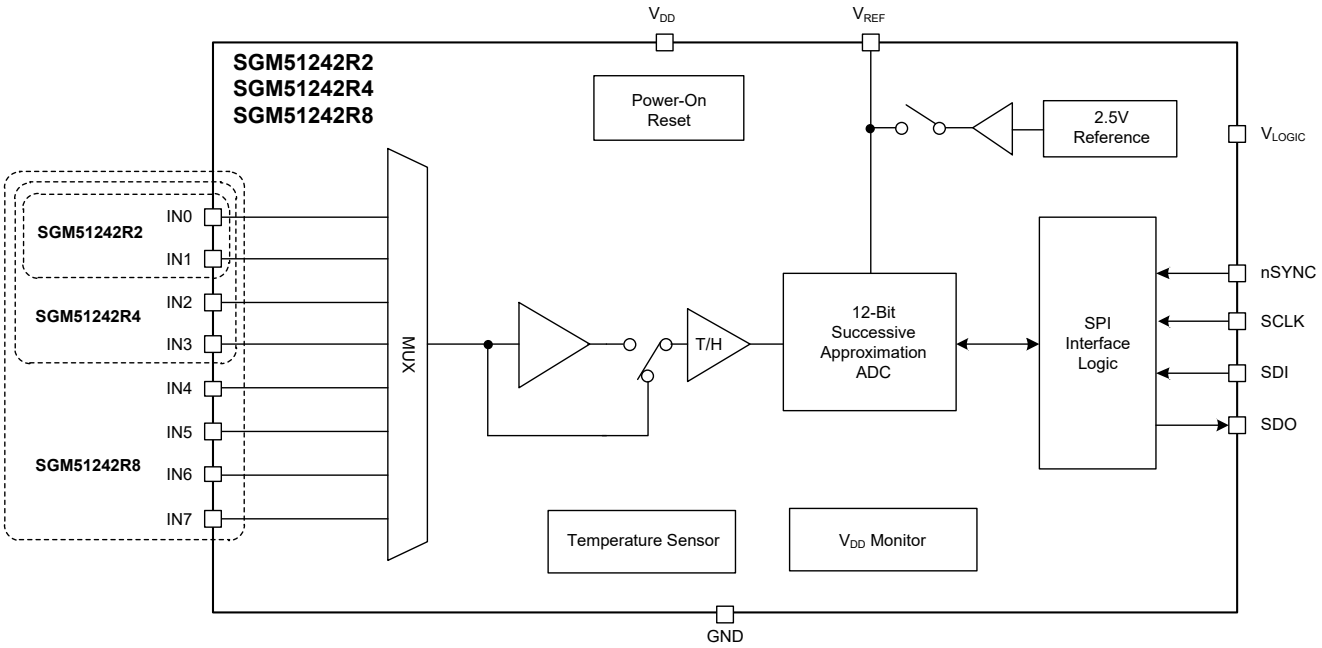


Figure 2. Block Diagram

DETAILED DESCRIPTION

The SGM51242R2, SGM51242R4, and SGM51242R8 are the 12-bit ADCs. The function of each pin is determined by programming the ADC configuration registers appropriately. See the Configuring the SGM51242R2/SGM51242R4/SGM51242R8 section and Table 3 for more information.

ADC Section

The device works as a multi-channel ADC, it works as same as a traditional multi-channel ADC with a multiplexer switching the inputs. The input channels are selected by setting the ADC sequence register. The sequencer switches the multiplexer to the next selected channel in ascending sequence automatically. Once the ADC sequence register setting is completed, the sequencer switches to the first selected channel and keeps in track mode. The first falling edge of nSYNC in the following operation frame stops the current sampling section and begins the conversion of the current channel, and the sequencer switches to the next selected channel and keeps in track mode. The nSYNC falling edge of the next operation frame starts the second channel conversion and clocks the first channel ADC result out.

The ADC conversion result is in 16-bit format, please refer to Table 1.

The ADC is a fast, 12-bit, unipolar power supply, SAR ADC. Each conversion takes 2μs. The ADC input range can be configured as 0V to V_{REF} or 0V to 2 × V_{REF}. All ADC channels share the same input range. The ADC input range is set by bit D5 in the ADC control register (refer to Table 4). The ADC output code is straight binary format.

Internal Reference

The SGM51242R2, SGM51242R4, and SGM51242R8 have an on-chip 2.5V reference, which is powered off by default when the chip is powered up. To enable the internal reference, the bit D9 is set in the power-down and reference control register (refer to Table 8).

Temperature Sensor

The SGM51242R2, SGM51242R4, and SGM51242R8 have an integrated temperature sensor that can be used to estimate the temperature of die. The temperature conversion time is about 1μs, no matter auxiliary buffer is enabled or not. To enable the temperature sampling, set the bit D8 in the ADC sequence register (refer to Table 6). The temperature result data is in address of 0b1000.

Calculation of the temperature is shown below:

When ADC gain = 1:

$$\text{Temperature}(℃) = 25 + \frac{(\text{ADC Code} - (0.56/V_{REF}) \times 4095)}{(3.015 \times (2.5/V_{REF}))} \quad (1)$$

When ADC gain = 2:

$$\text{Temperature}(℃) = 25 + \frac{(\text{ADC Code} - (0.56/(2 \times V_{REF})) \times 4095)}{(1.508 \times (2.5/V_{REF}))} \quad (2)$$

The codes range returned by the ADC is approximately 721 to 1219, and its temperature range is from -40℃ to +125℃.

Serial Interface

The SGM51242R2, SGM51242R4, and SGM51242R8 have an SPI-compatible interface. Please refer to Table 2 for the input shift register in 16-bit format. The most significant bit (MSB) D15 must be '0'. The means of each bit is shown in Table 2.

Table 3 lists the control registers map, which allows all the input pins to be configured and ADC channels to be included in sampling sequences.

Table 1. ADC Conversion Format

MSB LSB

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	ADC Address			12-Bit ADC Data											

Table 2. Input Shift Register Format

MSB LSB

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	Control Register Address				0	0	Control Register Data								

DETAILED DESCRIPTION (continued)

Table 3. Control Register Maps

MSB (D15)	Address (D[14:11])	Register Name	Description	Default Value
0	0000	NOP	No operation	0x000
0	0010	ADC Sequence Register	Select ADC channels for conversion	0x000
0	0011	ADC Control Register	ADC control register	0x000
0	0100	ADC Pin Configuration Register	Configure pins working as ADC inputs	0x000
0	0110	Pull-Down Configuration Register	Configure pins with a 85kΩ pull-down resistor to GND	0x0FF
0	0111	Readback Mode Register	Select read back configuration register	0x000
0	1011	Power-Down and Reference Control Register	Power down the selected channels and the internal reference	0x000
0	1111	Software Reset Register	Reset the chip	0x000
1	XXXX (1)	Reserved	Reserved	

NOTE:
1. D[14:11] is the control register address (see Table 2).

Power-Up Time

After the power supply is powered on, it will take SGM51242R2/SGM51242R4/SGM51242R8 about 250μs to initial the internal circuit blocks and load the registers with the default values. Any operation during this time is restricted.

Write Mode

Figure 1 shows the read and write timing for the device. A falling edge of nSYNC starts a write frame. Data is locked on the falling edge of SCLK. After 16 falling edges of SCLK, all 16-bit data is shifted in. Then nSYNC can be pulled high.

Read Mode

The SGM51242R2, SGM51242R4, and SGM51242R8 support both ADC conversion data read and the register data read. During the normal operation, the ADC conversion result automatically is shifted out a part of a sequence. Reading a register needs the following steps. First issue a write frame to the readback mode register to select the register to read out. The second step is that issue a 16 SCLKs operating frame, and the data in the selected register is shifted out.

Configuring the SGM51242R2/SGM51242R4/SGM51242R8

The SGM51242R2/SGM51242R4/SGM51242R8 input pins are software configurable. The control registers are listed in Table 3.

After the chip is powered up, all input pins are pulled down to GND by 85kΩ resistors by default. A command 0x00 to address 0b0110 can disable the pull-down resistor.

DETAILED DESCRIPTION (continued)

ADC Control Register

The ADC control register can configure the ADC buffer, ADC input range and ADC input pre-charge function. More details please refer to Table 4.

ADC Operation

The SGM51242R2, SGM51242R4, and SGM51242R8 are the traditional multi-channel ADCs which are composed of a multiplexer and one ADC core. Each nSYNC operation frame gives out previous channel conversion result and initiates the next conversion.

The ADC converts all selected channels in ascending order. The input channels are enabled in ADC sequence register. If REP bit in the ADC sequence register is set, once ADC finishes all selected channels, it will repeat the sequence. If REP bit is not set, once ADC finished all selected channels, it goes to 3-state.

The typical operating sequences of the SGM51242R2/SGM51242R4/SGM51242R8 are shown in Figure 3 to Figure 6. The ADC conversion result data format is shown in Table 7.

Changing an ADC Sequence

To start a new sequence setting, the current ADC sequence needs to be stopped first. Clearing REP, TEMP and ADC0 to ADC7 bits in the ADC sequence register can stop the ADC conversion sequence. The stop command cannot stop the on-going conversion. A new setting cannot be started until the current conversion is completed. A minimum 2μs is required between a new setting and the end of current conversion. After the new sequence setting command, it will take the ADC at least 500ns to sample before starting the next conversion.

Table 4. ADC Control Register Details

BITS	BIT NAME	DESCRIPTION	DEFAULT VALUE
D[15]	MSB	Must be set to 0.	0
D[14:11]	Register Address[3:0]	Set these bits to 0011.	0011
D[10]	Reserved	Reserved. Must be set to 0.	0
D[9]	ADC Auxiliary Buffer Configuration	0 = ADC auxiliary buffer disabled (default) 1 = ADC auxiliary buffer enabled	0
D[8]	Reserved	Reserved. Must be set to 0.	0
D[7]	Lock	Lock Configuration 0 = The contents configuration registers can be changed (default) 1 = The contents configuration registers are locked	0
D[6]	Reserved	Reserved. Set these bits to 0.	0
D[5]	ADC Range	ADC Input Range Setting 0 = Set the ADC range 0V to V_{REF} (default) 1 = Set the ADC range 0V to 2 × V_{REF}	0
D[4:0]	Reserved	Reserved. Must set these bits to 0.	0 0000

Table 5. ADC Pin Configuration Register Details

BITS	BIT NAME	DESCRIPTION	DEFAULT VALUE
D[15]	MSB	Set this bit to 0.	0
D[14:11]	Register Address[3:0]	Set these bits to 0100.	0100
D[10:8]	Reserved	Reserved. Set these bits to 0.	000
D[7:0]	ADC[7:0]	Select INx Pins as ADC Inputs 0 = INx is not an ADC input (default) 1 = INx is an ADC input	0000 0000

DETAILED DESCRIPTION (continued)

Table 6. ADC Sequence Register Details

BITS	BIT NAME	DESCRIPTION	DEFAULT VALUE
D[15]	MSB	Set this bit to 0.	0
D[14:11]	Register Address[3:0]	Set these bits to 0010.	0010
D[10]	V_{DD} Monitor	Include V_{DD} Monitor in ADC Sequence 0 = Disable V_{DD} monitor readback (default) 1 = Enable V_{DD} monitor readback	0
D[9]	REP	ADC Sequence Repetition 0 = Sequence repetition disabled (default) 1 = Sequence repetition enabled	0
D[8]	TEMP	Include Temperature Sensor Sampling in ADC Sequence 0 = Disable temperature sensor readback (default) 1 = Enable temperature sensor readback	0
D[7:0]	ADC[7:0]	Select Corresponding ADC Channels in Conversion Sequence 0 = The selected ADC channel is not included in the conversion sequence (default) 1 = Include the selected ADC channel in the conversion sequence	0000 0000

Table 7. ADC Data Register Format

MSB **LSB**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	ADC Address (1)			12-Bit ADC Data											
1	000 (2)			12-Bit Temperature Sensor Channel Data											
1	001 (3)			12-Bit V_{DD} Monitor Channel Data											

NOTES:
1. When D[15] = 0, the ADC addresses are as follows: 000 = ADC0, …, 111 = ADC7.
2. When D[15:12] = 1000, ADC result is internal temperature sensor sampling data.
3. When D[15:12] = 1001, V_{DD} monitor channel sends V_{DD}/4 into the ADC. For example, if V_{DD} = 5V, this channel result of ADC will be 1.25V.

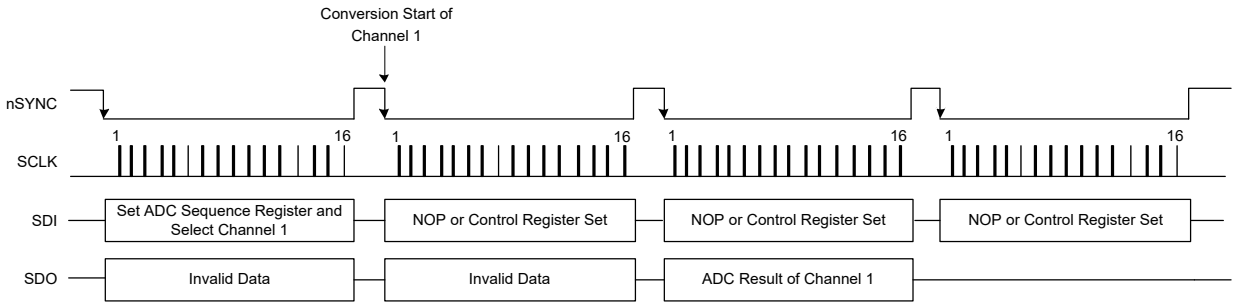


Figure 3. Single-Channel, No Repeat, ADC Conversion Sequence

DETAILED DESCRIPTION (continued)

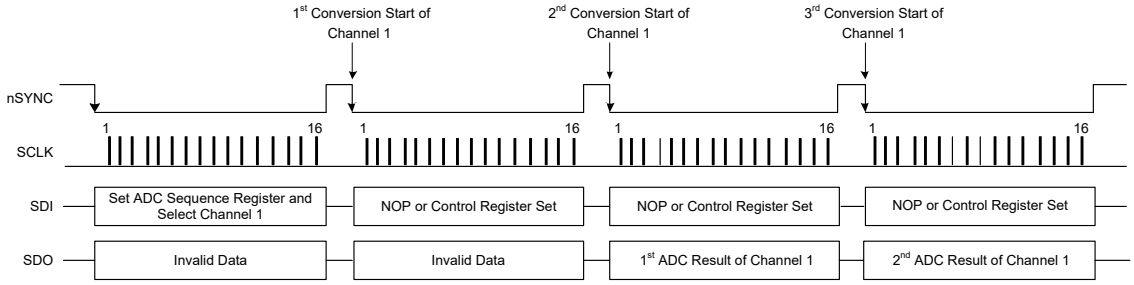


Figure 4. Single-Channel, Repeating, ADC Conversion Sequence

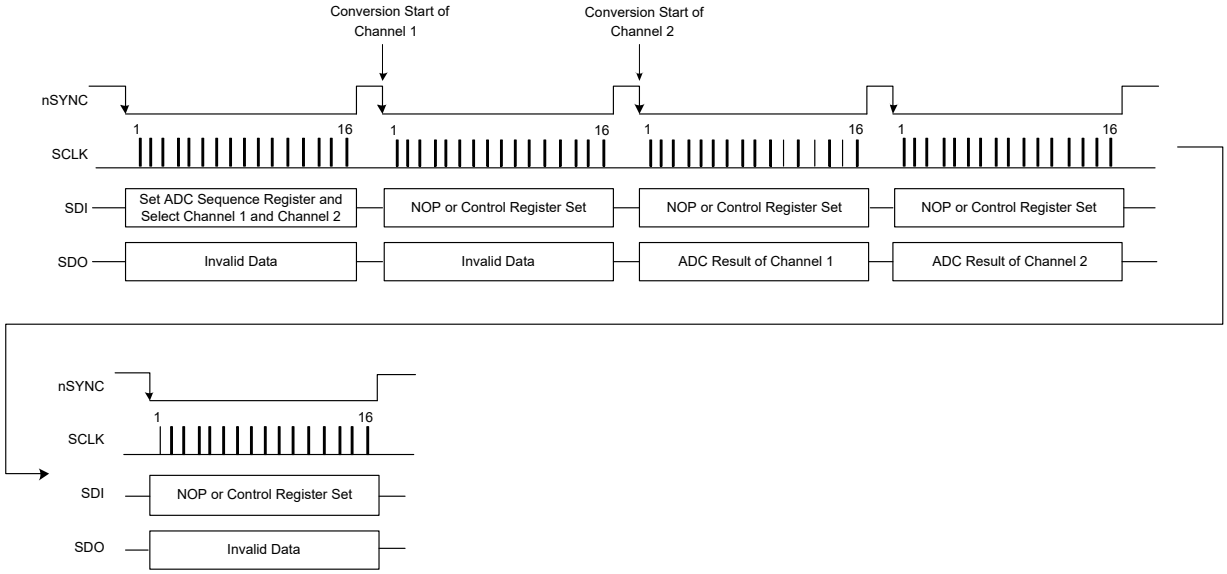


Figure 5. Multi-Channel, No Repeat, ADC Conversion Sequence

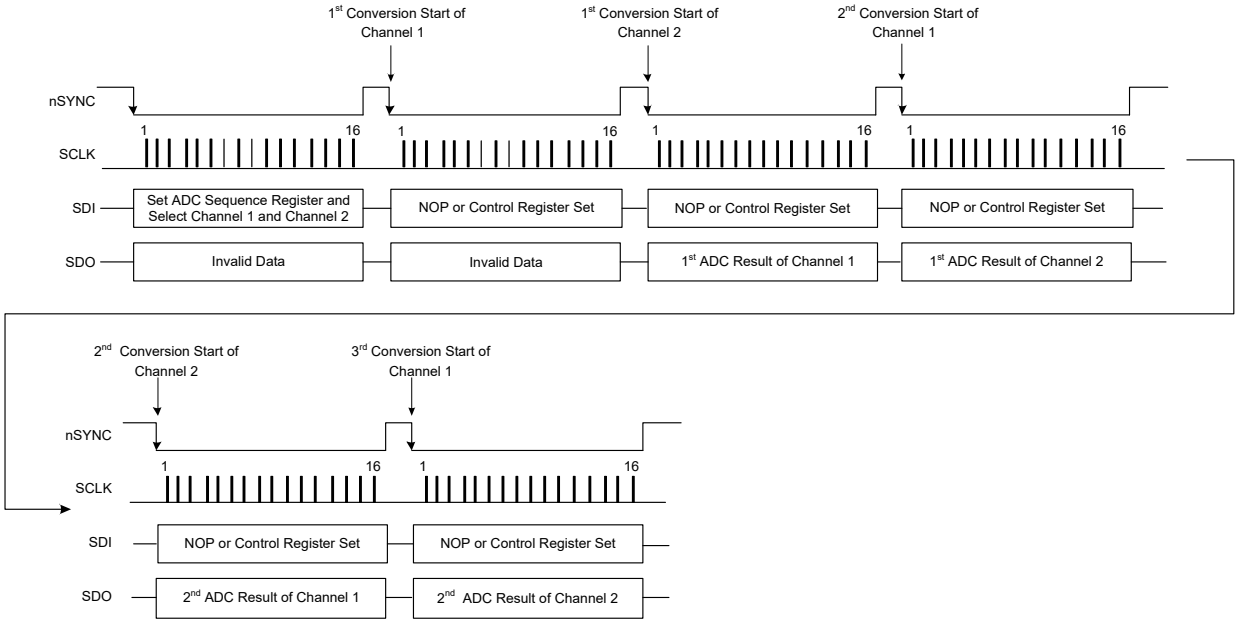


Figure 6. Multi-Channel, Repeating, ADC Conversion Sequence

DETAILED DESCRIPTION (continued)

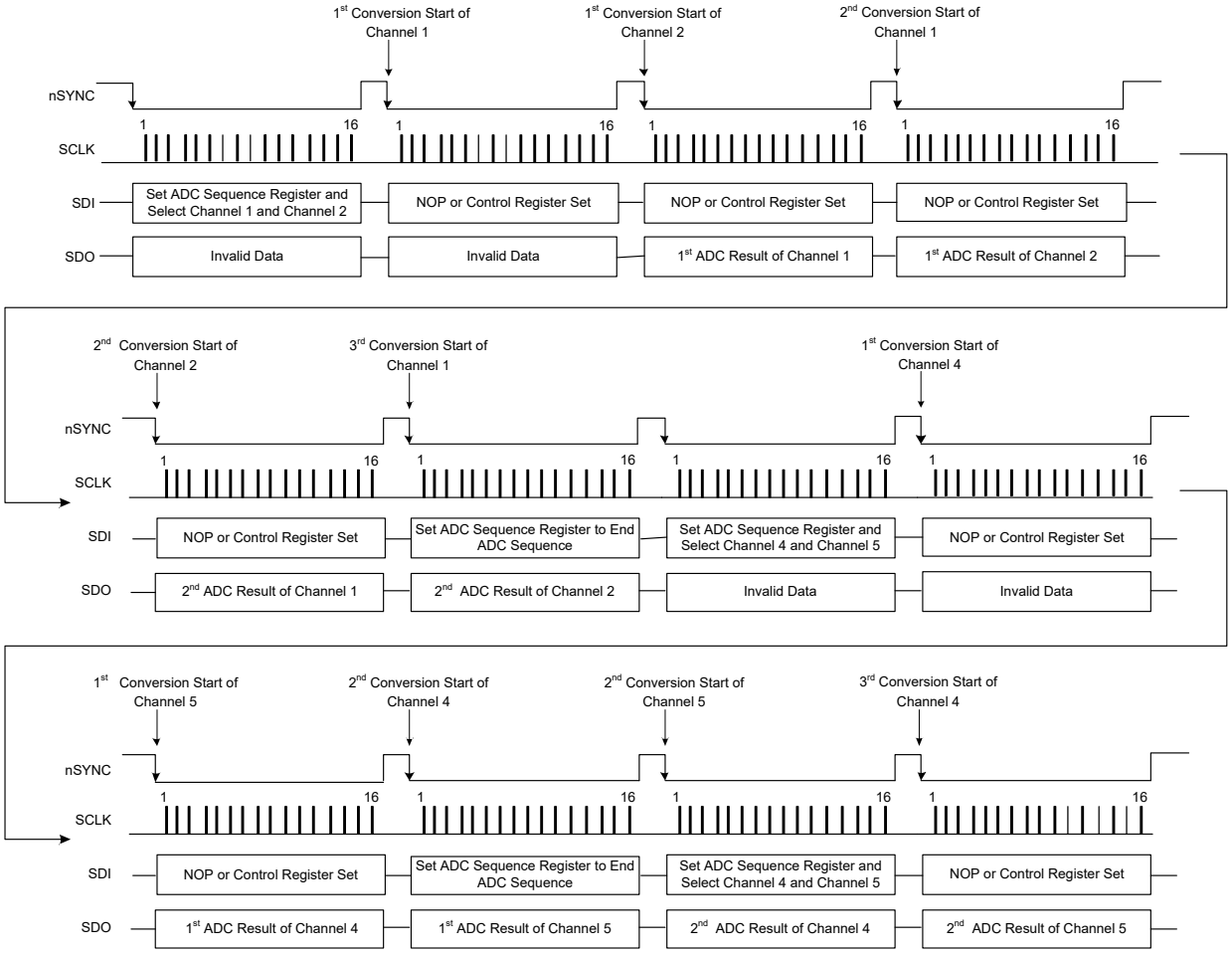


Figure 7. Changing a Multi-Channel, Repeating, ADC Conversion Sequence

DETAILED DESCRIPTION (continued)

Power-Down and Reference Control

The internal reference of the chip is powered down by default when the chip is powered up. If none of the input channels are enabled as ADCs, the chip is automatically powered down. More details are shown in Table 8.

Reset Function

The SGM51242R2, SGM51242R4, and SGM51242R8 support software reset (refer to Table 9). The reset command will reset all registers to the default values and reset all input pins to their default conditions. It will take the chip 250μs to complete the reset process. It is not recommended to do any operation during this time.

Readback Mode Register

The SGM51242R2, SGM51242R4, and SGM51242R8 support the register readback function. It needs to be enabled by setting bit D6 in readback mode register before performing a register readback. Bits D[5:2] are used to select the address of the register to be read back. After the first enable and register selected data frame, then the data of the selected register is shifted out in the next data frame. More details are shown in Table 10.

Table 8. Power-Down and Reference Control Register Details

BITS	BIT NAME	DESCRIPTION	DEFAULT VALUE
D[15]	MSB	Set this bit to 0.	0
D[14:11]	Register Address[3:0]	Set these bits to 1011.	1011
D[10]	PD_ALL	Power-Down Internal Reference 0 = The reference states depend on D9 bit (default) 1 = The reference and ADC are powered down	0
D[9]	EN_REF	Enable Internal Reference 0 = The reference and its buffer are powered down. Set this bit if an external reference is used (default) 1 = The reference and its buffer are powered up. The reference is available on the V_{REF} pin	0
D[8:0]	Reserved	Reserved. Set these bits to 0.	0 0000 0000

Table 9. Software Reset Register

MSB LSB

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	1	1	0	1	1	0	1	0	1	1	0	0
Control Register Write	Write to Reset Register				Reset the SGM51242R2/SGM51242R4/SGM51242R8										

Table 10. Readback Mode Register Details

BITS	BIT NAME	DESCRIPTION	DEFAULT VALUE
D[15]	MSB	Set this bit to 0.	0
D[14:11]	Register Address[3:0]	Set these bits to 0111.	0111
D[10:7]	Reserved	Reserved. Set these bits to 0.	0000
D[6]	EN	Enable Readback 0 = No readback is initiated (default) 1 = Bits D[5:2] select read back register. Bit D6 automatically clears when the read is completed	0
D[5:2]	REG_READBACK[3:0]	If bit D6 is 1, the bits D[5:2] determine which register is to be read back. 0000 = NOP (default) 0010 = ADC sequence 0011 = ADC control register configuration 0110 = Pull-down configuration 1011 = Power-down and reference control 1110 = Reserved 1111 = Software reset Others = Reserved	0000
D[1:0]	Reserved	Reserved	00

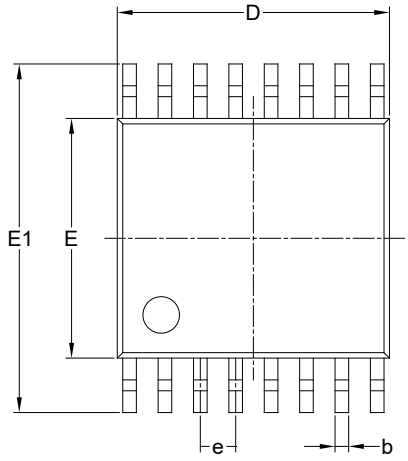
REVISION HISTORY

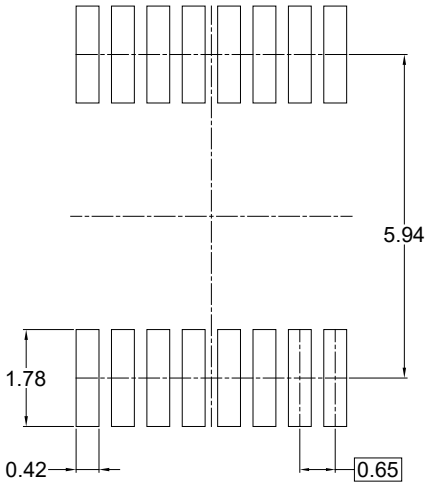
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (NOVEMBER 2023) to REV.A	Page
Changed from product preview to production data	All

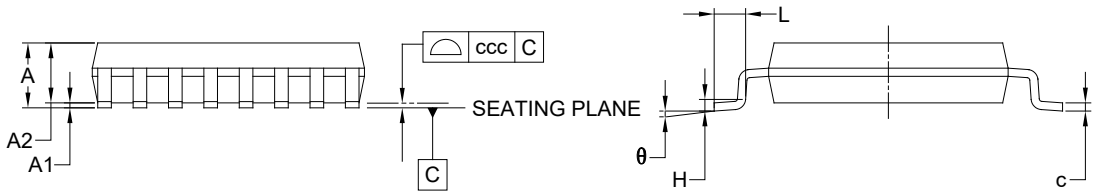
PACKAGE OUTLINE DIMENSIONS

TSSOP-16





RECOMMENDED LAND PATTERN (Unit: mm)

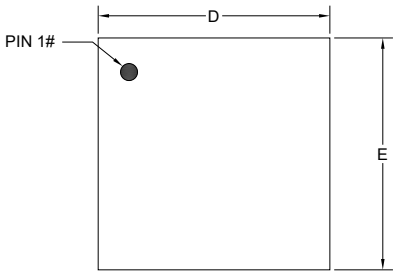


Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	-	-	1.200
A1	0.050	-	0.150
A2	0.800	-	1.050
b	0.190	-	0.300
c	0.090	-	0.200
D	4.860	-	5.100
E	4.300	-	4.500
E1	6.200	-	6.600
e	0.650 BSC		
L	0.450	-	0.750
H	0.250 TYP		
θ	0°	-	8°
ccc	0.100		

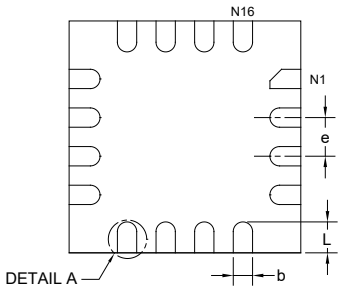
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-153.

PACKAGE OUTLINE DIMENSIONS

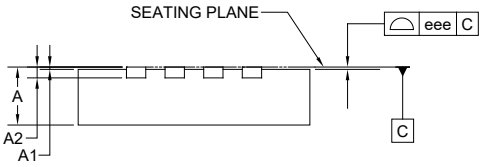
TQFN-3×3-16BL



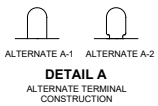
TOP VIEW



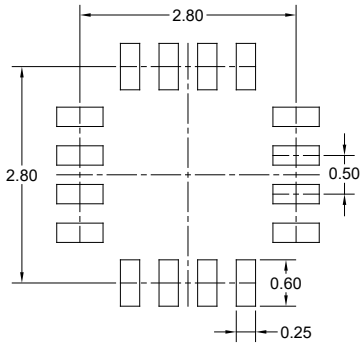
BOTTOM VIEW



SIDE VIEW



DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



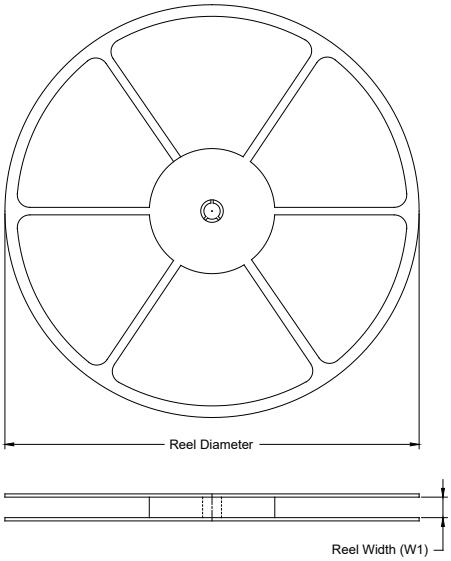
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	0.700	-	0.800
A1	-0.004	-	0.050
A2	0.110 REF		
b	0.200	-	0.300
D	2.900	-	3.100
E	2.900	-	3.100
e	0.500 BSC		
L	0.300	-	0.500
eee	0.080		

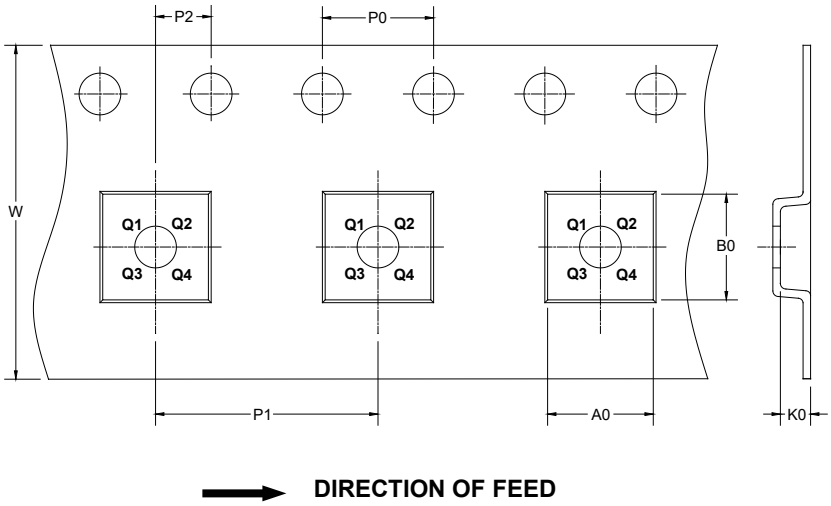
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



DIRECTION OF FEED

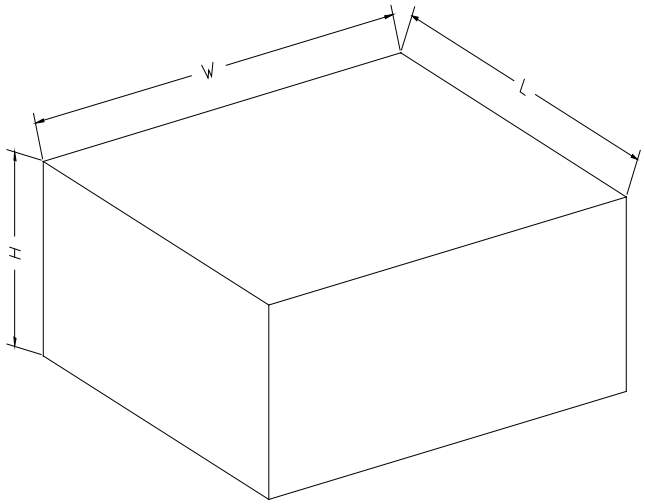
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP-16	13″	12.4	6.80	5.40	1.50	4.0	8.0	2.0	12.0	Q1
TQFN-3×3-16BL	13″	12.4	3.35	3.35	1.13	4.0	8.0	2.0	12.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002