SY7686

Integrated Power Solution For TFT LCD Panels Synchronous Boost and Synchronous Inverter Converters

General Description

The SY7686 is a high efficiency power solution for PAD panels. This device integrates a synchronous boost regulator and a synchronous inverting regulator. SY7686 works over a wide input voltage range from 2.5V to 5.5V. The 1.5MHz switching frequency minimizes the size of external components. The SY7686 also features enable on/off control, cycle-by-cycle current limit, short circuit protection and thermal shutdown.

The both converters employ peak current mode control. Output voltage of positive rail is adjustable from 4.6V to 7V.This channel can provides 0.15A output current. The Output voltage of negative rail also can be adjusted from -6V to -1.5V through FB divider resistor. This channel can provides 0.15A output current.

Ordering Information

SY7686 □(□□)□

- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY7686DCC	DFN3x3-12	--

Features

- 2.5V to 5.5V Input Voltage Range
- Synchronous Boost converter:
  - Low $R_{DS(ON)}$ for Internal Switches (P-Channel FET/N-Channel FET): 660/400mΩ
  - 150mA Output Current Capability
  - True Shutdown Output
  - 4.6V-7V Adjustable Output
  - Cycle-by-cycle Current Limiting Protection
- Synchronous Inverter Converter:
  - Low $R_{DS(ON)}$ for Internal Switches (P-Channel FET/N-Channel FET): 500/340mΩ
  - 150mA Output Current Capability
  - -6V to -1.5V Adjustable Inverting Output
  - Cycle-by-cycle Current Limiting Protection
- Internal Loop Compensation
- 1.5MHz Switch Frequency
- Low Shutdown Current <1uA
- xBuilt-in Softstart
- EN Control On/Off
- PSM Mode at Light Load for High Efficiency
- RoHS Compliant and Halogen Free
- Compact Package: DFN3x3-12

Applications

- PAD panels power driver
- Active Matrix OLED
- Mobile device

Typical Applications

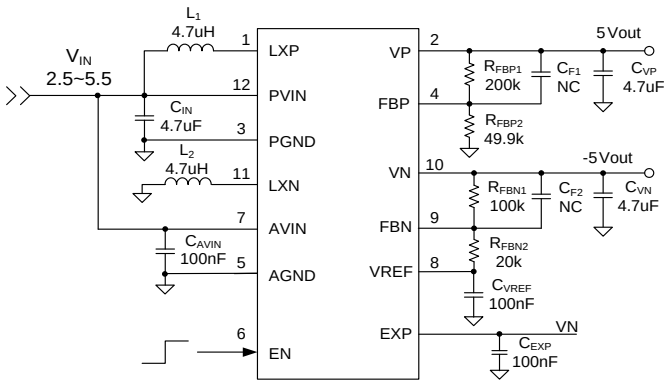
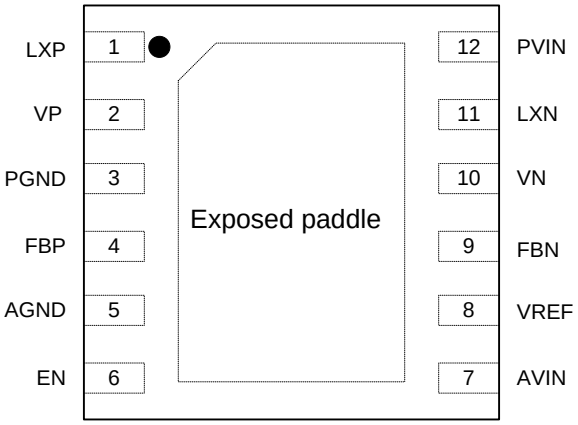


Figure1. Schematic Diagram

Pinout (top view)



(DFN3x3-12)

Top Mark: **AVO*xyz*, (**Device code: AVO, ***x=year code, y=week code, z= lot number code*****)**

Pin Name	Pin Number	Pin Description
LXP	1	Inductor pin for boost regulator. Connect this pin to the switching node of inductor.
VP	2	Boost regulator output pin. Decouple this pin to the PGND pin with at least 4.7uF ceramic capacitor.
PGND	3	Power ground pin.
FBP	4	Feedback pin for boost converter. Connect this pin to the center point of the output resistor divider to program the output voltage. The nominal voltage at this pin is at 1V when the output is regulated. VP=1+RFBP1/RFBP2
AGND	5	Analog ground pin.
EN	6	Enable control pin. Pull high to enable chip. Do not floating.
AVIN	7	Power supply input for analog circuit. Decouple this pin to PGND with at least 0.1uF ceramic capacitor
VREF	8	Reference output pin. Connect a 0.1uF Capacitor from VREF to AGND.
FBN	9	Feedback pin for inverter converter. Connect this pin to the center point of the output resistor divider to program the output voltage. The nominal voltage at this pin is at 0V when the output is regulated. VN=-(RFBP1/RFBP2)
VN	10	Inverter regulator output pin. Decouple this pin to the PGND pin with at least 4.7uF ceramic capacitor.
LXN	11	Inductor pin for inverter regulator. Connect this pin to the switching node of inductor.
PVIN	12	Power supply input for inverting regulator. Decouple this pin to PGND with at least 4.7uF ceramic capacitor.
Exposed pad		Exposed pad. Connect this pad to VN pin and connect a 0.1μF bypass capacitor between the exposed pad and ground.

Block Diagram

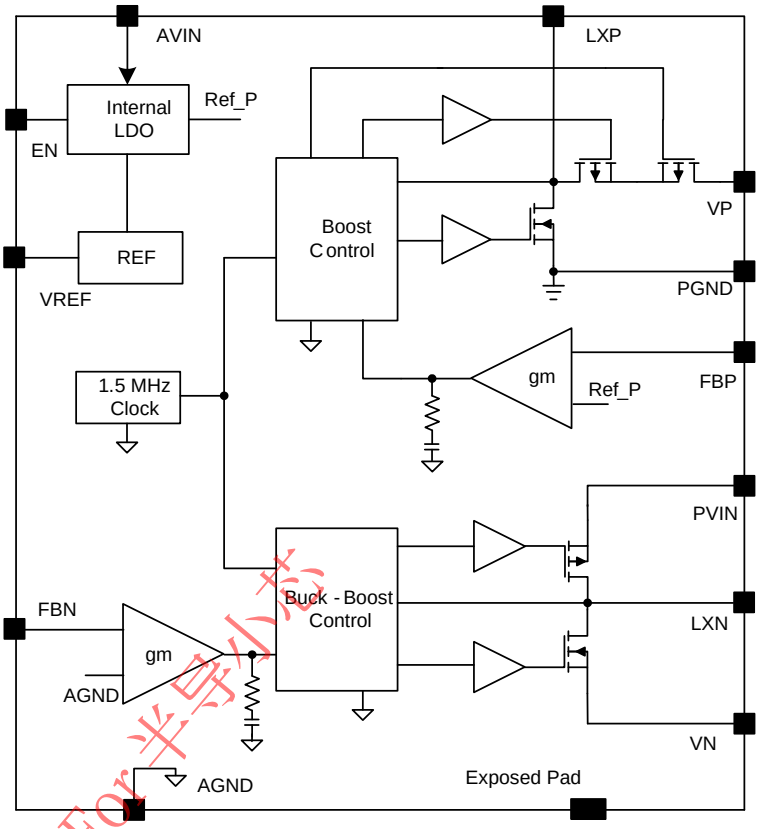


Figure2. Block Diagram

Start Up Sequence:

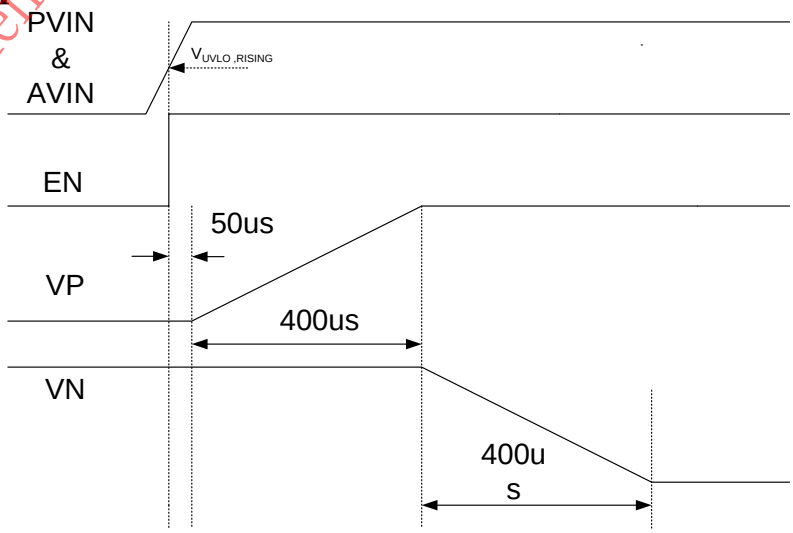


Figure3. Start Up Sequence

Absolute Maximum Ratings (Note 1)

PVIN, AVIN ---------- -0.3V to 6V
EN,FBN,FBP---------- -0.3V to PVIN+0.3V
VP---------- -0.3V to 8V
LXP---------- -0.3V to VP+0.3V
VN---------- -7V to PGND+0.3V
LXN---------- VN-0.3V to PVIN+0.3V
Power Dissipation, P_D @ T_A = 25℃ DFN3X3 ---------- 3.3W
Package Thermal Resistance (Note 2)
θ_{JA} ----------38℃/W
θ_{JC} ---------- 8℃/W
Junction Temperature Range ---------- 150℃
Lead Temperature (Soldering, 10 sec.) ---------- 260℃
Storage Temperature Range ---------- -65℃ to 150℃

Recommended Operating Conditions (Note 3)

PVIN,AVIN ---------- 2.5V to 5.5V
Junction Temperature Range ---------- -40℃ to 125℃
Ambient Temperature Range ---------- -40℃ to 85℃

Electrical Characteristics

(V_{IN} =3.6V, TA=25℃, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{PVIN}, V_{AVIN},		2.5		5.5	V
$V_{UVLO,RISING}$	$V_{UVLO,RISING}$	UVLO rising threshold voltage		2.21		V
Input UVLO Hysteresis	$V_{UVLO,HYS}$			0.12		V
Shutdown Current	I_{SHUT}	EN=0		0.01	1	μA
Switching Frequency	F_{SW}	CCM Mode	1.2	1.5	1.8	MHz
Internal Softstart Time	T_{SS}	Guaranteed by design		400		us
Enable Logic High Threshold	V_{EN_HIGH}	Rising	1.2			V
Enable Logic Low Threshold	V_{EN_LOW}	Falling			0.4	V
Thermal Shutdown Temperature	T_{SD}			160		℃
Thermal Shutdown hysteresis	T_{HYS}			20		℃
Channel 1 Synchronous Boost Converter						
Output Voltage Variation	ΔV_{VP}	V_{PVIN}=V_{AVIN}=3.7V, I_{VP} <150mA, T_J=25℃	-1		+1	%VP
FBP Regulation Voltage	V_{FBP}		0.99	1.00	1.01	V
VP Adjustable Range	$V_{VP,ADJ}$		4.6		7	V
P-Channel Power FET R_{ON}	$R_{DS(ON),P1}$			614		mΩ
N-Channel Power FET	$R_{DS(ON),N1}$			250		mΩ

R_{ON}						
Maximum Load Current	$I_{MAX, LOAD}$	V_{AVIN}=V_{PVIN}=2.9-4.5V	150			mA
NFET Peak Current Limit	$I_{LIM, PEAK}$			1.1		A
Discharge Resistor	R_{DIS}			135		Ω
PSM Mode Ripple	$V_{RIP,PSM MODE}$	V_{AVIN}=V_{PVIN}=2.9-4.5V, V_{VP} =5V,I_{VP}=1mA		12		mV
Channel 2 Synchronous Inverter Converter						
Output Voltage Variation	V_{REF} –V_{FBN}	V_{PVIN}=V_{AVIN}=3.6V, I_{VN} <150mA, T_J=25℃	0.99	1	1.01	V
FBN Regulation Voltage	V_{FBN}		-10	0	+10	mV
VN Adjustable Range	$V_{VN,ADJ}$		-6		-1.5	V
P-Channel Power FET R_{ON}	$R_{DS(ON),P2}$			570		mΩ
N-Channel Power FET R_{ON}	$R_{DS(ON),N2}$			300		mΩ
Maximum Load Current	$I_{MAX, LOAD}$	V_{AVIN}=V_{PVIN}=2.9-4.5V	150			mA
PFET Peak Current Limit	$I_{LIM, PEAK}$			1.14		A
Discharge Resistor	R_{DIS}			370		Ω
PSM Mode Ripple	$V_{RIP,PSM MODE}$	V_{AVIN}=V_{PVIN}=2.9-4.5V, V_{VN} =-5V,I_{VN}=1mA		12		mV

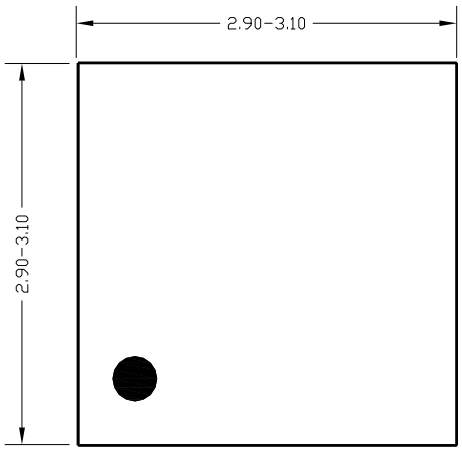
Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25℃ on a low effective 2-layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Paddle of DFN3x3 packages is the case position for θ_{JC} measurement.

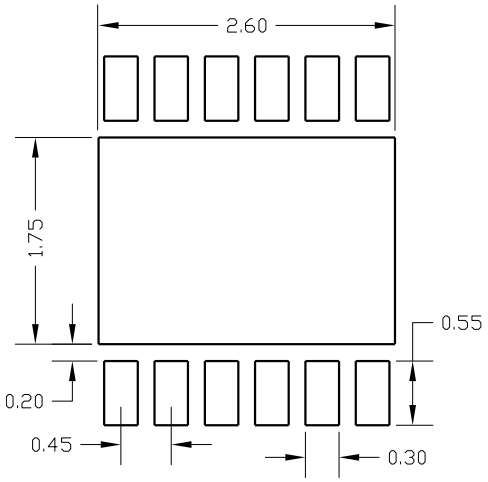
Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Performance of boost converter is not guaranteed at VP< $V_{PVIN,AVIN,}$+0.4V

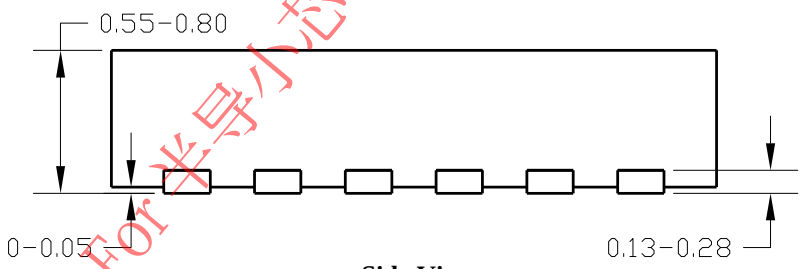
DFN3x3-12 Package Outline



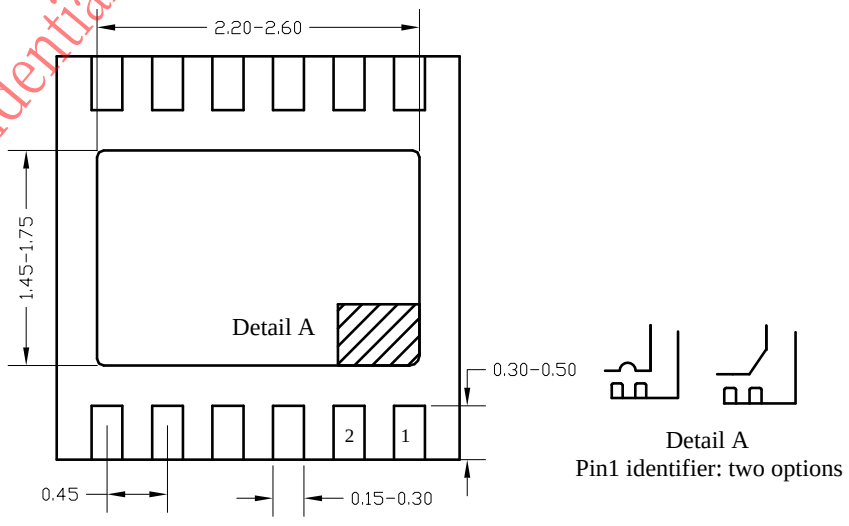
Top View



PCB layout (Recommended)



Side View

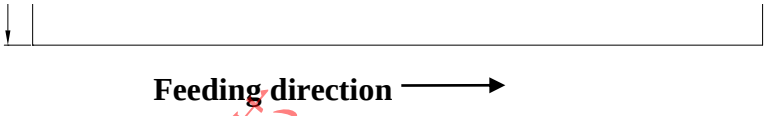


Bottom View

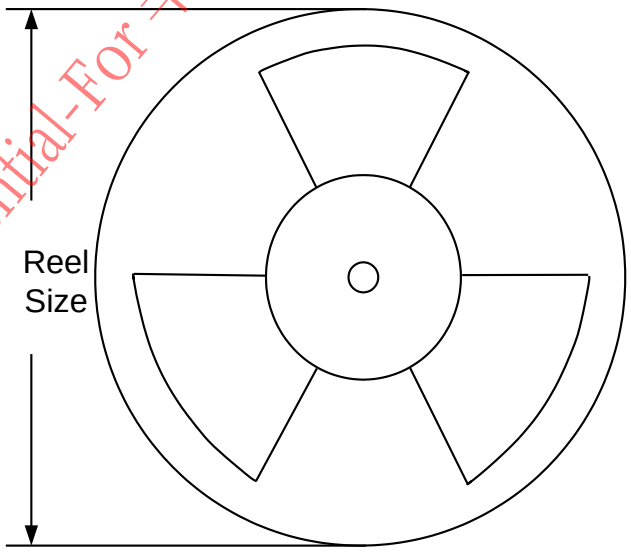
Notes: All dimensions are in millimeters and exclude mold flash & metal burr.

Taping & Reel Specification

1. DFN3x3-12 taping orientation



2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
DFN3x3	12	8	13"	400	400	5000

3. Others: NA

单击下面可查看定价，库存，交付和生命周期等信息

>>SILERGY(矽力杰)