SM80592

High Efficiency, 1.5MHz
2A Synchronous Step Down Regulator
Advanced Design Specification

General Description

The SM80592 is a high efficiency 1.5MHz synchronous step down DC/DC regulator, capable of delivering up to 2A output currents. It can operate over a wide input voltage range from 2.5V to 5.5V and integrates main switch and synchronous switch with very low $R_{DS\ (ON)}$ to minimize the conduction loss.

The SM80592 is in a space saving, low profile DFN1.3×0.9-6 package.

Ordering Information

SM80592 □(□□□)
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SM80592IHD	DFN1.3×0.9-6	--

Features

- 2.5V to 5.5V Input Voltage Range.
- Low $R_{DS(ON)}$ for Internal Switches (Top/Bottom): 125mΩ /75mΩ
- High Switching Frequency 1.5MHz Minimizes the External Components
- Internal Soft-start Limits the Inrush Current
- 100% Dropout Operation
- Power Good Indicator
- Hic-cup for Short Circuit Protection
- Output Auto Discharge Function
- RoHS Compliant and Halogen Free
- Compact Package: DFN1.3×0.9-6

Applications

- Set Top Box
- USB Dongle
- Media Player
- Smart Phone

Typical Application

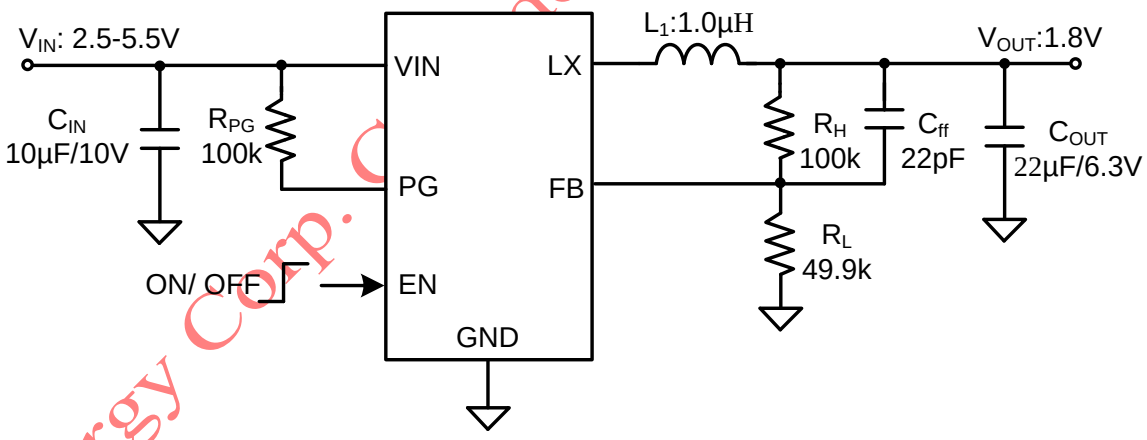
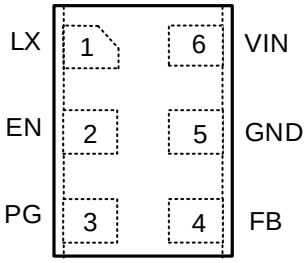


Figure1. Schematic Diagram

Pin out (Top View)



(DFN1.3×0.9-6**)**

Top Mark: 6E*xyz* (device code: 6E, ***x=year code, y=week code, z= lot number code)***

Pin Description

Pin Name	Pin Number	Pin Description
LX	1	Inductor pin. Connect this pin to the switching node of the inductor.
EN	2	Enable control. Pull high to turn on. Do not leave it floating.
PG	3	Power good indicator. Power good indicator (open drain output). Low if the output < 90% or the output >120% of regulation voltage; High otherwise. Connect a pull-up resistor to the input.
FB	4	Output feedback pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: $V_{OUT}=0.6\times(1+R_H/R_L)$.
GND	5	Ground pin.
VIN	6	Input pin. Decouple this pin to the GND pin with at least a 10μF ceramic capacitor.

Function Block

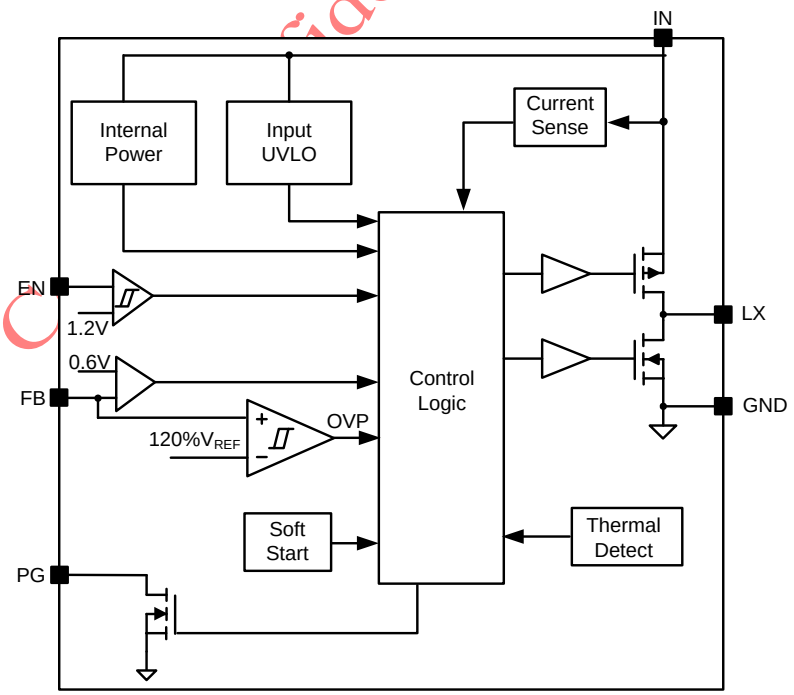


Figure2. Block Diagram

Absolute Maximum Ratings (Note 1)

Supply Input Voltage ---------- -0.3V to 6.0V
FB, EN, PG Voltage ---------- -0.3V to V_{IN} + 0.6V
LX Voltage ---------- -0.3V (*1) to 6.0V (*2)
Power Dissipation, P_D @ T_A = 25℃ ---------- 1.1W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 90℃/W
θ_{JC} ---------- 20℃/W
Junction Temperature Range ---------- -40℃ to 150℃
Lead Temperature (Soldering, 10 sec.) ---------- 260℃
Storage Temperature Range ---------- -65℃ to 150℃
(*1) LX Voltage Tested Down to -3V <20ns
(*2) LX Voltage Tested Up to +7V <20ns

Recommended Operating Conditions (Note 3)

Supply Input Voltage ---------- 2.5V to 5.5V
Junction Temperature Range ---------- -40℃ to 125℃
Ambient Temperature Range ---------- -40℃ to 85℃

Electrical Characteristics

(V_{IN} = 5V, V_{OUT} = 1.8V, L = 1.0μH, C_{OUT} = 22μF, T_A = 25℃, unless otherwise specified)

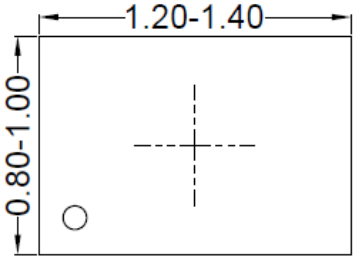
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		2.5		5.5	V
Input UVLO Threshold	V_{UVLO}			2.45	2.5	V
Input UVLO Hysteresis	V_{YST}			150		mV
Shutdown Current	I_{SHDN}	V_{EN}=0V		0.1	1	μA
Quiescent Current	I_Q	V_{FB}=V_{REF}×105%		55		μA
Feedback Reference Voltage	V_{REF}	I_{OUT}=1A, CCM	0.591	0.6	0.609	V
LX Node Discharge Resistance	R_{DIS}			50		Ω
Top FET R_{ON}	$R_{DS(ON)1}$			125		mΩ
Bottom FET R_{ON}	$R_{DS(ON)2}$			75		mΩ
EN Input Voltage High	$V_{EN,H}$		1.2			V
EN Input Voltage Low	$V_{EN,L}$				0.4	V
PG Threshold for Under Voltage Detection	$V_{PG,UVP}$			90		%
PG Low Delay Time for Under Voltage Detection	$t_{UVP,DLY}$			15		μs
PG Threshold for Over Voltage Detection	$V_{PG,OVP}$			120		%
PG Low Delay Time for Over Voltage Detection	$t_{OVP,DLY}$			15		μs
Min ON Time	$t_{ON,MIN}$			50		ns
Maximum Duty Cycle	D_{MAX}		100			%
Turn On Delay Time	$t_{ON,DLY}$	from EN high to LX start switching		0.25		ms
Soft-start Time	t_{SS}	V_{OUT} from 0% to 100%		0.75		ms
Switching Frequency	f_{SW}	I_{OUT}=1A, CCM		1.5		MHz
Top FET Current Limit	$I_{LMT,TOP}$		3			A
Output Under Voltage Protection Threshold	V_{UVP}			50		%V_{REF}
Output UVP Delay	$t_{UVP,DLY}$			10		μs
UVP Hiccup ON Time	$t_{UVP,ON}$			1.45		ms
UVP Hiccup OFF Time	$t_{UVP,OFF}$			1.45		ms
Thermal Shutdown Temperature	T_{SD}			160		℃
Thermal Shutdown Hysteresis	T_{HYS}			20		℃

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

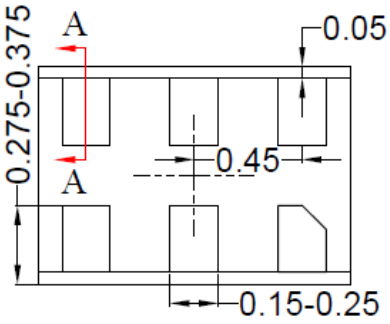
Note2: θ_{JA} of SM80592IHD is measured in the natural convection at T_A = 25℃ on 2OZ two-layer Silergy evaluation board. Pin 1 is the case position for SM80592IHD θ_{JC} measurement.

Note 3: The device is not guaranteed to function outside its operating conditions.

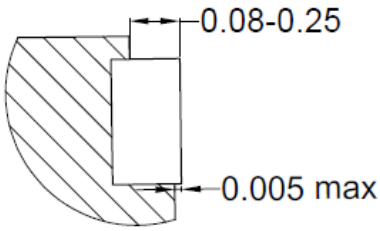
DFN1.3×0.9-6 Package Outline Drawing



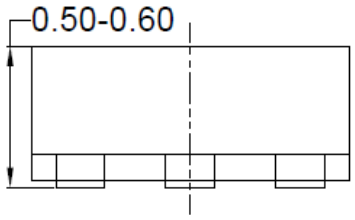
Top View



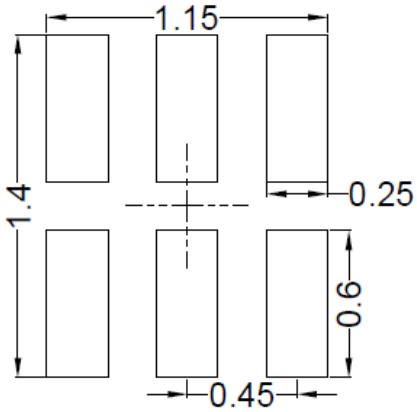
Bottom View



A-A



Front View



Recommended PCB layout
(Reference only)

Notes: 1, All dimension in millimeter and exclude mold flash & metal burr
2, center line refers chip body center

单击下面可查看定价，库存，交付和生命周期等信息

>>SILERGY(矽力杰)