General Description

SY8891E is a high efficiency 1.5MHz synchronous step down DC/DC regulator, capable of delivering up to 1A output current. It can operate over a wide input voltage range from 2.5V to 5.5V and integrate main switch and synchronous switch with very low $R_{DS\ (ON)}$ to minimize the conduction loss.

SY8891E is in a space saving, low profile SOT563 package.

Ordering Information

SY8891 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY8891EARC	SOT563	--

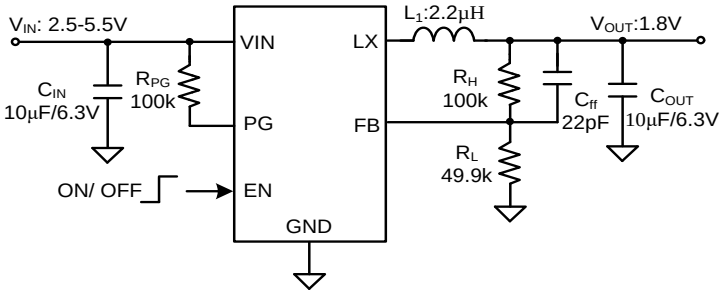
Features

- 2.5V to 5.5V Input Voltage Range.
- Low $R_{DS(ON)}$ for Internal Switches (top/bottom) 170mΩ /100mΩ
- High Switching Frequency 1.5MHz Minimizes the External Components
- Internal Soft-start Limits the Inrush Current
- 100% Dropout Operation
- Forced PWM Operation
- Power Good Indicator
- Hic-cup for Short Circuit Protection
- Output Auto Discharge Function
- RoHS Compliant and Halogen Free
- Compact Package: SOT563

Applications

- Set Top Box
- USB Dongle
- Media Player
- Smart Phone

Typical Application



Inductor and C_{OUT} Selection Table

V_{OUT} [V]	L [µH]	C_{OUT} [µF]		
		4.7	10	22
1.2	1.5		√	√
	2.2		☆	√
1.8	1.5		√	√
	2.2		☆	√
3.3	2.2		☆	√

Figure1. Schematic Diagram

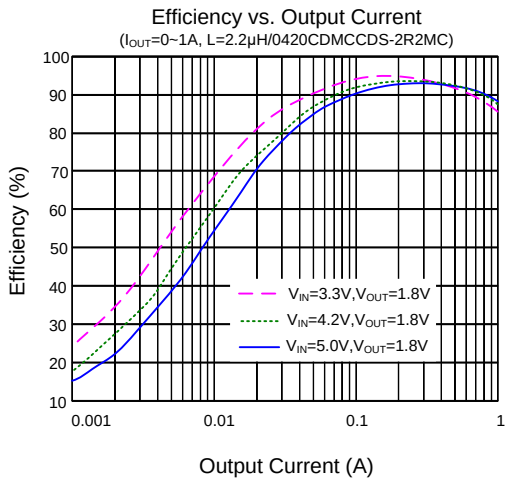
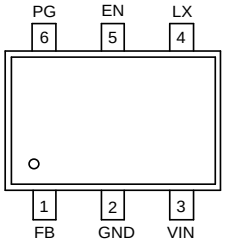


Figure2. Efficiency vs. Output Current

Pin out (Top View)



Top Mark: E2 *xyz* (device code: E2, ***x=year code, y=week code, z= lot number code)***

Pin Description

Pin Name	Pin Number	Pin Description
FB	1	Output feedback pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: $V_{OUT}=0.6\times(1+R_H/R_L)$.
GND	2	Ground pin.
VIN	3	Input pin. Decouple this pin to GND pin with at least a 10μF ceramic capacitor.
LX	4	Inductor pin. Connect this pin to the switching node of inductor.
EN	5	Enable control. Pull high to turn on. Do not leave it floating.
PG	6	Power good indicator. Power good indicator (open drain output). Low if the output < 90% or the output >120% of regulation voltage; High otherwise. Connect a pull-up resistor to the input.

Function Block

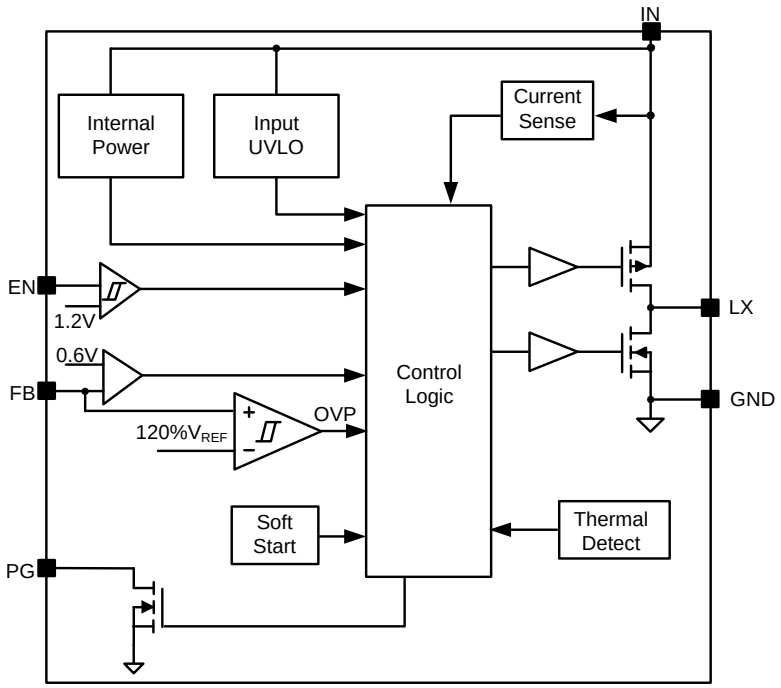


Figure3. Block Diagram

Absolute Maximum Ratings (Note 1)

Supply Input Voltage ---------- -0.3V to 6.0V
FB, EN, PG Voltage ---------- -0.3V to V_{IN} + 0.6V
LX Voltage ---------- -0.3V (*1) to 6.0V (*2) (*3)
Power Dissipation, P_D @ T_A = 25°C ---------- 0.95W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 105°C/W
θ_{JC} ---------- 30°C/W
Junction Temperature Range ---------- -40°C to 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C
(*1) LX Voltage Tested Down to -3V <20ns
(*2) LX Voltage Tested Up to +7V <20ns
(*3) LX Voltage Tested Up to +8.5V <2ns (Note3)

Recommended Operating Conditions (Note 4)

Supply Input Voltage ---------- 2.5V to 5.5V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(V_{IN} = 5V, V_{OUT} = 1.8V, L = 2.2μH, C_{OUT} = 10μF, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		2.5		5.5	V
Input UVLO Threshold	V_{UVLO}			2.45	2.5	V
Input UVLO Hysteresis	V_{YST}			150		mV
Shutdown Current	I_{SHDN}	V_{EN}=0V		0.1	1	μA
Feedback Reference Voltage	V_{REF}	I_{OUT}=0A, CCM	0.591	0.6	0.609	V
LX Node Discharge Resistance	R_{DIS}			50		Ω
Top FET R_{ON}	$R_{DS(ON)1}$			170		mΩ
Bottom FET R_{ON}	$R_{DS(ON)2}$			100		mΩ
EN Input Voltage High	$V_{EN,H}$		1.2			V
EN Input Voltage Low	$V_{EN,L}$				0.4	V
PG Threshold for Under Voltage Detection	$V_{PG,UVP}$			90		%
PG Low Delay Time for Under Voltage Detection	$t_{UVP,DLY}$			15		us
PG Threshold for Over Voltage Detection	$V_{PG,OVP}$			120		%
PG Low Delay Time for Over Voltage Detection	$t_{OVP,DLY}$			15		us
Min ON Time	$t_{ON,MIN}$			50		ns
Maximum Duty Cycle	D_{MAX}		100			%
Turn on Delay Time	$t_{ON,DLY}$	from EN high to LX start switching		0.25		ms
Soft-start Time	t_{SS}	V_{OUT} from 0% to 100%		0.75		ms
Switching Frequency	f_{SW}	I_{OUT}=0A, CCM		1.5		MHz
Top FET Current Limit	$I_{LMT,TOP}$		1.4		2.5	A
Bottom FET Reverse Current Limit	$I_{LMT,RVS}$		0.3		0.85	A
Output Under Voltage Protection Threshold	V_{UVP}			50		$\%V_{REF}$
Output UVP Delay	$t_{UVP,DLY}$			10		μs
UVP Hiccup On Time	$t_{UVP,ON}$			1.45		ms
UVP Hiccup Off Time	$t_{UVP,OFF}$			1.45		ms
Thermal Shutdown Temperature	T_{SD}			160		°C
Thermal Shutdown Hysteresis	T_{HYS}			20		°C

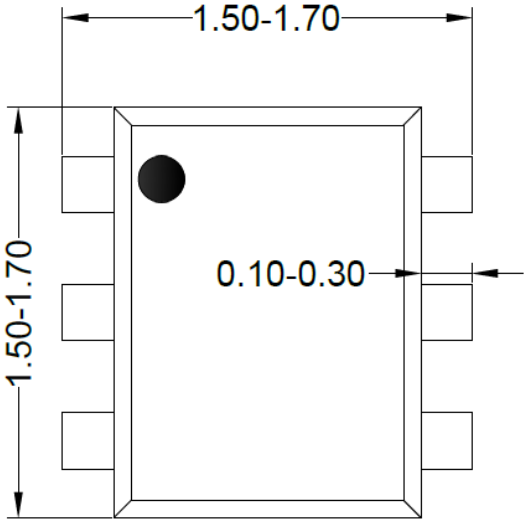
Note1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note2: θ_{JA} of SY8891EARC is measured in the natural convection at T_A = 25°C on 2OZ two-layer Silergy evaluation board. Pin 4 is the case position for SY8891EARC θ_{JC} measurement.

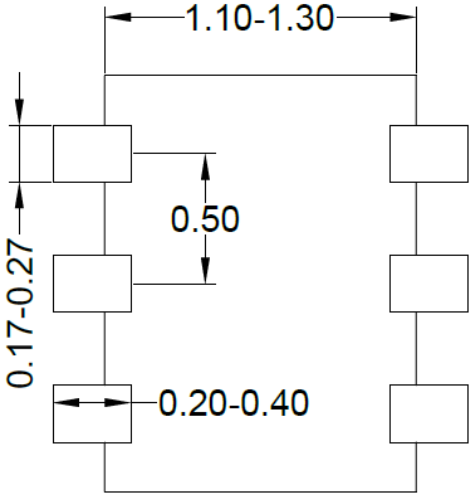
Note3: The voltage is measured by 500MHz bandwidth oscilloscope. Probe point should be the LX and GND pins, and the loop formed by probe tip and ground ring should be minimized to avoid noise coupling.

Note4: The device is not guaranteed to function outside its operating conditions.

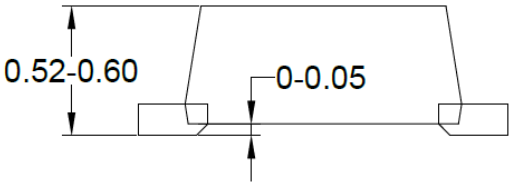
SOT563 Package Outline Drawing



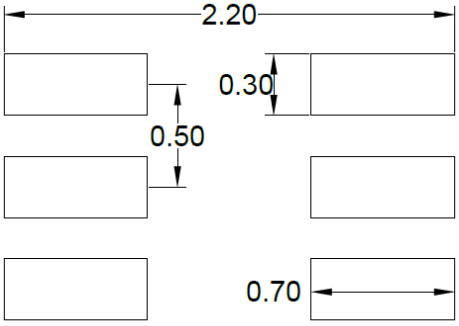
Top view



Bottom view



Side View



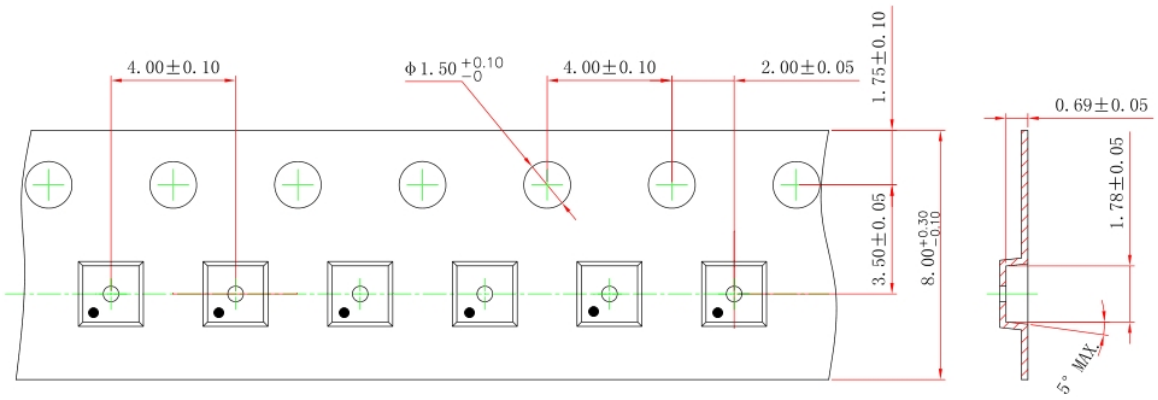
Recommended PCB layout
(Reference only)

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

Taping & Reel Specification

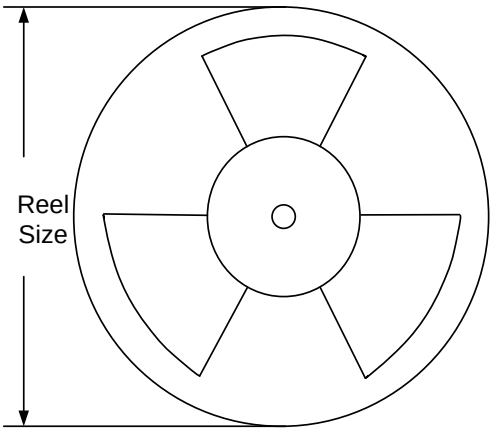
1. Taping Orientation

SOT563



Feeding Direction ⟶

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
SOT563	8	4	7”	280	160	5000

3. Others: NA

单击下面可查看定价，库存，交付和生命周期等信息

>>SILERGY(矽力杰)