Application Notes: AN_SY8186

High Efficiency Fast Response, 16A, 18V Input Synchronous Step Down Regulator

Preliminary Specification

General Description

The SY8186 develops a high efficiency synchronous step-down DC-DC regulator capable of delivering 16A current. The device integrates main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss. The SY8186 operate over a wide input voltage range from 4V to 18V.

The device adopts the instant PWM architecture to achieve fast transient responses for high step down applications and high efficiency at light loads. In addition, it operates at pseudo-constant frequency of 500kHz under continuous conduction mode to minimize the size of inductor and capacitor.

Ordering Information

SY78186 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY8186QXC	QFN4x4-11	--

Features

- Low $R_{DS(ON)}$ for internal switches (top/bottom): 7.5/2.5 mΩ
- Wide input voltage range: 4-18V
- External bypass input for higher light load efficiency
- Instant PWM architecture to achieve fast transient responses
- Internal 1ms soft-start limits the inrush current
- Pseudo-constant frequency: 500kHz
- 16A output current capability
- ±1% 0.6V reference
- Programmable valley current limit
- Power good indicator
- Output discharge function
- Output short circuit latch off protection
- Output over voltage latch off protection
- Input UVLO
- Over temperature protection
- RoHS Compliant and Halogen Free
- Compact package: QFN4x4-11

Applications

- LCD-TV/Net-TV/3DTV
- Set Top Box
- Notebook
- High Power AP

Typical Applications

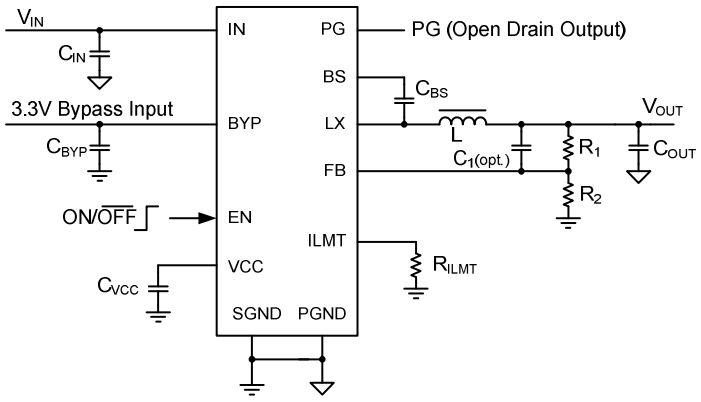


Figure 1 Schematic

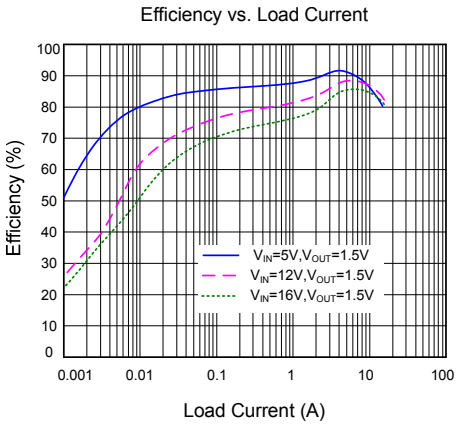
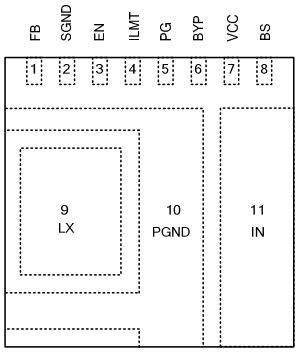


Figure 2. Efficiency

Pinout (top view)



QFN4x4-11

Top Mark: **AQQ*xyz*, (**Device code: AQQ, ***x=year code, y=week code, z= lot number code*****)**

Pin Name	Pin Number	Pin Description
FB	1	Output feedback pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: Vout=0.6*(1+R1/R2)
SGND	2	Signal ground pin.
EN	3	Enable control. Pull this pin high to turn on the IC. Do not leave this pin floating.
ILMT	4	Current limit setting pin. Connect a resistor from this pin to ground to program the bottom FET current limit. $I_{LMT}(A) = 2880/R_{ILMT}(k\Omega)$
PG	5	Power good Indicator. Open drain output when the output voltage is within 90% to 120% of regulation point. Pull low otherwise
BYP	6	Bypass input for the internal LDO. BYP can be connected to external 3.3V DC supply. When the BYP voltage rises above the bypass switch turn-on threshold, the internal 3.3V LDO shuts down and the VCC pin is connected to the BYP pin through an internal switch.
VCC	7	Internal 3.3V LDO output. Power supply for internal analog circuits and driving circuit. Bypass a capacitor to SGND.
BS	8	Boot-strap pin. Supply high side gate driver. Decouple this pin to LX pin with 0.1uF ceramic cap.
LX	9	Inductor pin. Connect this pin to the switching node of inductor
PGND	10	Power ground pin
IN	11	Input pin. Decouple this pin to PGND pin with at least 22uF ceramic cap

Absolute Maximum Ratings (Note 1)

IN, LX, PG, EN ---------- 19V
BS-LX, FB, ILMT, VCC, BYP ---------- 4V
SGND-PGND ---------- -0.3V to 0.3V
Power Dissipation, PD @ T_A = 25°C QFN4X4-11 FC---------- 3.5W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 2°C/W
θ_{JC} ---------- 28°C/W
Junction Temperature Range ---------- 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C
Dynamic LX voltage in 10ns duration ---------- IN+3V to PGND-5V

Recommended Operating Conditions (Note 3)

Supply Input Voltage ---------- 4V to 18V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(V_{IN} = 12V, V_{OUT} = 1.5V, C_{OUT} = 100uF, T_A = 25°C, I_{OUT} = 1A unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		4.0		18	V
Quiescent Current	I_Q	I_{OUT}=0, V_{FB}=V_{REF}*105%		200		μA
Shutdown Current	I_{SHDN}	EN=0		7	10	μA
Feedback Reference Voltage	V_{REF}		0.594	0.6	0.606	V
FB Input Current	I_{FB}	V_{FB}=4V	-50		50	nA
Top FET RON	Rds(on)1			7.5		mΩ
Bottom FET RON	Rds(on)2			2.5		mΩ
Discharge FET RON	Rdis			50		Ω
Bottom FET Current	I_{LMT}			2880k/ R_{ILMT}		A
Bottom FET Current Limit Program Range	$I_{LMT,RNG}$		12		24	A
Bottom FET Current Limit Accuracy	$I_{LMT, ACC}$		-20		20	%
Soft-start Time	T_{SS}			1		ms
EN Rising Threshold	V_{ENH}		0.8			V
EN Falling Threshold	V_{ENL}				0.4	V
Input UVLO Threshold	V_{UVLO}				3.9	V
UVLO hysteresis	V_{HYS}			0.3		V
Oscillator Frequency Program Range	F_{OSC}		425	500	575	kHz
Min ON Time	$t_{ON,MIN}$			80		ns
Min OFF Time	$t_{OFF,MIN}$			120		ns
VCC Output	V_{CC}	V_{IN}=4V	3.2	3.3	3.4	V
Output Over Voltage Threshold	V_{OVP}	V_{FB} Rising	115	120	125	%V_{REF}
Output Over Voltage Hysteresis	$V_{OVP,HYS}$			2		%V_{REF}
Output Over Voltage Delay Time	$t_{OVP, DLY}$			10		us
Power Good Threshold	V_{PG}	V_{FB} Rising (Good)	88	90	92	%V_{REF}
Power Good Hysteresis	$V_{PG,HYS}$			2		%V_{REF}
Power Good Delay Time	$t_{PG, DLY}$			10		us
Bypass Switch RON	R_{BYP}			5		Ohm
Bypass Switch Turn-on Voltage	$V_{BYP,ON}$		2.97	3.1		V
Bypass Switch Switchover Hysteresis	$V_{BYP,SW}$			0.2		V
BYP Input Voltage Range	V_{BYP}		3.250	3.3	3.350	V
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Shutdown hysteresis	T_{HYS}			15		°C

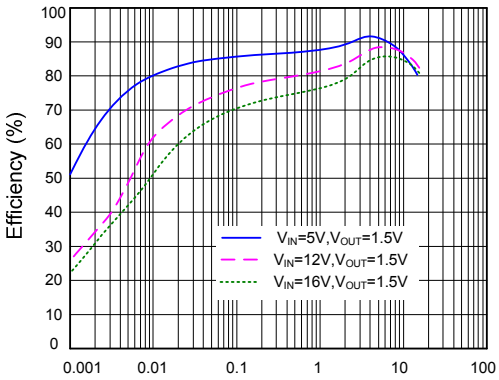
Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Note 2: θJA is measured in the natural convection at TA = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 3: The device is not guaranteed to function outside its operating conditions.

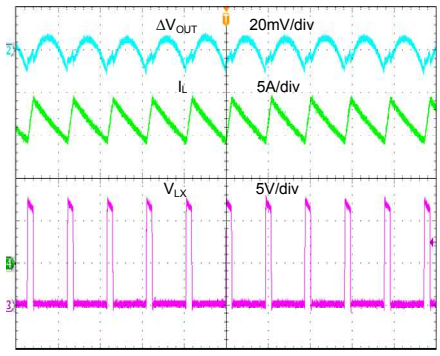
Typical Performance Characteristics

Efficiency vs. Load Current



Output Ripple

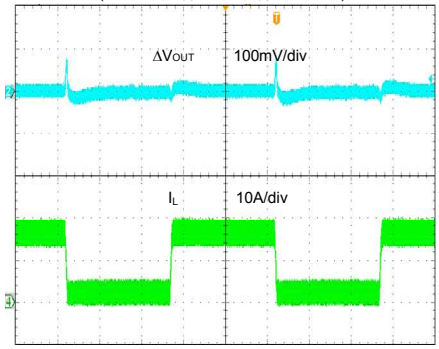
(V_{IN}=12V, V_{OUT}=1.5V, I_{OUT}=16A)



Time (2μs/div)

Load Transient

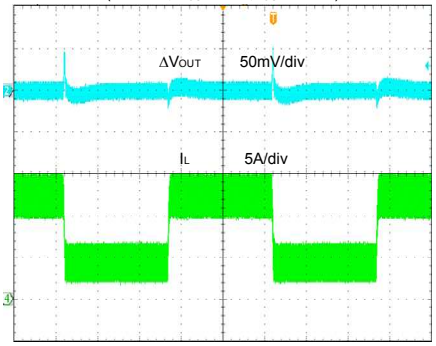
(V_{IN}=12V, V_{OUT}=1.5V, I_{OUT}=1.6-16A)



Time (200μs/div)

Load Transient

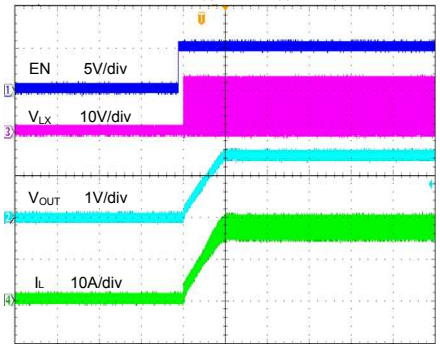
(V_{IN}=12V, V_{OUT}=1.5V, I_{OUT}=4-12A)



Time (200μs/div)

Startup from Enable

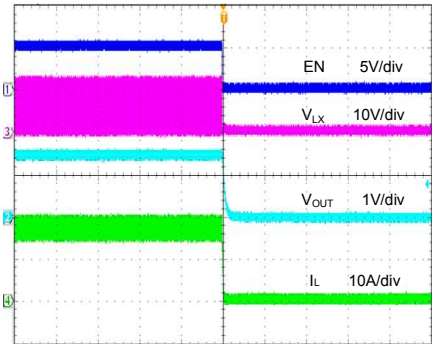
(V_{IN}=12V, V_{OUT}=1.5V, I_{OUT}=16A)



Time (800μs/div)

Shutdown from Enable

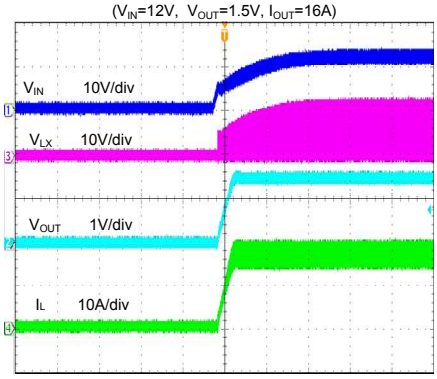
(V_{IN}=12V, V_{OUT}=1.5V, I_{OUT}=16A)



Time (200μs/div)

Startup from VIN

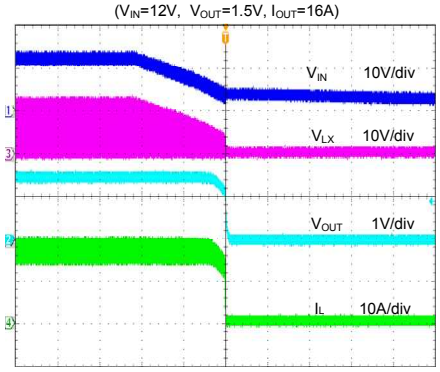
(V_{IN}=12V, V_{OUT}=1.5V, I_{OUT}=16A)



Time (2ms/div)

Shutdown from VIN

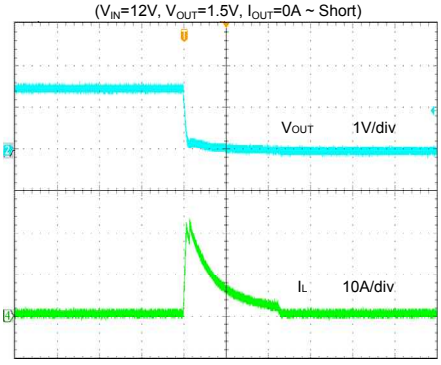
(V_{IN}=12V, V_{OUT}=1.5V, I_{OUT}=16A)



Time (400μs/div)

Short Circuit Protection

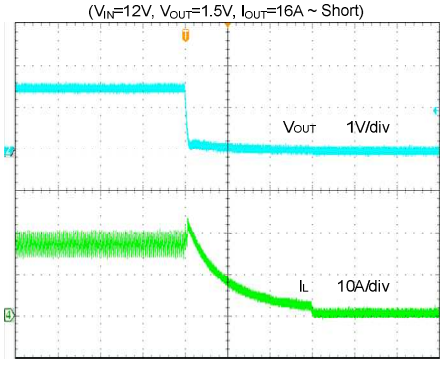
(V_{IN}=12V, V_{OUT}=1.5V, I_{OUT}=0A ~ Short)



Time (40μs/div)

Short Circuit Protection

(V_{IN}=12V, V_{OUT}=1.5V, I_{OUT}=16A ~ Short)



Time (40μs/div)

Operation

The SY8186 develops a high efficiency synchronous step-down DC-DC regulator capable of delivering 16A current. The device integrates main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss. The SY8186 operate over a wide input voltage range from 4V to 18V.

The device adopts the instant PWM architecture to achieve fast transient responses for high step down applications and high efficiency at light loads. In addition, it operates at pseudo-constant frequency of 500kHz under continuous conduction mode to minimize the size of inductor and capacitor.

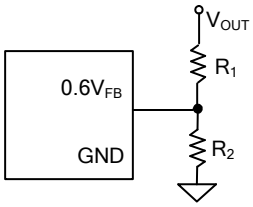
Applications Information

Because of the high integration in the SY8186 IC, the application circuit based on this regulator IC is rather simple. Only input capacitor C_{IN}, output capacitor C_{OUT}, output inductor L and feedback resistors (R_1 and R_2) need to be selected for the targeted applications specifications.

Feedback resistor dividers R_1 and R_2:

Choose R_1 and R_2 to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R_1 and R_2. A value of between 10kΩ and 1MΩ is highly recommended for both resistors. If Vout is 3.3V, R_1=100k is chosen, then using following equation, R_2 can be calculated to be 22.1k:

$$R_2 = \frac{0.6V}{V_{OUT} - 0.6V} R_1 .$$



Input capacitor C_{IN}:

The ripple current through input capacitor is calculated as:

$$I_{CIN\_RMS} = I_{OUT} \cdot \sqrt{D(1-D)} \cdot$$

To minimize the potential noise problem, place a typical X5R or better grade ceramic capacitor really close to the IN and GND pins. Care should be taken to minimize the loop area formed by C_{IN}, and IN/GND pins. In this case, a 22uF low ESR ceramic capacitor is recommended.

Output capacitor C_{OUT}:

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For most applications, an X5R or better grade ceramic capacitor greater than 120uF capacitance can work well. The capacitance derating with DC voltage must be considered.

Output inductor L:

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{F_{SW} \times I_{OUT,MAX} \times 40\%}$$

where Fsw is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

The SY8186 regulator IC is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{V_{OUT}(1\text{-}V_{OUT}/V_{IN,MAX})}{2 \cdot F_{SW} \cdot L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<10mΩ to achieve a good overall efficiency.

Current limit setting

The current limit can be programmed with a resistor R_{ILMT} connecting from ILMT pin to ground:

$$I_{ILMT} = \frac{2880k}{R_{ILMT}} (\mathrm{A})$$

Soft-start

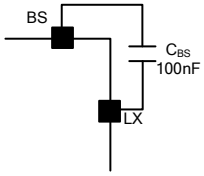
The SY8186 has a built-in soft-start to control the rise rate of the output voltage and limit the input current surge during IC start-up. The typical soft-start time is 1ms.

Enable Operation

Pulling the EN pin low (<0.4V) will shut down the device. During shutdown mode, the SY8186 shutdown current drops to lower than 10uA. Driving the EN pin high (>0.8V) will turn on the IC again.

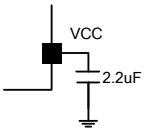
External Boostrap Cap

This capacitor provides the gate driver voltage for internal high side MOSEFET. A 100nF low ESR ceramic capacitor connected between BS pin and LX pin is recommended.



VCC LDO

The 3.3V VCC LDO provides the power supply for internal control circuit. Bypass this pin to ground with a 2.2uf ceramic capacitor.



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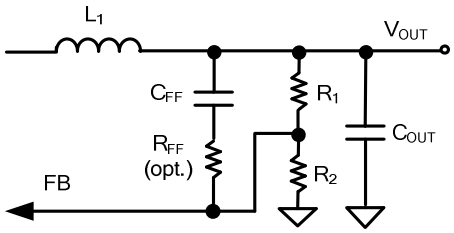
Power Good Indication

PG is an open drain output. This pin is externally pulled high when the FB voltage is within 90% to 120% of the internal reference voltage. Otherwise is pulled low.

Load Transient Considerations:

The SY8186 regulator IC adopts the instant PWM architecture to achieve good stability and fast transient responses. In applications with high step load current, adding an RC network R_{FF} and C_{FF} parallel with R1 may further speed up the load transient responses.



Layout Design:

The layout design of SY8186 regulator is relatively simple. For the best efficiency and minimum noise problem, we should place the following components close to the IC: C_{IN}, C_{VCC} L, R1 and R2.

1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.

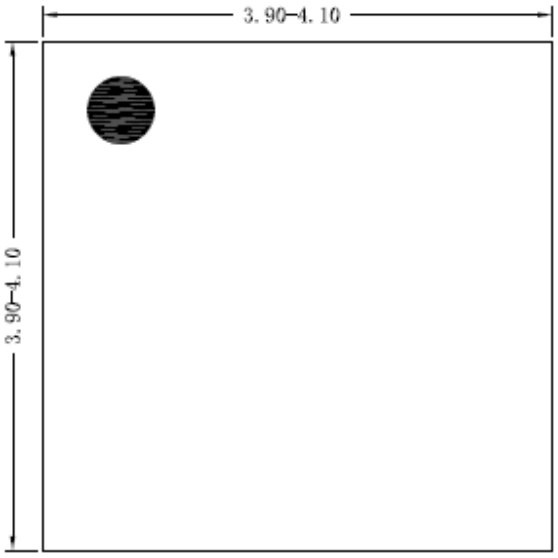
2) C_{IN} must be close to Pins IN and GND. The loop area formed by C_{IN} and GND must be minimized.

3) The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem.

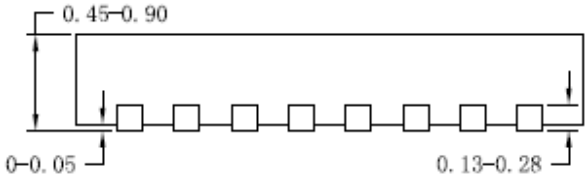
4) The components R_1 and R_2, and the trace connecting to the FB pin must NOT be adjacent to the LX net on the PCB layout to avoid the noise problem.

5) If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the IN pin is connected directly to a power source such as a Li-Ion battery, it is desirable to add a pull down 1Mohm resistor between the EN and GND pins to prevent the noise from falsely turning on the regulator at shutdown mode.

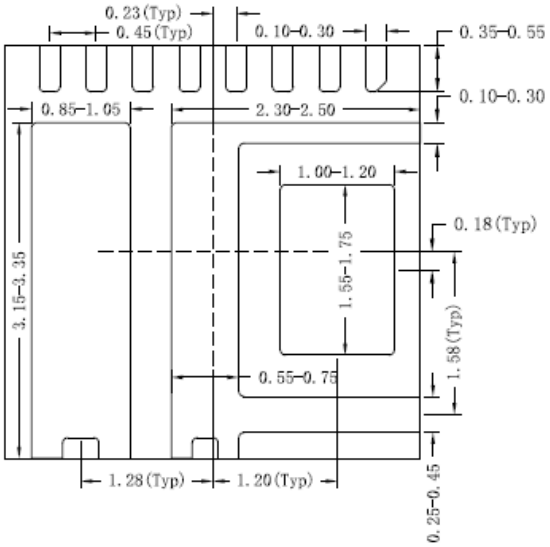
QFN4x4-11 Package Outline

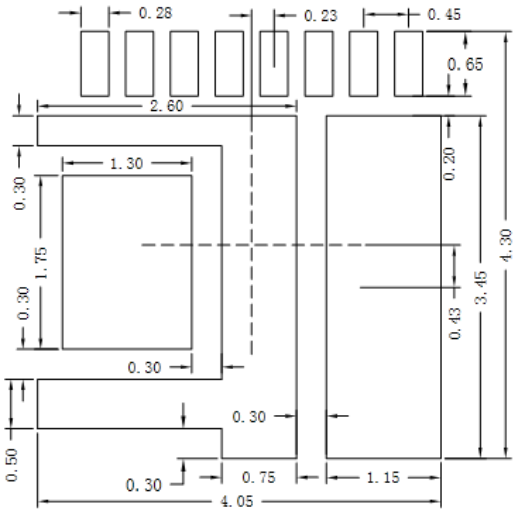


Top View



Side View





Bottom View

Notes: **All dimension in MM and exclude mold flash & metal burr**

单击下面可查看定价，库存，交付和生命周期等信息

>>SILERGY(矽力杰)