SYT06U05DVC

Ultra-Low Capacitance TVS Protection

Features

- Transient protection for high-speed data lines
  IEC 61000-4-2 (ESD) ±20kV (Air)
  ±20kV (Contact)
  IEC 61000-4-5 (Surge) 3A (8/20μs)
- For 5V and below operating voltage
- Ultra-small package (2.5mm×1.0mm×0.55mm)
- Protects four data lines
- Ultra Low capacitance: 0.6pF for each channel
- Low leakage current: 0.1μA @ V_{RWM} (Typical)
- Low clamping voltage
- Each I/O pin can withstand over 1000 ESD strikes for ±8kV contact discharge
- Pb free & RoHS Compliant

Description

SYT06U05DVC is an ultra-low capacitance Transient Voltage Suppressor (TVS) designed to provide electrostatic discharge (ESD) protection for high-speed data interfaces. With typical capacitance of 0.6pF only, SYT06U05DVC is designed to protect parasitic-sensitive systems against over-voltage and over-current transient events. It complies with IEC 61000-4-2 (ESD) (±20kV air, ±20kV contact discharge), IEC 61000-4-5 (Surge) (3A, 8/20μs), etc.

SYT06U05DVC uses ultra-small DFN2.5*1.0-10 package. Each SYT06U05DVC device can protect four high-speed data lines. The combined features of ultra-low capacitance, ultra-small size and high ESD robustness make SYT06U05DVC ideal for high-speed data ports and high-frequency lines (e.g., HDMI & DVI) applications. The low clamping voltage of the SYT06U05DVC guarantees a minimum stress on the protected IC.

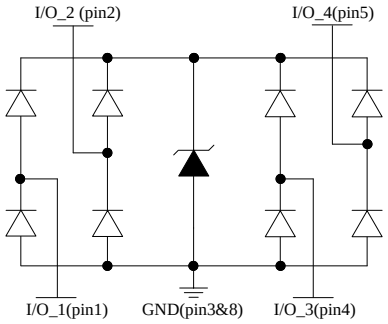
Applications

- Serial ATA
- PCI Express
- Desktops, Servers and Notebooks
- MDDI Ports
- USB2.0 Power and Data Line Protection
- Display Ports
- High Definition Multi-Media Interface (HDMI)
- Digital Visual Interfaces (DVI)

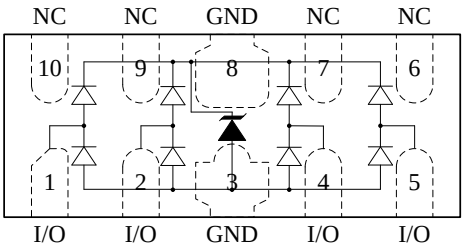
Mechanical Characteristics

- DFN2.5*1.0-10 package
- Flammability Rating: UL 94V-0
- Marking: Part number, Date
- Packaging: Tape and Reel

Circuit Diagram



Pin Configuration



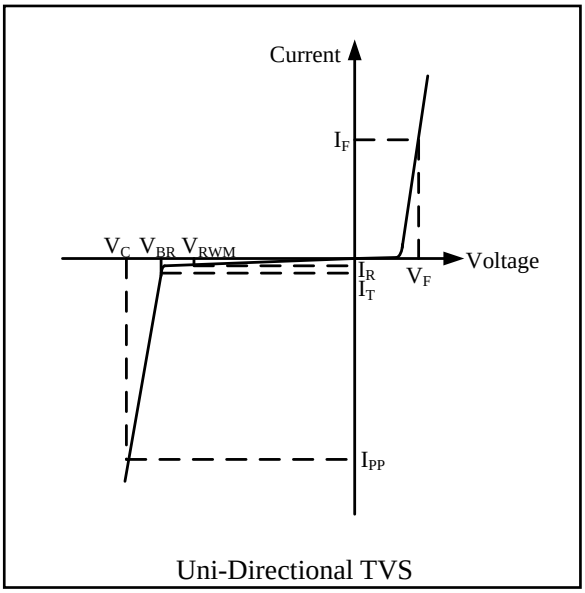
DFN2.5*1.0-10
(Top View)

Absolute Maximum Rating

Symbol	Parameter	Value	Units
I_{PP}	Peak Pulse Current (8/20μs)	3	A
P_{PK}	Peak Pulse Power (8/20μs)	45	Watts
V_{ESD}	ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	±20 ±20	kV
T_{OPT}	Operating Temperature	-40/+125	°C
T_{STG}	Storage Temperature	-55/+150	°C

Electrical Characteristics (T = 25°C)

Symbol	Parameter
V_{RWM}	Nominal Reverse Working Voltage
I_R	Reverse Leakage Current @ V_{RWM}
V_{BR}	Reverse Breakdown Voltage @ I_T
I_T	Test Current for Reverse Breakdown
V_C	Clamping Voltage @ I_{PP}
I_{PP}	Maximum Peak Pulse Current
C_{ESD}	Parasitic Capacitance
V_R	Reverse Voltage
f	Small Signal Frequency
I_F	Forward Current
V_F	Forward Voltage @ I_F



Uni-Directional TVS

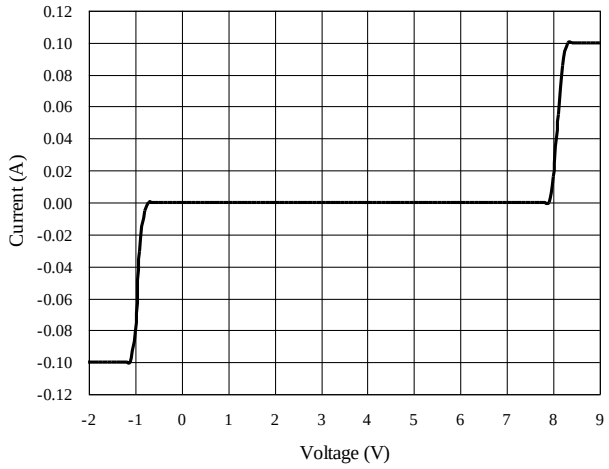
Symbol	Test Condition	Minimum	Typical	Maximum	Units
V_{RWM}				5.0	V
I_R	V_{RWM} = 5V, T = 25°C Between I/O and GND		0.1	1.0	μA
V_{BR}	I_T = 1mA Between I/O and GND	6.0	8.0	10.0	V
V_C[1]	I_{PP} = 3A, t_p = 8/20μs Between I/O and GND		10	12	V
V_C[1]	I_{PP} = 16A, t_p = 10/100ns Between I/O and GND		10.5	12.5	V
R_{DYN}[1,2]	t_p = 10/100ns Between I/O and GND		0.2		Ω
C_{ESD}[1]	V_R = 0V, f = 1MHz Between I/O and GND		0.6	0.8	pF
C_{ESD}[1]	V_R = 0V, f = 1MHz Between I/O and I/O		0.25	0.4	pF

NOTES

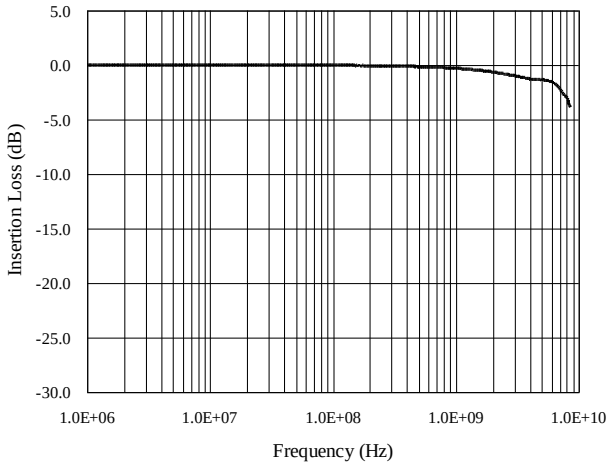
[1]Guaranteed by design and is not subject to production test.

[2]R_{DYN} calculated based on I_{PP}=8A to I_{PP}=16A, t_p = 10/100ns.

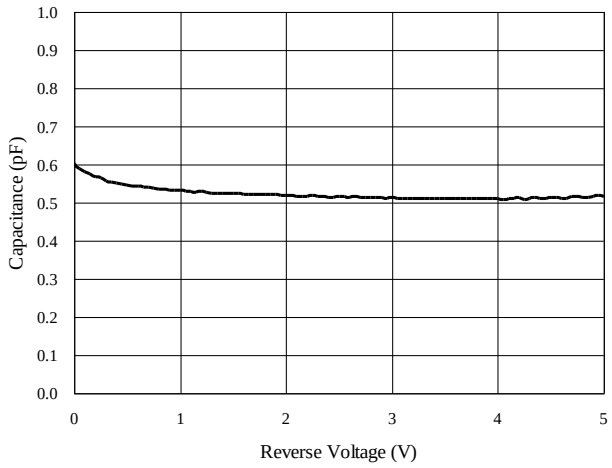
Voltage Sweeping of I/O to GND



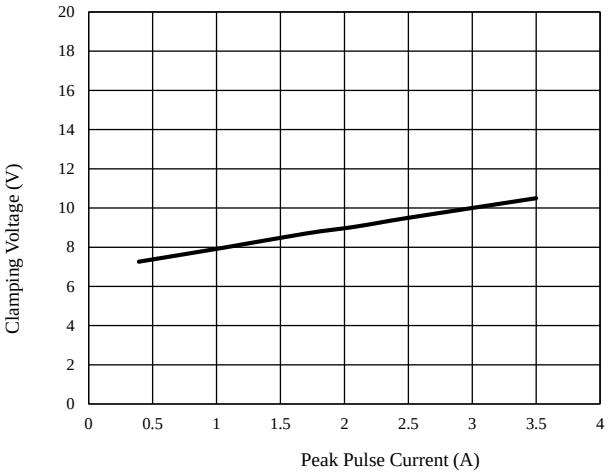
Insertion Loss S21 of I/O to GND



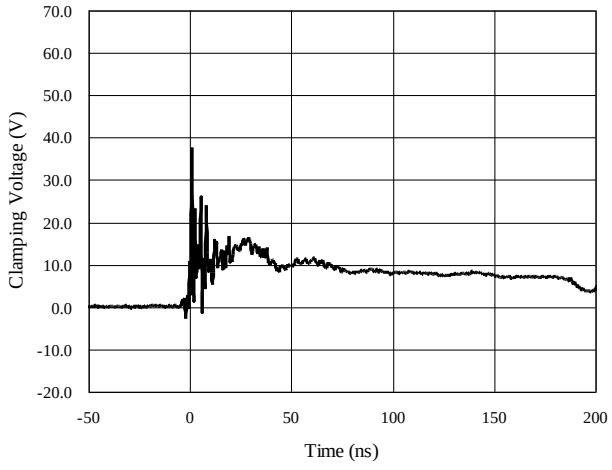
Capacitance vs. Voltage of I/O to GND (f = 1MHz)



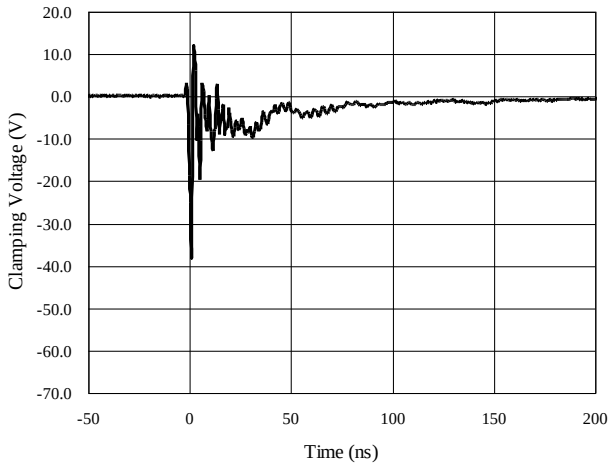
Clamping Voltage vs. Peak Pulse Current (8/20μs)



ESD Clamping of I/O to GND (+8kV Contact per IEC 61000-4-2)



ESD Clamping of I/O to GND (-8kV Contact per IEC 61000-4-2)



Application Information

Pin Connection in PCB

SYT06U05DVC provides ESD protection for four data lines simultaneously. The pin connection is shown in the figure below.

Four parallel data lines, from inner IC to I/O port connector, could connect to SYT06U05DVC four I/O pins directly. Pin 3&8 of SYT06U05DVC is the GND pin, which should connect to the GND of PCB. The wire should be as short as possible in order to minimize the parasitic inductance.

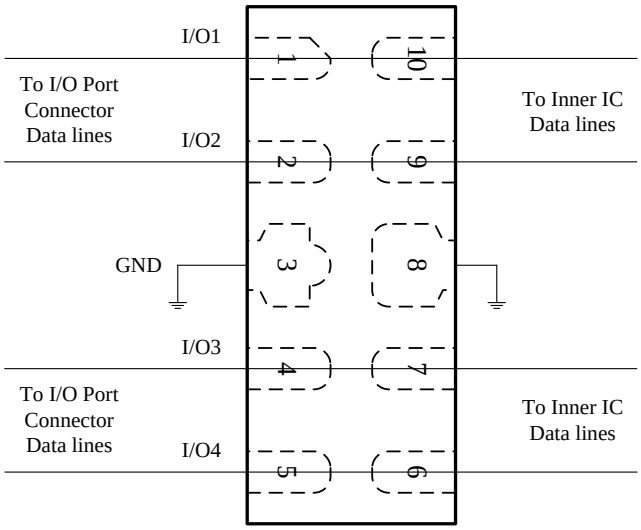


Figure1. SYT06U05DVC pin connection in PCB

PCB Layout Guidelines

For optimum ESD protection and the whole circuit performance, the following PCB layout guidelines are recommended:

- SYT06U05DVC GND pin to the PCB GND rail path should be as short as possible. It could reduce the ESD transient return path to GND.
- The vias connecting SYT06U05DVC GND pins to the PCB GND should be wide.
- Place SYT06U05DVC as close to the connector port as possible. It could reduce the parasitic inductance and restrict ESD coupling into adjacent traces.
- Avoid running critical signals near board edges.

Application Information

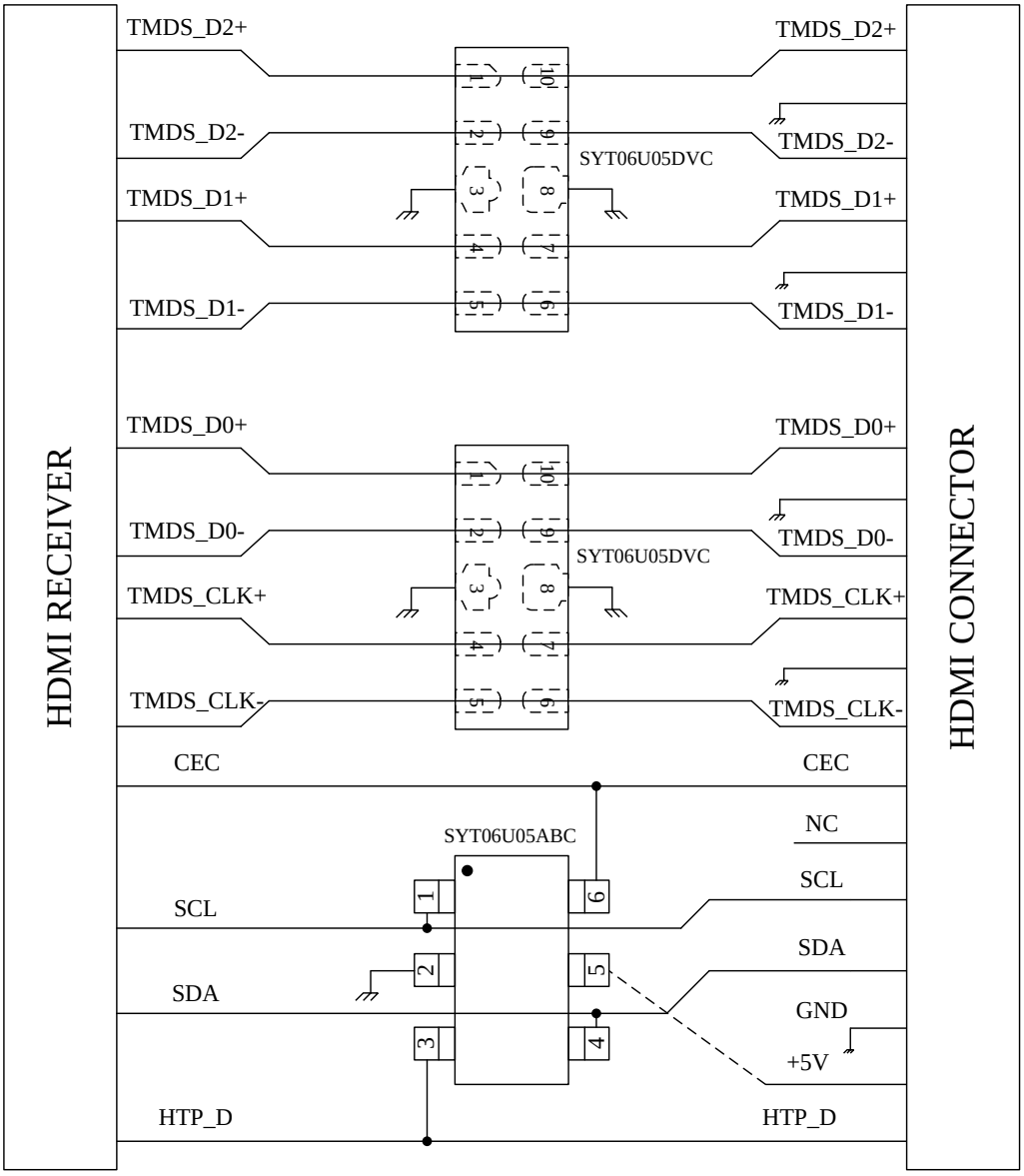
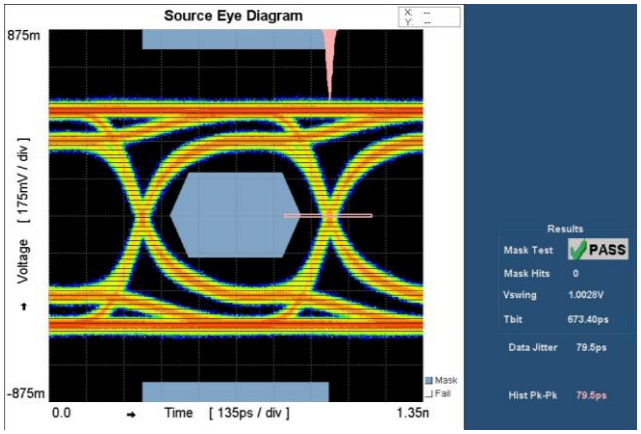
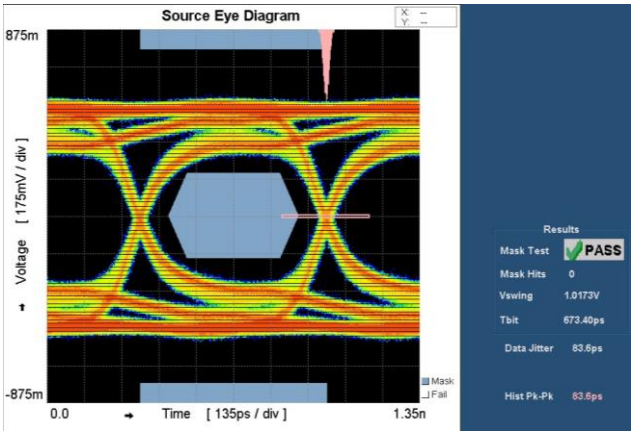


Figure2. Layout Top View for HDMI Interface with SYT06U05DVC & SYT06U05ABC

Eye Diagram Measurements for 1080P HDMI Data Transmission



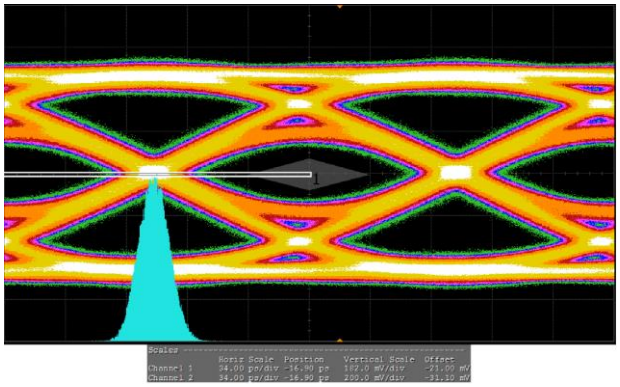
Without TVS



With SYT06U05DVC

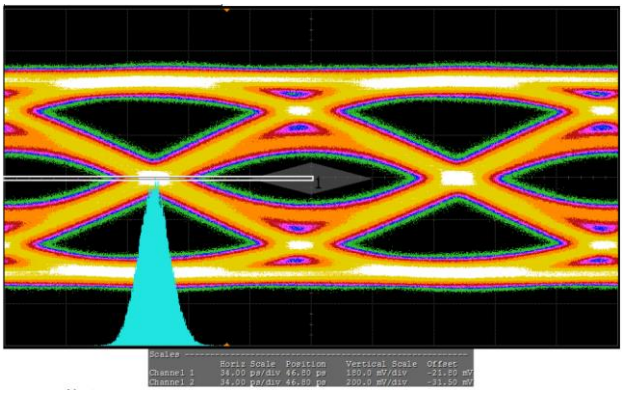
Figure3. Eye Diagram Measurements for 1080P HDMI

Eye Diagram Measurement for HDMI2.0



Data Rate：6Gb/s

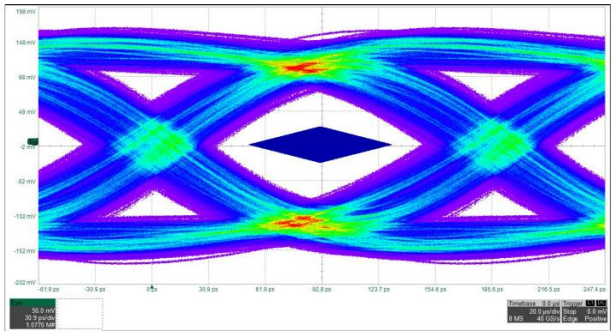
Figure 4 HDMI2.0 Eye Diagram without SYT06U05DVC



Data Rate：6Gb/s

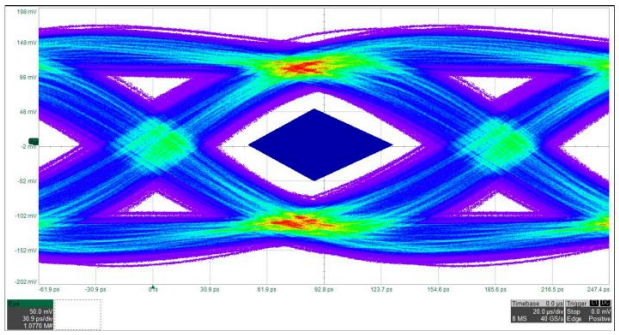
Figure 5 HDMI2.0 Eye Diagram with SYT06U05DVC

Eye Diagram Measurement for USB3.0



Data Rate：5.4Gb/s

Figure 6 USB3.0 Eye Diagram without SYT06U05DVC



Data Rate：5.4Gb/s

Figure 7 USB3.0 Eye Diagram with SYT06U05DVC

TDR Measurements for HDMI

The combination of low capacitance, small package, and flow-through design means it is possible to use SYT06U05DVC to meet the HDMI impedance requirements of 100 Ohms ±15%. Figures 8 shows impedance test result for a TDR rise time of 100ps, using a CitrusCom evaluation board with 100 Ohm differential traces. Measurements were taken using a TDR method as outlined in the HDMI Compliance Test Specification (CTS). In this case, the device meets the HDMI CTS requirement of 100 Ohm ±15% with plenty of margin.

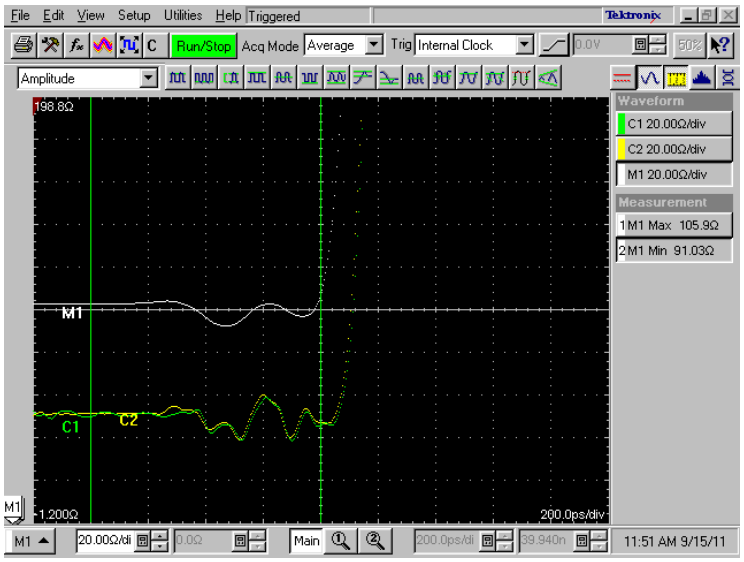
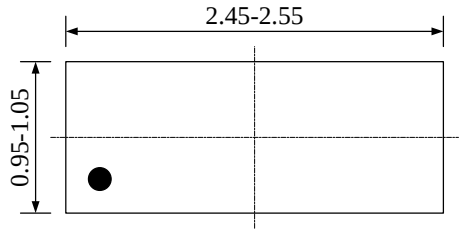


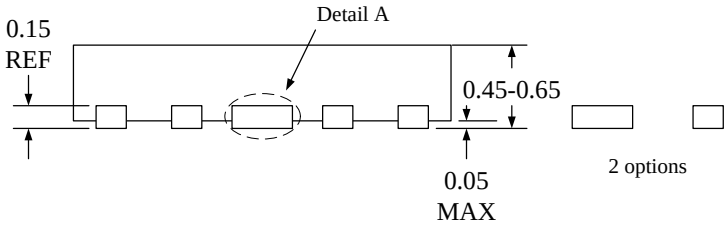
Figure 8. TDR Measurements for HDMI

Package Outline

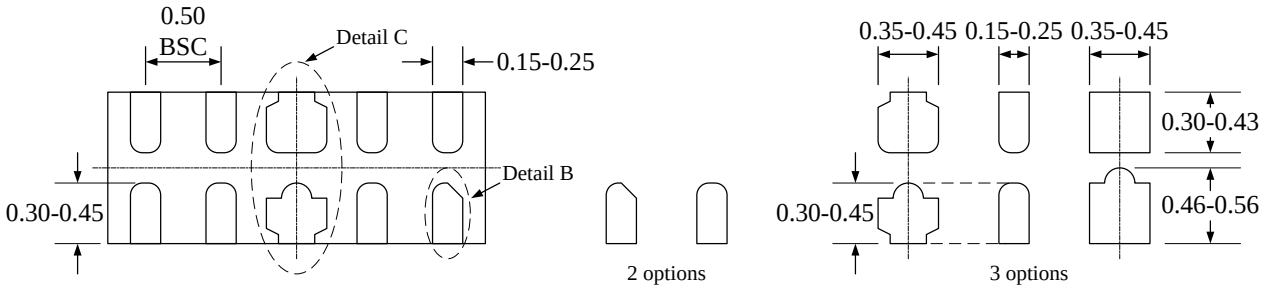
- DFN2.5x1.0-10 package



TOP VIEW



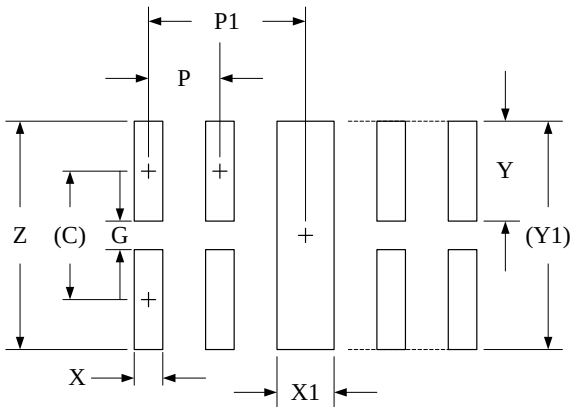
SIDE VIEW **Detail A**



BOTTOM VIEW **Detail B** **Detail C**

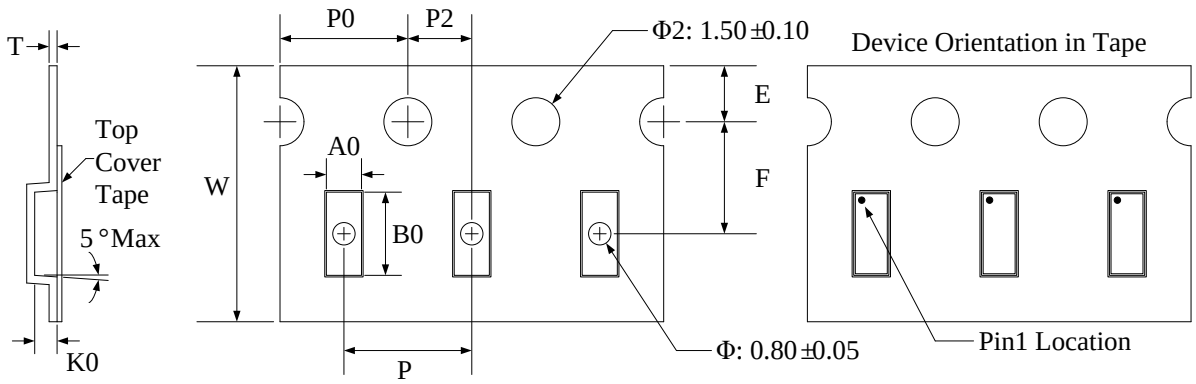
Notes: All dimension in millimeter and exclude mold flash & metal burr.

PCB Layout Pattern



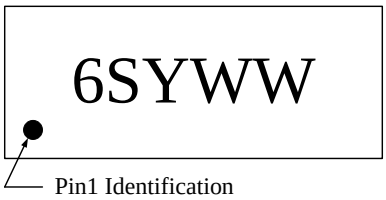
DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(0.034)	(0.875)
G	0.008	0.20
P	0.020	0.50
P1	0.039	1.00
X	0.008	0.20
X1	0.016	0.40
Y	0.027	0.675
Y1	(0.061)	(1.55)
Z	0.061	1.55

Tape and Reel Specification



Symbol	W	A0	B0	K0	E	F	P	P0	P2	T
Dimensions (mm)	8.00+0.3 -0.1	1.23 ±0.05	2.7 ±0.05	0.7 ±0.05	1.75 ±0.1	3.5 ±0.05	4.0 ±0.1	4.0 ±0.1	2.0 ±0.05	0.25 ±0.02

Marking Codes



Ordering Information

Part Number	Working Voltage	Quantity Per Reel	Reel Size
SYT06U05DVC	5V	3,000	7 Inch

Note:

(1) "6S" is part number, while "YWW" is date code.

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