Application Notes: AN_SY6014

Analog Class-D Audio IC with EMI Suppression

General Description

The SY6014 is an analog Class-D audio power amplifier. It has filterless operation control strategy which eliminates the LC filter for each channel to reduce the size of final product and the cost of mass production. It has high conversion efficiency for driving two bridge-tied stereo speakers with no need for an external heat sink when playing music. The spread spectrum operation mode is achieved internally to improve the EMI performance. The amplifier gain of SY6014 in audible bandwidth is selectable by the external pin. Output power limit is adjustable to limit the power consumption on speaker. Low-power shutdown mode is available. Fully short protection at output side against shorts to GND, V_{DD} and out-to-out is achieved with auto recovery capability.

Ordering Information

SY6014 □(□□)□

- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY6014QCC	QFN4×4-24	----

Features

- 2×7W into 8Ω BTL Loads @1% THD+N From a 12V Supply
- 2×4W into 8Ω BTL Loads @10% THD+N From an 8V Supply
- 2×2.3W into 8Ω BTL Loads @10% THD+N From a 6V Supply
- Operates From 5.5V to 16V
- Filterless/Filter Operation
- Adjustable Power Limit
- Spread-Spectrum Modulation for Good EMI Performance
- High PSRR
- High Efficiency Class-D Operation Eliminates Need for Heat Sinks
- Four Fixed-gain Controlled: 20dB, 26dB, 32dB and 36dB
- Internal Oscillator (No External Components Required)
- Thermal and Short-Circuit Protection With Auto Recovery
- Comprehensive Click and Pop Suppression
- Space-saving Surface Mount QFN4×4-24 Package

Applications

- Flat Panel Display TVs, DLP®TVs, CRT TVs
- Powered Speakers
- Music Instruments
- Boom Box
- DVD Players, Game Machines

Typical Application

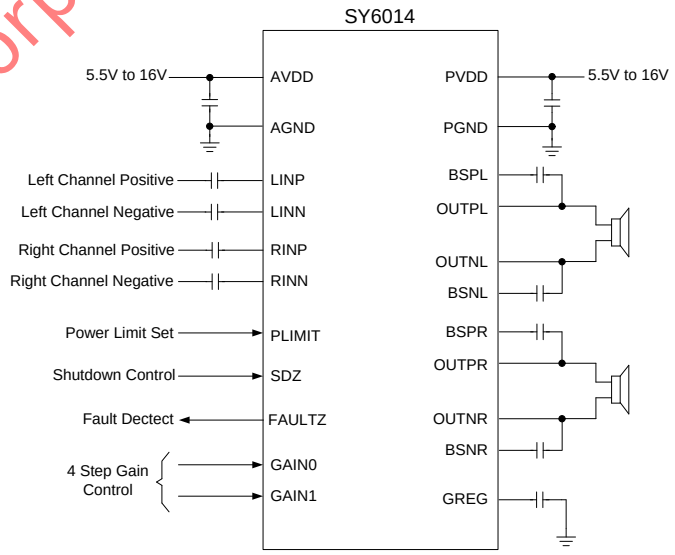
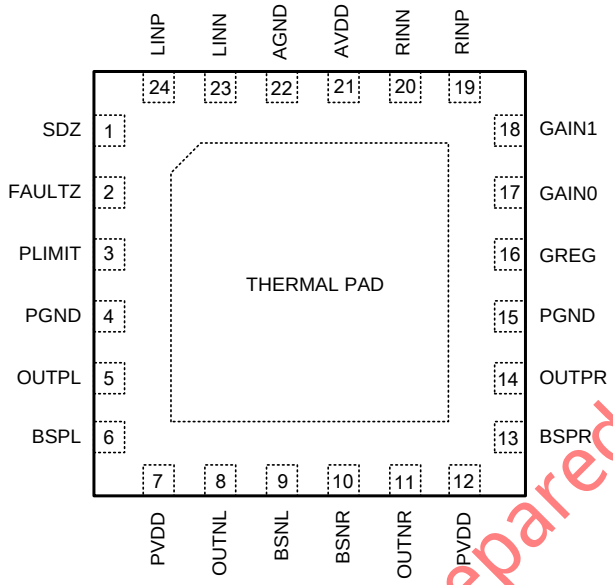


Figure1. Typical Application Circuit

Pinout (top view)



Top mark: **BDP*xyz*** (Device code: BDP, ***x=year code, y=week code, z= lot number code***)

Name	Number	Description
SDZ	1	Shutdown signal for IC (low=disabled, high=operational). TTL logic levels with compliance to AVDD.
FAULTZ	2	Open drain output used to display short circuit. Voltage compliant to AVDD. Short circuit faults can be set to auto-recovery by connecting this pin to SDZ pin.
PLIMIT	3	Power limit level adjust. Connect a resistor divider from GREG to GND to set power limit. Connect directly to GREG for no power limit.
PGND	4	Power ground.
OUTPL	5	Class-D H-bridge positive output for left channel.
BSPL	6	Bootstrap I/O for left positive channel.
PVDD	7	Power supply.
OUTNL	8	Class-D H-bridge negative output for left channel.
BSNL	9	Bootstrap I/O for left negative channel.
BSNR	10	Bootstrap I/O for right negative channel.
OUTNR	11	Class-D H-bridge negative output for right channel.
PVDD	12	Power supply.
BSPR	13	Bootstrap I/O for right positive channel.
OUTPR	14	Class-D H-bridge positive output for right channel.
PGND	15	Power ground.
GREG	16	Gate drive supply. Nominal voltage is 3.4V.
GAIN0	17	Gain select least-significant bit. TTL logic levels with compliance to AVDD.
GAIN1	18	Gain select most-significant bit. TTL logic levels with compliance to AVDD.
RINP	19	Positive audio input for right channel. Biased at 1.7V.
RINN	20	Negative audio input for right channel. Biased at 1.7V.
AVDD	21	Analog power supply. Not internally connected to PVDD.
AGND	22	Analog ground.
LINN	23	Negative audio input for left channel. Biased at 1.7V.
LINP	24	Positive audio input for left channel. Biased at 1.7V.
Thermal Pad	25	Connect to GND for best system performance. If not connected to GND, leave floating.

Function Block

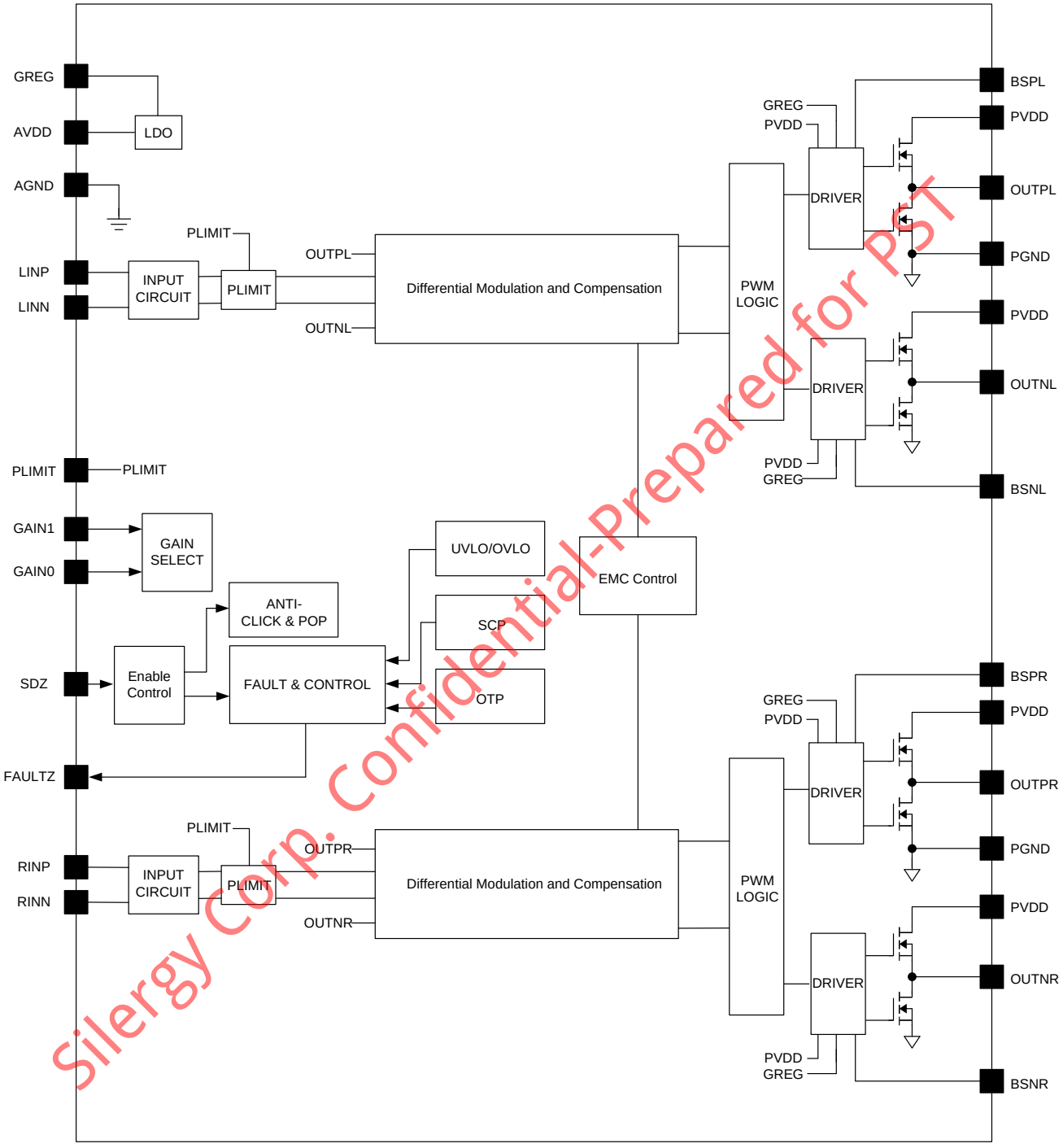


Figure2. Block Diagram

Absolute Maximum Ratings (Note 1)

AVDD, PVDD (Note 2) ---------- 18V
RIN, LIN ---------- 3.6V
SDZ, GAIN1, GAIN0 ---------- (AVDD+0.3)V
PLIMIT ---------- (GREG+0.3)V
Minimum Load Resistance Output Configuration ---------- 6Ω
Junction Temperature Range ---------- -40℃ to 150℃
Storage Temperature Range ---------- -40℃ to 125℃
Package Thermal Resistance
θ_{JA} (Note 3) ---------- 70℃/W
θ_{JC} ---------- 35℃/W

Recommended Operating Conditions

Supply Voltage Range ---------- 5.5V to 16V
Junction Temperature Range ---------- -40℃ to 125℃
Ambient Temperature Range ---------- -40℃ to 85℃

Electrical Characteristics

(T_A =25℃, V_{DD}=12V, R_L=8Ω, Gain=26dB, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
DC Characteristics						
AVDD, PVDD	V_{DD}		5.5		16	V
Quiescent Supply Current	I_Q	SDZ=1, no load or filter (Note 4)		10.7		mA
		SDZ=0, no load or filter		62	82	μA
High-level Input Voltage	V_{IH}	SDZ, GAIN1, GAIN0	2.05			V
Low-level Input Voltage	V_{IL}	SDZ, GAIN1, GAIN0			0.65	V
Low-level Output Voltage (Note 4)	V_{OL}	FAULTZ, $R_{PULL-UP}$=100kΩ, PVDD=16V		0.63		V
High-level Input Current	I_{IH}	GAIN1, GAIN0, V_I= 2V	-0.1		0.1	μA
		SDZ, V_I= 2V	1	3	4	μA
Drain-source On-state Resistance	$R_{DS(ON)}$			300		mΩ
Gain	G	GAIN0=0, GAIN1=0, No Load	19	20	21	dB
		GAIN0=1, GAIN1=0, No Load	25	26	27	
		GAIN0=0, GAIN1=1, No Load	31	32	33	
		GAIN0=1, GAIN1=1, No Load	35	36	37	
Turn-on Time (Note 4)	t_{ON}	SDZ=1		24		ms
Turn-off Time (Note 4)	t_{OFF}	SDZ=0		1		μs
Output Offset Voltage	$\|V_{OS}\|$	V_I=0V, Measured Differentially at VDD=6V		1.5	15	mV
Gate Drive Supply	GREG	SDZ=1, V_I=0V	3.2	3.4	3.6	V
Output Voltage Maximum under PLIMIT Control	V_O	V_{PLIMIT}=1V, V_I=0.5V_P, f=1kHz, SE input	13.5	15.5	17.5	V_{PP}
PWM Frequency (Note 4)	f_{PWM}			350		kHz
AC Characteristics (Note 4)						
Output Integrated Noise	V_n	20Hz to 22kHz, A-weighted filter, Gain=20dB		70		μV

Signal to Noise Ratio	SNR	Max output at THD+N<1%, V_{DD}=6V,f=1kHz,Gain=20dB, A-weighted		94		dB
		Max output at THD+N<1%, V_{DD}=8V,f=1kHz,Gain=20dB, A-weighted		97		
		Max output at THD+N<1%, V_{DD}=12V,f=1kHz,Gain=20dB, A-weighted		100.5		
Total Harmonic Distortion +Noise	THD+N	V_{DD}=6V, f=1kHz, Po=0.5W		0.05		%
		V_{DD}=6V, f=1kHz, Po=1W		0.055		
		V_{DD}=8V, f=1kHz, Po=1W		0.05		
		V_{DD}=8V, f=1kHz, Po=1.6W		0.055		
		V_{DD}=12V, f=1kHz, Po=1W		0.05		
		V_{DD}=12V, f=1kHz, Po=3.5W		0.05		
Output Power	P_O	V_{DD}=6V, f=1kHz, 1% THD+N		1.85		W
		V_{DD}=6V, f=1kHz, 10% THD+N		2.3		
		V_{DD}=8V, f=1kHz, 1% THD+N		3.25		
		V_{DD}=8V, f=1kHz, 10% THD+N		4		
		V_{DD}=12V, f=1kHz, 1% THD+N		7		
Crosstalk		Vo=1Vrms, f=1kHz, Gain=20dB		-90		dB
Power Supply Rejection Ratio	PSRR	200mV_{PP} ripple, f=1kHz , Gain=20dB		-60		dB
Protection						
V_{DD} Under Voltage Lockout Voltage	V_{UVLO_RISE}	V_{DD} Rising		5.25	5.5	V
	V_{UVLO_FALL}	V_{DD} Falling	4.75	5		V
V_{DD} Over Voltage Lockout Voltage	V_{OVLO_RISE}	V_{DD} Rising		21	22	V
	V_{OVLO_FALL}	V_{DD} Falling	16.9	17.7		V
Short Circuit Protection Current Limit**(Note 4)**	I_{SC}			4		A
Thermal Shutdown Temperature**(Note 4)**	T_{SD}			135		℃
Thermal Shutdown Hysteresis**(Note 4)**	T_{HYS}			30		℃

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: DC voltage rating could be derated a little according to the possible switching spike on switching node if the snubber is not appropriate enough.

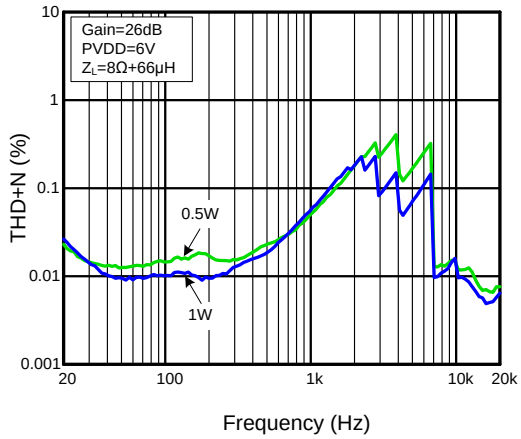
Note 3: θ_{JA} is measured in the natural convection at T_A=25℃ on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 4: Typical value tested on demonstration board is guaranteed by design.

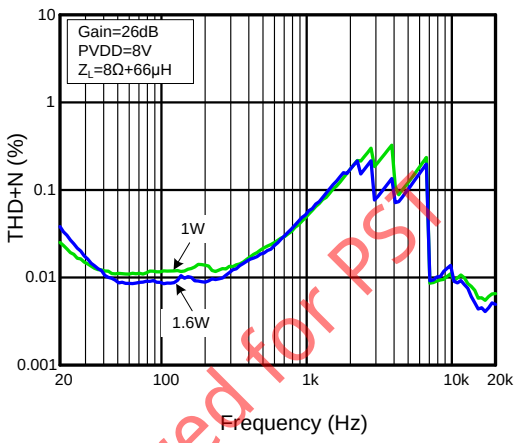
Typical Performance Characteristics

(All measurements taken at 1kHz, unless otherwise noted.)

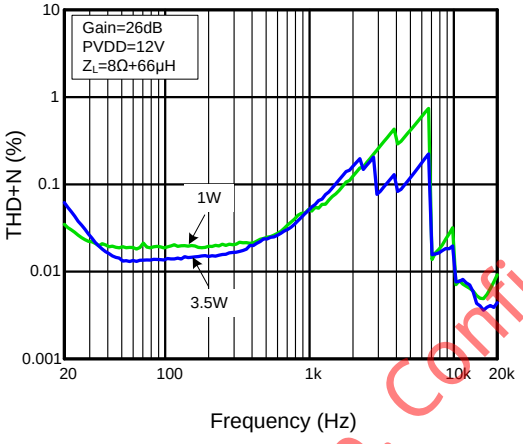
THD+N vs. Frequency



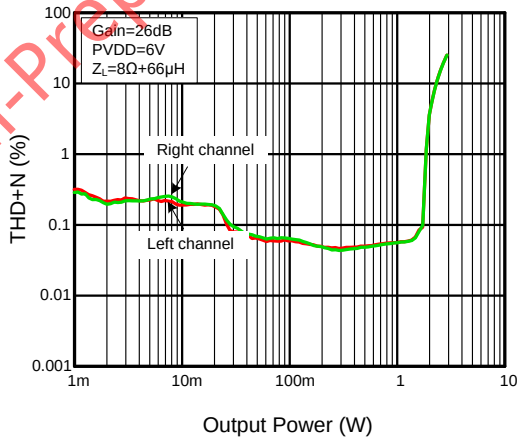
THD+N vs. Frequency



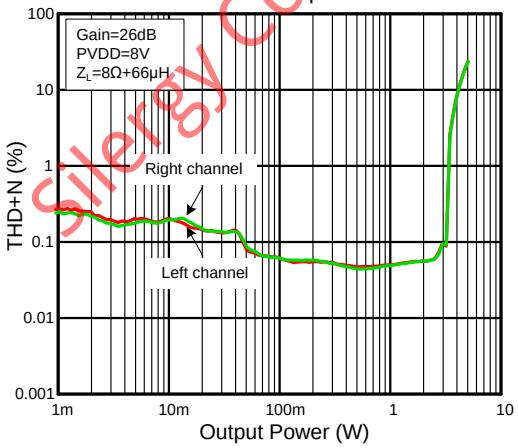
THD+N vs. Frequency



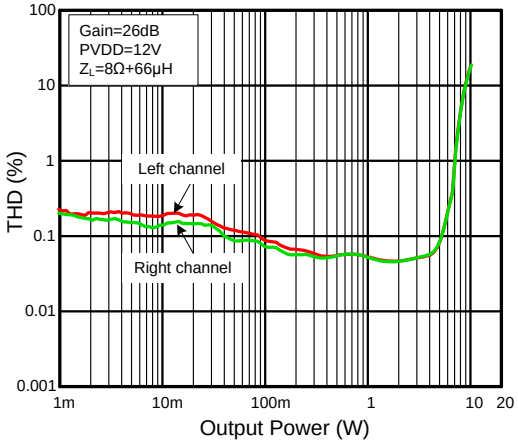
THD+N vs. Output Power

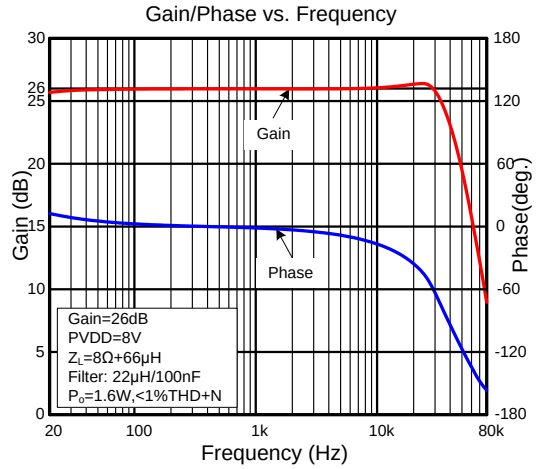


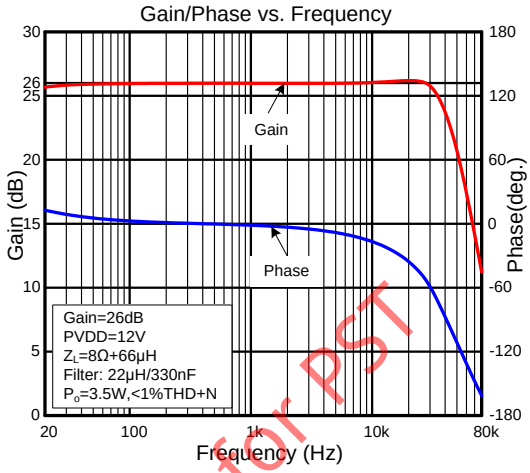
THD+N vs. Output Power

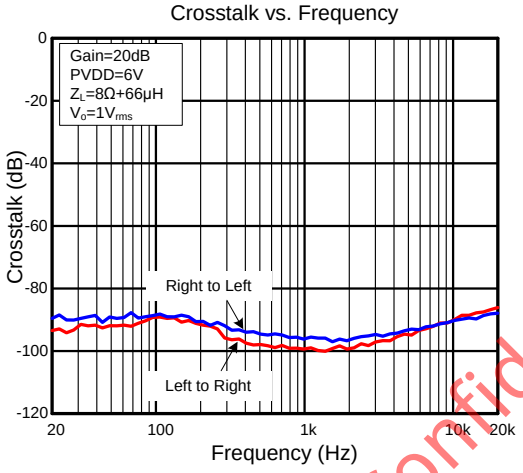


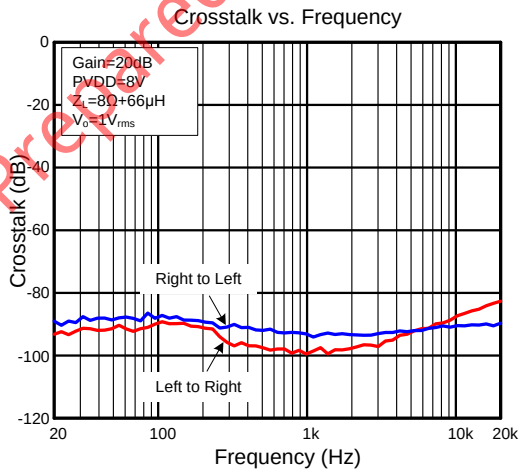
THD vs. Output Power

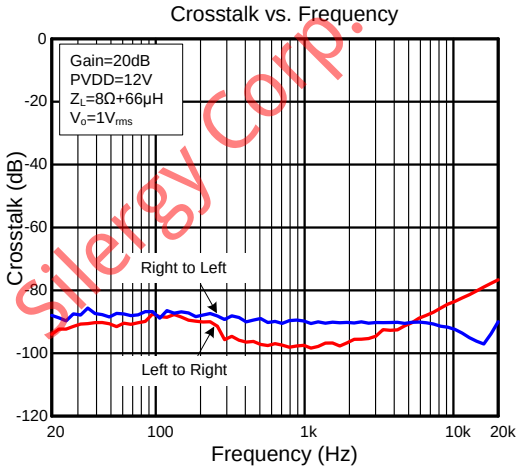


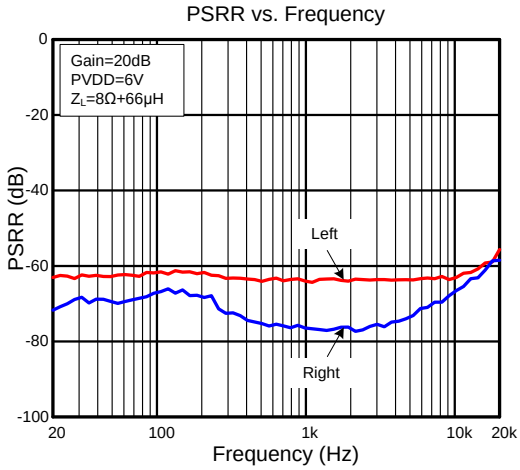


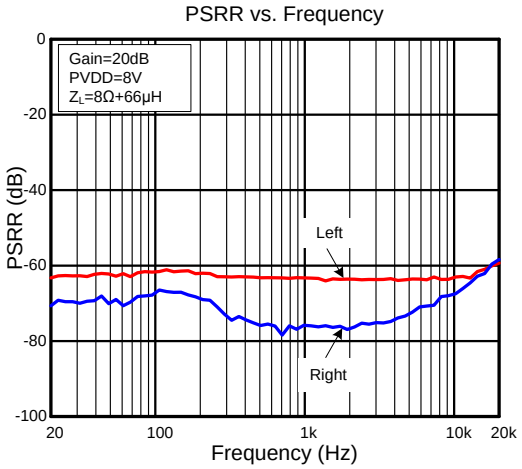


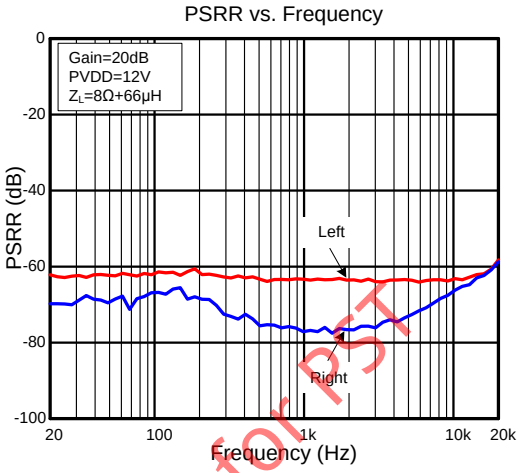


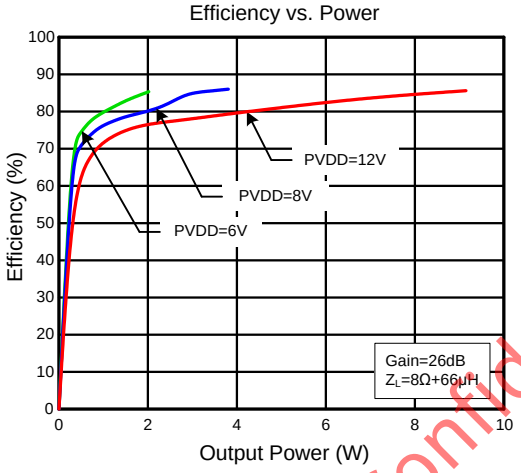












Function Description

This section focuses on the description of SY6014 Class-D function block operation.

Gain Setting

The gain of the SY6014 is set by two input terminals, GAIN0 and GAIN1.The programmable gain is listed in Table 1.

Table1. Gain Setting

GAIN1	GAIN0	Typical Amplifier Gain (dB)
0	0	20
0	1	26
1	0	32
1	1	36

Modulation Scheme

The SY6014 uses BD mode modulation scheme that allows operation without the classic LC reconstruction filter when the Class-D is driving an inductive load, see as Figure 3. Each output is switching from 0V to the supply voltage. The OUTP and OUTN are in phase with each other with no input so that there is little or no current in the speaker. The duty cycle of OUTP is greater than 50% and OUTN is less than 50% for positive output voltages. The duty cycle of OUTP is less than 50% and OUTN is greater than 50% for negative output voltages. The voltage across the load sits at 0V throughout most of the switching period, greatly reducing the switching current, which reduces any I^2R losses in the load.

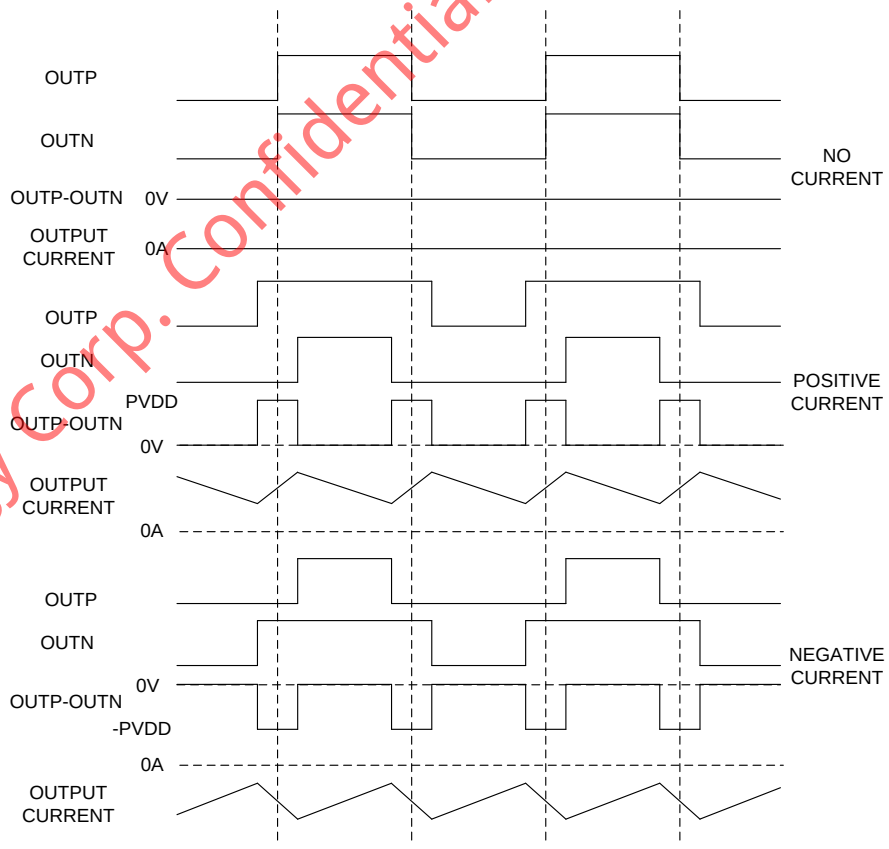


Figure3. BD Modulation

Spread Spectrum Mode

The SY6014 employs a unique spread spectrum mode (SSM) that flattens the wideband spectral components, improving EMI emissions that may be radiated by the speaker and cables.

The switching frequency varies near randomly by using pseudorandom modulation method (PRM), which is accomplished by M-Sequence. The frequency varies typically from 300kHz to 450kHz and the minimum frequency step is 3.5kHz. Instead of a large amount of spectral energy present at multiples of the switching frequency, the energy is now spread over a bandwidth that increases with frequency. Above a few MHz, the wideband spectrum looks like white noise for EMI purposes. A proprietary amplifier topology ensures this does not corrupt the noise floor in the audio bandwidth.

PLIMIT

The PLIMIT circuit sets a limit on the output peak-to-peak voltage. The limiting is done by limiting the duty cycle to a fixed maximum value. This limit can be thought of as a "virtual" voltage rail which is lower than the supply connected to PVDD. For single ended inputs, this "virtual" rail is approximately 7.5 times of the voltage at the PLIMIT pin; for differential inputs, this "virtual" rail is approximately 15 times of the voltage at the PLIMIT pin. This output voltage can be used to calculate the maximum output power for a given maximum input voltage and speaker impedance.

Increasing the PLIMIT voltage from a given value increases the maximum output voltage swing until it equals PVDD. Add a resistor divider from GREG to ground to set the voltage at the PLIMIT pin. An external reference may also be used if tighter tolerance is required. Also add a 1μF capacitor from PLIMIT pin to ground. Adjusting PLIMIT to a higher value will disable the PLIMIT function and will offer highest available output power, however for SY6014 it is always advised to use the PLIMIT function if PVDD is higher than nominal value to prevent shutdown due to over current protection. If PLIMIT is disabled on SY6014 an over current shutdown can occur with minimum recommended load impedance when PVDD is higher than its nominal value. To disable the PLIMIT function, it is recommended to connect PLIMIT pin to GREG.

The output voltage can be used to calculate the maximum output power for a given maximum input voltage and speaker impedance, shown as Equation (1).

$$P_{OUT} = \frac{\left(\left(\frac{R_L}{R_L + 2 \cdot R_S}\right) \cdot V_P\right)^2}{2 \cdot R_L} \quad \text{for unclipped power} \qquad (1)$$

Where

- R_S is the total series resistance including $R_{DS(ON)}$, and any resistance in the output filter.
- R_L is the load resistance.
- V_P is the peak amplitude of the output possible within the supply rail.

$$V_P = \begin{cases} 7.5 \cdot \text{PLIMIT voltage for SE input if } V_P < \text{PVDD.} \\ 15 \cdot \text{PLIMIT voltage for differential input if } V_P < \text{PVDD.} \end{cases}$$

- P_{OUT} (10% THD+N) = 1.25·P_{OUT} (unclipped).

Input Capacitor, C_I

In the typical application, input capacitor C_I is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case C_I and the input impedance of the amplifier (Z_I) form a high-pass filter with the corner frequency determined in Equation 2.

$$f_c = \frac{1}{2\pi \cdot Z_I \cdot C_I} \qquad (2)$$

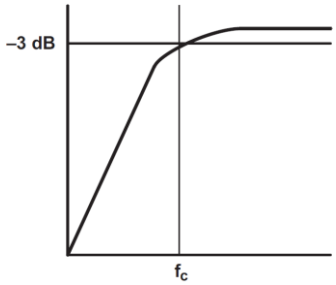


Figure4. -3dB frequency of HPF

The value of C_I is important, as it directly affects the bass (low-frequency) performance of the circuit. The input resistance of the SY6014 value is fixed at 16kΩ ±20%, Consider the specification calls for a flat bass response down to 20Hz. Equation 2 is reconfigured as Equation 3.

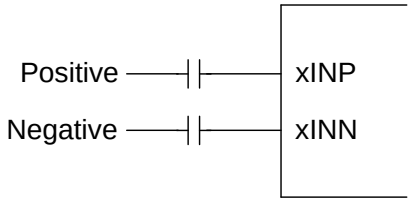
$$C_I = \frac{1}{2\pi \cdot Z_I \cdot f_c} \qquad (3)$$

In this example, C_I is 0.5μF; so, one would likely choose a value of 1μF as this value is commonly used. A further consideration for this capacitor is the leakage path from the input source through the input network, C_I, and the feedback network to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high-gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at 1.7V, which is likely higher than the source dc level. Note that it is important to confirm the capacitor polarity in the application. Additionally, lead-free solder can create dc offset voltages, and it is important to ensure that boards are cleaned properly.

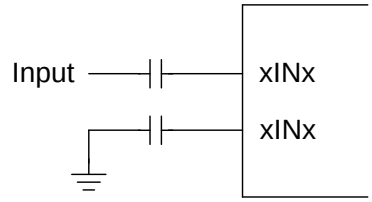
Differential Inputs

The differential input stage of the amplifier cancels any noise that appears on both input lines of the channel. To use the SY6014 with a differential source, connect the positive lead of the audio source to the INP input and the negative lead from the audio source to the INN input. To use the SY6014 with a single-ended source, ac ground the INP or INN input through a capacitor equal in value to the input capacitor on INN or INP and apply the audio source to either input. In a single-ended input application, the unused input should be ac grounded at the audio source instead of at the device input for best noise performance. For good transient performance, the impedance seen at each of the two differential inputs should be the same. The input signal connection is shown as Figure 5.

The impedance seen at the inputs should be limited to an RC time constant to allow the input dc blocking capacitors to become completely charged during the 24ms power-up time. If the input capacitors are not allowed to completely charge, there will be some additional sensitivity to component matching which can result in pop if the input components are not well matched.



(a) Differential Input



(b) Single-ended Input

Figure5. Input Signal Connection

BSN and BSP

The half H-bridge output stages use only NMOS transistors. Therefore, they require bootstrap capacitors for the high side of each output to turn on correctly. A 220nF ceramic capacitor, rated for at least 16V, must be connected from each output to its corresponding bootstrap input. Specifically, one 220nF capacitor must be connected from OUTP to BSP, and one 220nF capacitor must be connected from OUTN to BSN.

The bootstrap capacitors connected between the BSXX pins and their corresponding outputs function as a floating power supply for the high-side N-channel power MOSFET gate-drive circuitry. During each high-side switching cycle, the bootstrap capacitors hold the gate-to-source voltage high enough to keep the high-side MOSFETs turned on.

SDZ Operation

The SY6014 employs a shutdown mode of operation designed to reduce supply current to the absolute minimum level during periods of nonuse for power conservation. The SDZ input terminal should be held high (see specification table for trip point) during normal operation when the amplifier is in use. Pulling SDZ low causes the outputs to mute and the amplifier to enter a low-current state. Never leave SDZ unconnected, because amplifier operation would be unpredictable.

For the best power-up pop performance, place the amplifier in the shutdown mode prior to applying the power supply voltage.

Efficiency: LC Filter Required With the Traditional Class-D Modulation Scheme

The main reason that the traditional Class-D amplifier needs an output filter is that the switching waveform results in maximum current flow. This causes more loss in the load, which causes lower efficiency. The ripple current is large for the traditional modulation scheme, because the ripple current is proportional to voltage multiplied by the time at that voltage. The differential voltage swing is $2\times V_{DD}$, and the time at each voltage is half the period for the traditional modulation scheme. An ideal LC filter is needed to store the ripple current from each half cycle for the next half cycle, while any resistance causes power dissipation. The speaker is both resistive and reactive, whereas an LC filter is almost purely reactive.

The SY6014 modulation scheme has little loss in the load without a filter because the pulses are short and the change in voltage is V_{DD} instead of $2\times V_{DD}$. As the output power increases, the pulses widen, making the ripple current larger. Ripple current could be filtered with an LC filter for increased efficiency, but for most applications the filter is not needed.

An LC filter with a cutoff frequency less than the Class-D switching frequency allows the switching current to flow through the filter instead of the load. The filter has less resistance but higher impedance at the switching frequency than the speaker, which results in less power dissipation, therefore increasing efficiency. Figure 6 is the typical LC filter structure.

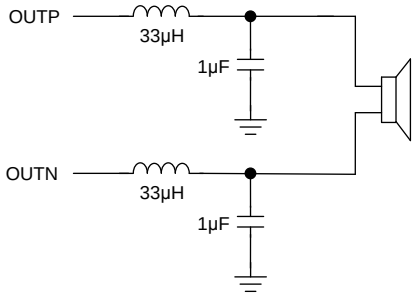


Figure6. Typical LC Output Filter, Cutoff Frequency is 27kHz, Speaker Resistor = 8Ω

Ferrite Bead Filter Considerations

Using the edge rate control method in the SY6014 amplifier it is possible to design a high efficiency Class-D audio amplifier while minimizing interference to surrounding circuits. It is also possible to accomplish this with only a low-cost ferrite bead filter. In this case it is necessary to carefully select the ferrite bead used in the filter.

One important aspect of the ferrite bead selection is the type of material used in the ferrite bead. Not all ferrite material is alike, so it is important to select a material that is effective in the 10MHz to 100MHz range which is the key to the operation of the Class-D amplifier. Many of the specifications regulating consumer electronics have emissions limits as low as 30MHz. It is important to use the ferrite bead filter to block radiation in the 30MHz and above range from appearing on the speaker wires and the power supply lines which are good antennas for these signals. The impedance of the ferrite bead can be used along with a small capacitor with a value in the range of 1nF to reduce the frequency spectrum of the signal to an acceptable level. For best performance, the resonant frequency of the ferrite bead/ capacitor filter should be less than 10MHz.

Also, it is important that the ferrite bead is large enough to maintain its impedance at the peak currents expected for the amplifier. Some ferrite bead manufacturers specify the bead impedance at a variety of current levels. In this case it is possible to make sure the ferrite bead maintains an adequate amount of impedance at the peak current the amplifier will see. If these specifications are not available, it is also possible to estimate the bead current handling capability by measuring the resonant frequency of the filter output at very low power and at maximum power. A change of resonant frequency of less than fifty percent under this condition is desirable.

A high quality ceramic capacitor is also needed for the ferrite bead filter. A low ESR capacitor with good temperature and voltage characteristics will work best.

Additional EMC improvements may be obtained by adding snubber networks from each of the class D outputs to ground. Suggested values for a simple RC series snubber network would be 10Ω in series with a 470pF capacitor although design of the snubber network is specific to every application and must be designed taking into account the parasitic reactance of the printed circuit board as well as the audio amp. Take care to evaluate the stress on the component in the snubber network especially if the amp is running at high PVDD. Also, make sure the layout of the snubber network is tight and returns directly to the PGND. The typical ferrite bead filter is shown as Figure 7.

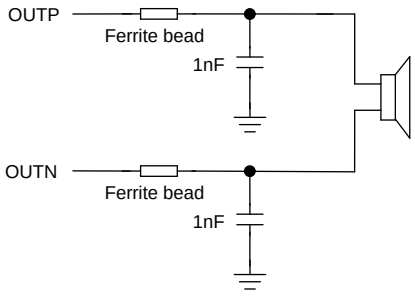


Figure7. Typical Ferrite Bead EMI Filter

When to Use an Output Filter for EMI Suppression

There may be a few circuit instances where it is necessary to add a complete LC reconstruction filter. These circumstances might occur if there are nearby circuits which are very sensitive to noise. In these cases a classic second order Butterworth filter similar to those shown in the figures above can be used.

Some systems have little power supply decoupling from the AC line but are also subject to line conducted interference (LCI) regulations. These include systems powered by "wall warts" and "power bricks." In these cases, it LC reconstruction filters can be the lowest cost means to pass LCI tests. Common mode chokes using low frequency ferrite material can also be effective at preventing line conducted interference.

Protection Circuits

The device is fully protected against short circuit, over temperature, over voltage and under voltage. The FAULTZ pin will signal if an short circuit error is detected.

Short Circuit Protection (SCP)

The SY6014 has short circuit protection against load is shorted or exceeded. The short circuit protection fault is reported on the FAULTZ pin as a low state. The amplifier outputs are switched to a Hi-Z state when the short circuit protection latch is engaged. The latch can be cleared by cycling the SDZ pin through the low state.

If automatic recovery from the short circuit protection latch is desired, connect the FAULTZ pin directly to the SDZ pin. This allows the FAULTZ pin function to automatically drive the SDZ pin low which clears the short-circuit protection latch.

Under Voltage Lockout (UVLO) and Over Voltage Lockout (OVLO)

If at any time the voltage on the PVDD pin falls below the under voltage or rises above over voltage lockout threshold voltage, all circuitry in the device is disabled and internal logic is reset. Operation resumes when PVDD rises above the UVLO threshold with hysteresis or falls below OVLO threshold with hysteresis.

Over Temperature Protection (OTP)

Thermal protection on the SY6014 prevents damage to the device when the internal die temperature exceeds 135℃. There is a ±15℃ tolerance on this trip point from device to device. Once the die temperature exceeds the thermal set point, the device enters into the shutdown state and the outputs are disabled. This is not a latched fault. The thermal fault is cleared once the temperature of die is reduced by 30℃.

Power Supply Recommendations

The power supply requirements for the SY6014 consist of one higher-voltage supply to power the output stage of the speaker amplifier. Several on-chip regulators are included on the SY6014 to generate the voltages necessary for the internal circuitry of the audio path. It is important to note that the voltage regulators which have been integrated are sized only to provide the current necessary to power the internal circuitry. The external pins are provided only as a connection point for off-chip bypass capacitors to filter the supply. Connecting external circuitry to these regulator outputs may result in reduced performance and damage to the device. The high voltage supply, between 5.5V and 16V, supplies the analog circuitry

(AVDD) and the power stage (PVDD). The AVDD supply feeds the internal LDO.

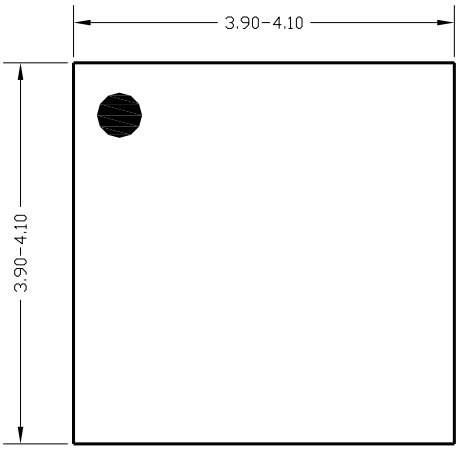
The SY6014 is a high-performance CMOS audio amplifier that requires adequate power-supply decoupling to ensure that the output total harmonic distortion (THD) is as low as possible. Power-supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power-supply leads. For higher-frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1µF to 1µF, placed as close as possible to the device V_{DD} lead works best. For filtering lower frequency noise signals, a larger aluminum electrolytic capacitor of 220µF or greater placed near the audio power amplifier is recommended. The 220µF capacitor also serves as local storage capacitor for supplying current during large signal transients on the amplifier outputs. The PVDD terminals provide the power to the output transistors, so a 220µF or larger capacitor should be placed on each PVDD terminal. A 10µF capacitor on the AVDD terminal is adequate. These capacitors must be properly checked for voltage and ripple-current rating to ensure reliability.

Printed Circuit Board (PCB) Layout

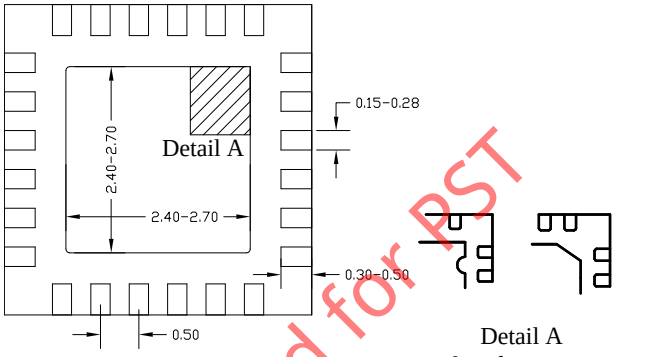
The SY6014 can be used with a small, inexpensive ferrite bead output filter for most applications. However, since the Class-D switching edges are fast, it is necessary to take care when planning the layout of the printed circuit board. The following suggestions will help to meet EMC requirements.

- Decoupling capacitors—the high-frequency decoupling capacitors should be placed as close to the PVDD and AVDD terminals as possible. Large (220µF or greater) bulk power supply decoupling capacitors should be placed near the SY6014 on the PVDD supplies. Local, high-frequency bypass capacitors should be placed as close to the PVDD pins as possible. These capacitors can be connected to the IC ground pad directly for an excellent ground connection. Consider adding a small, good quality low ESR ceramic capacitor between 220pF and 1000pF and a larger mid-frequency cap of value between 0.1µF and 1µF also of good quality to the PVDD connections at each end of the chip.
- Keep the current loop from each of the outputs through the ferrite bead and the small filter cap and back to PGND as small and tight as possible. The size of this current loop determines its effectiveness as an antenna.
- Grounding—the AVDD decoupling capacitor should be grounded to analog ground (AGND). The PVDD decoupling capacitors should connect to PGND. Analog ground and power ground should be connected at the thermal pad, which should be used as a central ground connection or star ground for the SY6014.
- Output filter—the ferrite EMI filter should be placed as close to the output terminals as possible for the best EMI performance. The LC filter should be placed close to the outputs. The capacitors used in both the ferrite and LC filters should be grounded to power ground.
- Thermal pad—the thermal pad must be soldered to the PCB for proper thermal performance and optimal reliability. The dimensions of the thermal pad and thermal land should be as large as possible. Solid vias should be equally spaced underneath the thermal land. The vias should connect to a solid copper plane, either on an internal layer or on the bottom layer of the PCB.

QFN4×4-24 Package Outline & PCB Layout

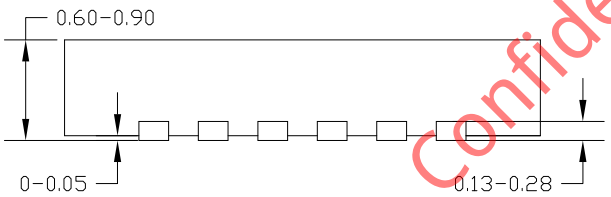


Top View

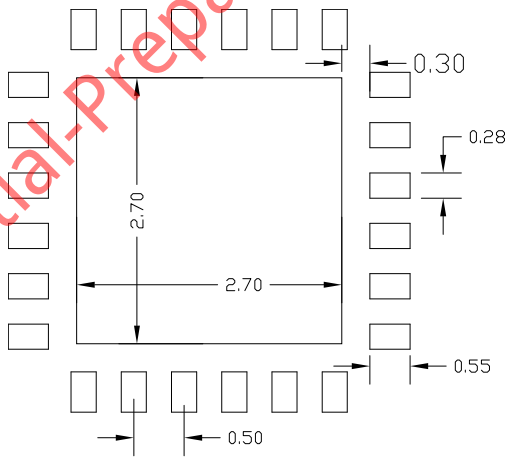


Bottom View

Detail A
Pin1 identifier: two options



Side View



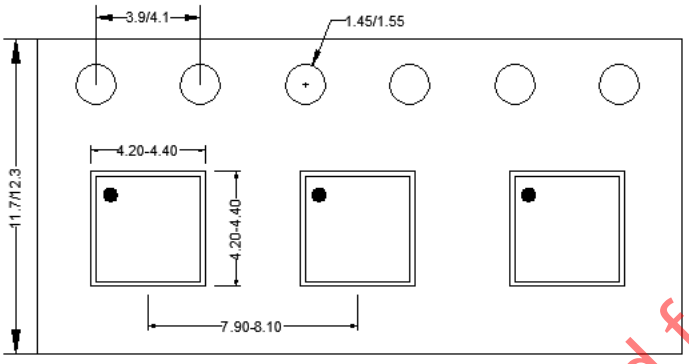
PCB Layout (Recommended)

Notes: All dimension in millimeter and exclude mold flash & metal burr.

Taping & Reel Specification

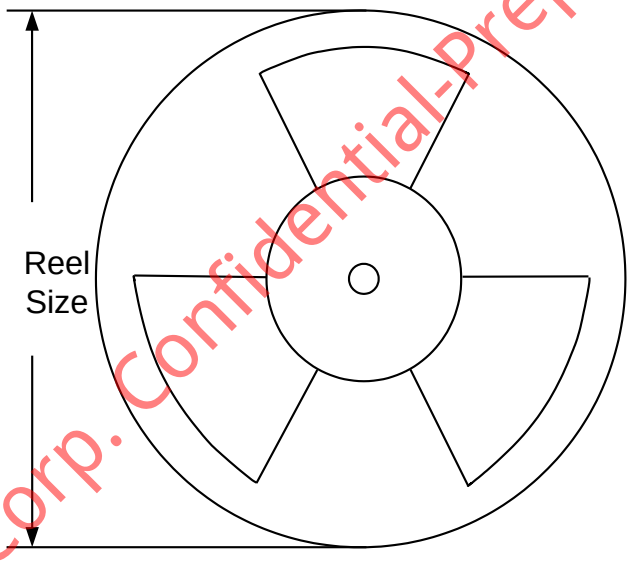
1. Taping orientation

QFN4×4



Feeding direction →

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN4×4	12	8	13"	400	400	5000

3. Others: NA

单击下面可查看定价，库存，交付和生命周期等信息

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