

SWR10P10

100V Single P-Channel Enhancement-Mode MOSFET

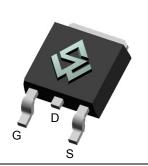
General Description

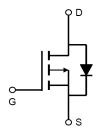
- Low gate charge.
- Uses advanced trench process technology.
- Use in PWM applications

Product Summary

- BV_{DSS} -100V
- $R_{DS(on)}$ @VGS = -10V < 220m Ω
- $R_{DS(on)}$ @VGS = -4.5V < 255m Ω

TO-252 D-PAK





Absolute Maximum Ratings (T_A = 25°C unless otherwise noted)

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	-100	>
Gate-Source Voltage	V_{GS}	±20	>
Drain Current (T _A =25°C)		-15	Α
Drain Current (T _A =75°C)	I _D	-8	Α
Pulsed Drain Current ^a	I _{DM}	-30	Α
Power Dissipation ^b (T _C =25°C)		10	W
Power Dissipation ^b (T _A =25°C)	P _D	2.5	W
Junction and Storage Temperature Range	T _{J,} T _{STG}	-55 ~ +150	°C

Thermal Characteristics

Parameter	Symbol	Maximum	Units
Junction-to-Ambient ^a (t ≤ 10s)	D	25	°C/W
Junction-to-Ambient ^{a,d} (Steady-State)	$R_{ heta JA}$	50	°C/W
Junction-to-Lead (Steady-State)	$R_{ heta JL}$	5	°C/W



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Symbol	Parameter	Conditions	Min	Тур	Max	Units
Off Char	acteristics					
BV_{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0V , I _D = -250uA	-100			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = -100V , V _{GS} = 0V			-1	uA
I_{GSS}	Gate-Body Leakage Current	$V_{GS} = \pm 20V, V_{DS} = 0V$			±100	nA
On Char	acteristics					
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = -250uA$	-2		-4	V
	Drain-Source On-State Resistance	V _{GS} = -10V , I _D = -7.8A		180	220	mΩ
R _{DS(ON))}		V _{GS} = -4.5V , I _D = -6A		210	255	mΩ
g FS	Forward Transconductance	$V_{DS} = -10V$, $I_{D} = -7.8A$		20		S
Drain-So	urce Diode Characteristics					
V_{SD}	Diode Forward Voltage	V _{GS} = 0V , I _S = -10A			-1.3	٧
Is	Maximum Body-Diode Continuous Current				-10	Α
Dynamic	Characteristics					
C _{iss}	Input Capacitance			1096		pF
Coss	Output Capacitance	$V_{DS} = -30V$, $V_{GS} = 0V$ f = 1.0MHz		72		pF
C _{rss}	Reverse Transfer Capacitance	1.00012		43		pF
Switchin	g Characteristics					
Q_g	Total Gate Charge	$V_{DS} = -50V$, $I_{D} = -7.8A$ $V_{GS} = -10V$		20.9		nC
Q_gs	Gate-Source Charge			4.5		nC
Q_{gd}	Gate-Drain Charge			5.3		nC
$t_{D(ON})$	Turn-On Delay Time			12		ns
t _r	Turn-On Rise Time	$V_{DD} = -30V$, ID = -1A $V_{GS} = -10 V$ $R_{GEN} = -3 \text{ ohm}$		11		ns
t _{D(OFF)}	Turn-Off Delay Time			56		ns
t _f	Turn-Off Fall Time			32		ns

a. Repetitive rating, Pulse width limited by junction temperature $T_{J(MAX)}$ =150 °C. Ratings are based on low frequency and duty cycles to keep initial T_J =25 °C

b. The power dissipation P_D is based on $T_{J(MAX)}$ =150 $^{\circ}C$, using \leqslant 10s junction-to-ambient thermal resistance.

c. The value of $R_{\theta JA}$ is measured with the device mounted on $1in^2$ FR-4 board with 2oz. Copper, in a still air environment with T_A = 25°C. The value in any given application depends on the user's specific board design.

d. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.



Typical Characteristics

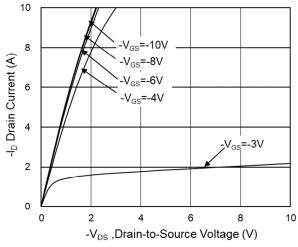


Fig.1 Typical Output Characteristics

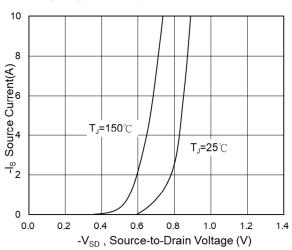


Fig.3 Source Drain Forward Characteristics

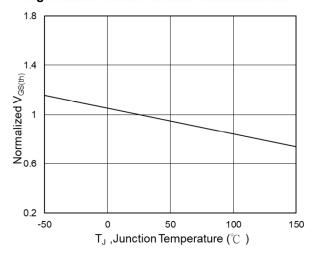


Fig.5 Normalized $V_{GS(th)}$ vs T_J

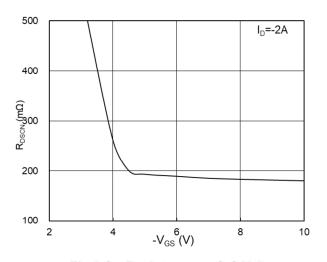


Fig.2 On-Resistance vs G-S Voltage

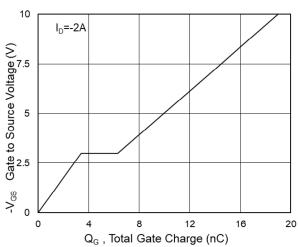


Fig.4 Gate-Charge Characteristics

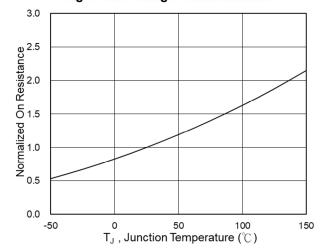
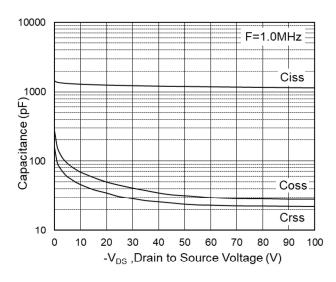


Fig.6 Normalized R_{DSON} vs T_J



Typical Characteristics



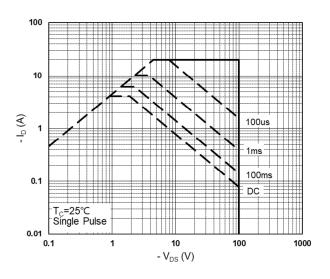


Fig.7 Capacitance

Fig.8 Safe Operating Area

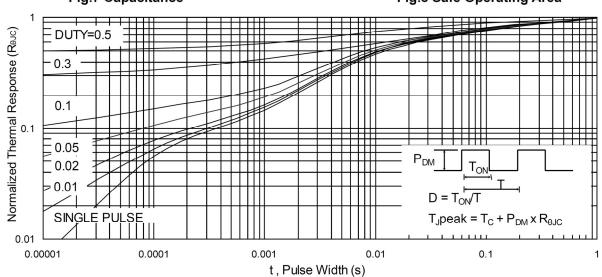
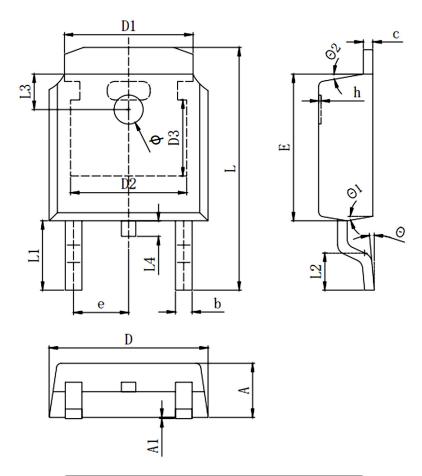


Fig.9 Normalized Maximum Transient Thermal Impedance



TO-252 D-PAK Package



Symbols	Millimeters		
Symbols	MIN.	Mom.	MAX.
Α	2.200	2.300	2.400
A1	0.000		0.127
b	0.640	0.690	0.740
c(电镀后)	0.460	0.520	0.580
D	6.500	6.600	6.700
D1	5.334 REF		
D2	4.826 REF		
D3	3.166REF		
E	6.000	6.100	6.200
e	2.286 TYP		
h	0.000	0.100	0.200
L	9.900	10.100	10.300
L1	2.888 REF		
L2	1.400	1.550	1.700
L3	1.600 REF		
L4	0.600	0.800	1.000
Ф	1.100	1.200	1.300
θ	0°		8°
θ1	9° TYP		
θ2	9° TYP		

单击下面可查看定价,库存,交付和生命周期等信息

>>SiliconWisdom(矽睿半导体)