SWR40P04

40V Single P-Channel Enhancement-Mode MOSFET

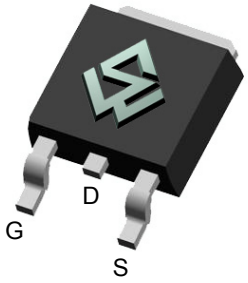
General Description

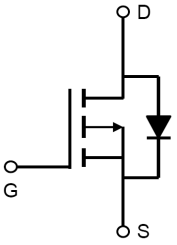
- Low gate charge.
- Uses advanced trench process technology.
- Use in PWM applications

Product Summary

- BV_{DSS} -40V
- $R_{DS(on)}$ @VGS = -10V < 19mΩ
- $R_{DS(on)}$ @VGS = -4.5V < 25mΩ

TO-252 D-PAK





Absolute Maximum Ratings (T_A = 25°C unless otherwise noted)

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	-40	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current (T_A=25ºC)	I_D	-40	A
Drain Current (T_A=75ºC)		-18	A
Pulsed Drain Current [a]	I_{DM}	-140	A
Power Dissipation [b] (T_C=25ºC)	P_D	40	W
Power Dissipation [b] (T_A=25ºC)		2.5	W
Junction and Storage Temperature Range	T_J, T_{STG}	-55 ~ +150	ºC

Thermal Characteristics

Parameter	Symbol	Maximum	Units
Junction-to-Ambient [a] (t ≤ 10s)	$R_{\theta JA}$	25	ºC/W
Junction-to-Ambient [a,d] (Steady-State)		50	ºC/W
Junction-to-Lead (Steady-State)	$R_{\theta JL}$	5	ºC/W

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0V , I_D = -250uA	-40			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -40V , V_{GS} = 0V			-1	uA
I_{GSS}	Gate-Body Leakage Current	V_{GS} = ±20V, V_{DS} = 0V			±100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS} , I_D = -250uA	-1.8		-3	V
$R_{DS(ON))}$	Drain-Source On-State Resistance	V_{GS} = -10V , I_D = -12A		14	19	mΩ
		V_{GS} = -4.5V , I_D = -8A		20	25	mΩ
g_{FS}	Forward Transconductance	V_{DS} = -5V , I_D = -12A		16		S
Drain-Source Diode Characteristics						
V_{SD}	Diode Forward Voltage	V_{GS} = 0V , I_S = -1A			-1.0	V
I_S	Maximum Body-Diode Continuous Current				-12	A
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = -20V , V_{GS} = 0V f = 1.0MHz		2657		pF
C_{oss}	Output Capacitance			193		pF
C_{rss}	Reverse Transfer Capacitance			163		pF
Switching Characteristics						
Q_g	Total Gate Charge	V_{DS} = -20V , I_D = -12A V_{GS} = -10V		34.1		nC
Q_{gs}	Gate-Source Charge			7		nC
Q_{gd}	Gate-Drain Charge			8		nC
$t_{D(ON)}$	Turn-On Delay Time	V_{DS} = -20V , ID = -12A V_{GS} = -10 V R_{GEN} = -3 ohm		14		ns
t_r	Turn-On Rise Time			22.2		ns
$t_{D(OFF)}$	Turn-Off Delay Time			34		ns
t_f	Turn-Off Fall Time			12.5		ns

a. Repetitive rating, Pulse width limited by junction temperature $T_{J(MAX)}$=150 ºC. Ratings are based on low frequency and duty cycles to keep initial T_J=25 ºC

b. The power dissipation P_D is based on $T_{J(MAX)}$=150 ºC , using≤10s junction-to-ambient thermal resistance.

c. The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A = 25°C. The value in any given application depends on the user's specific board design.

d. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.

Typical Characteristics

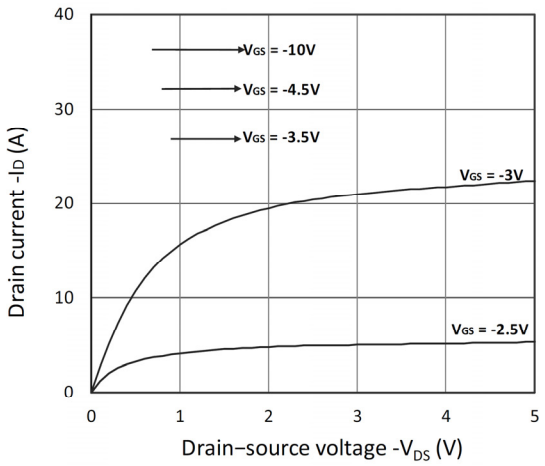


Figure 1. Output Characteristics

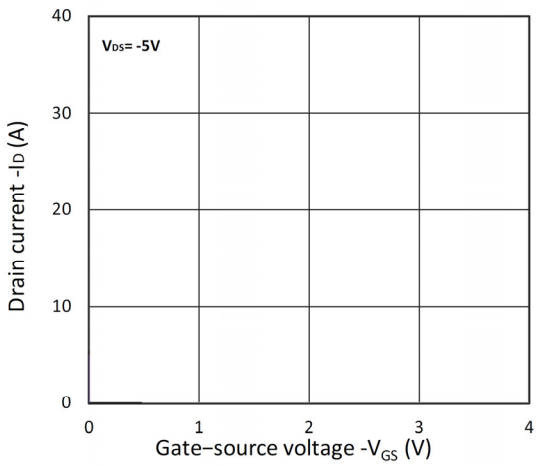


Figure 2. Transfer Characteristics

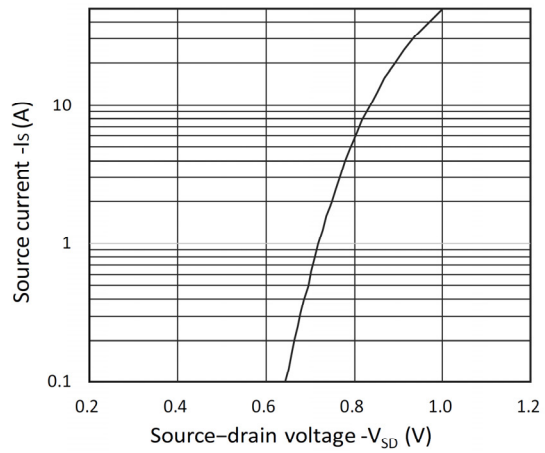


Figure 3. Forward Characteristics of Reverse

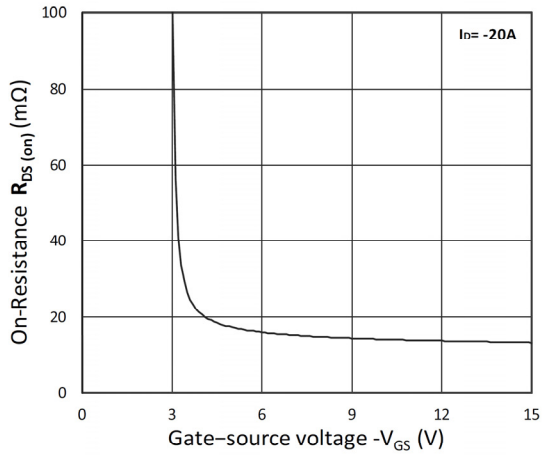


Figure 4. $R_{DS(ON)}$ vs. V_{GS}

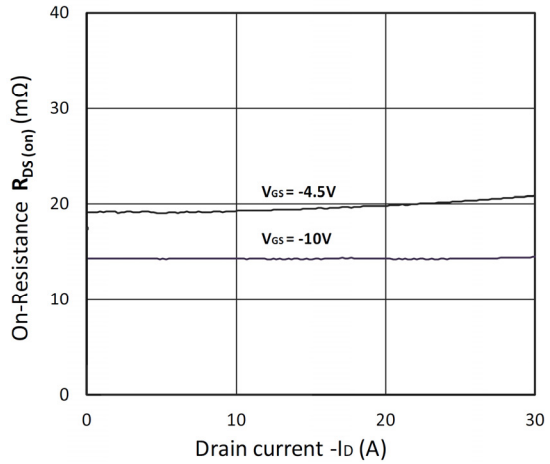


Figure 5. $R_{DS(ON)}$ vs. I_D

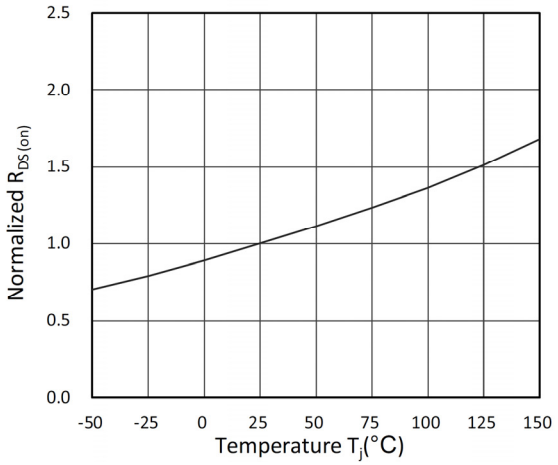


Figure 6. Normalized $R_{DS(on)}$ vs. Temperature

Typical Characteristics

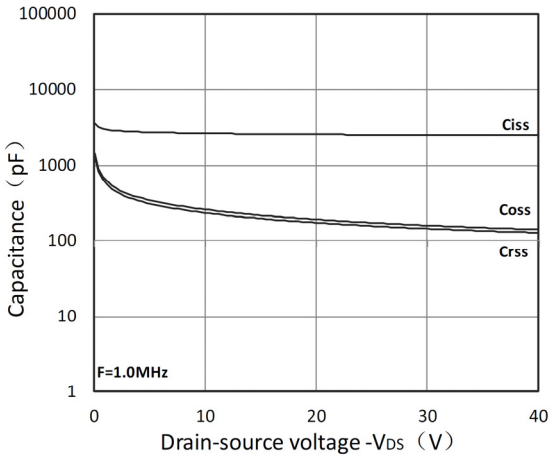


Figure 7. Capacitance Characteristics

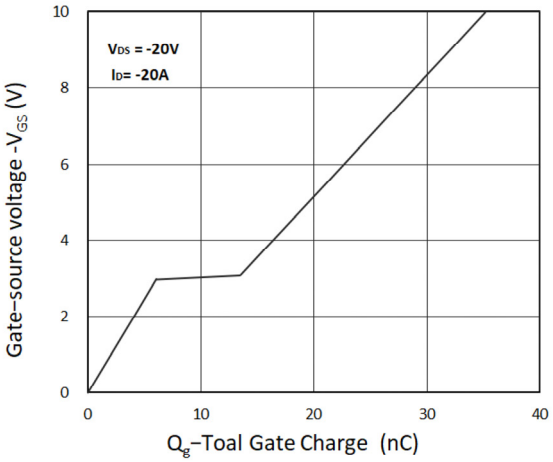


Figure 8. Gate Charge Characteristics

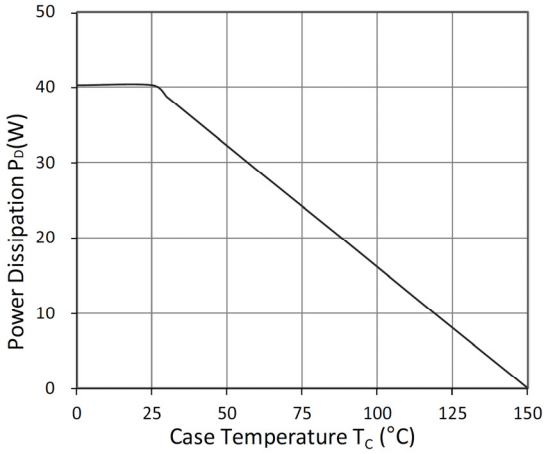


Figure 9. Power Dissipation

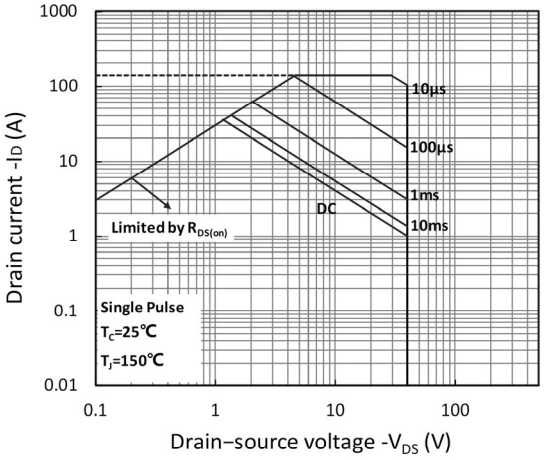


Figure10. Safe Operating Area

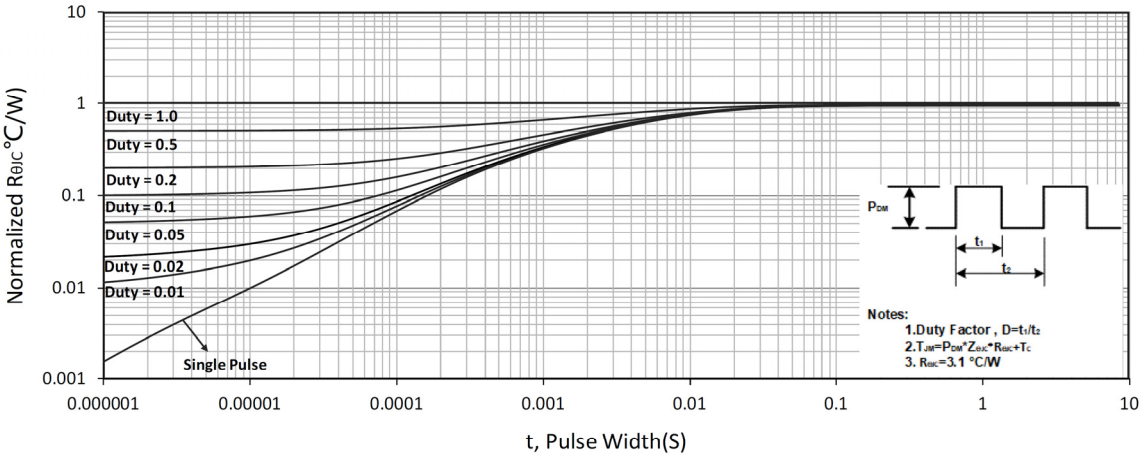
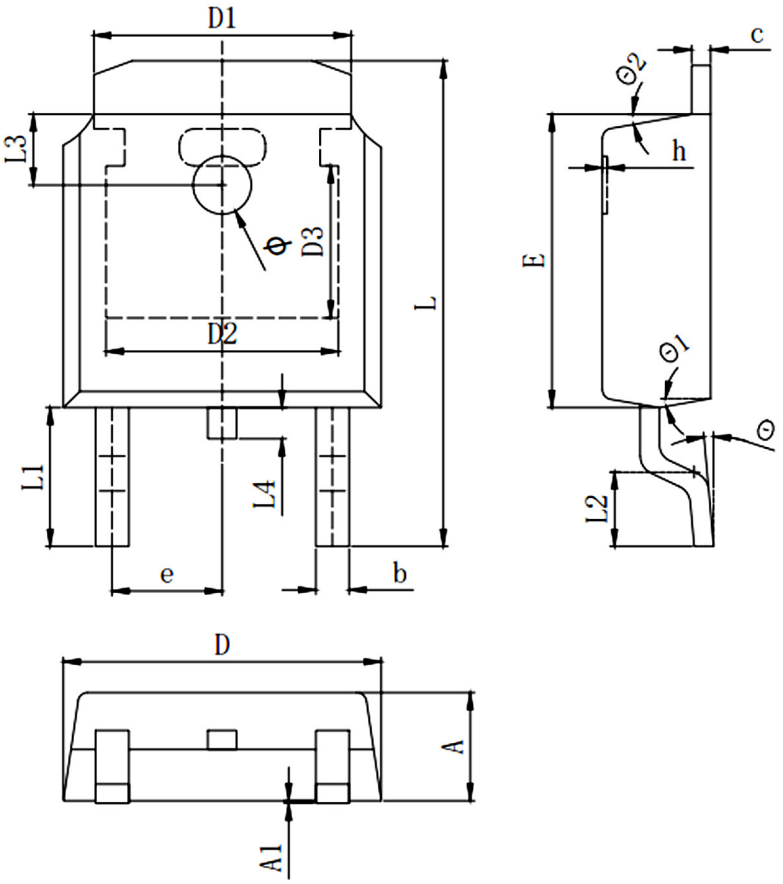


Figure 11. Normalized Maximum Transient Thermal Impedance

TO-252 D-PAK Package



Symbols	Millimeters		
	MIN.	Mom.	MAX.
A	2.200	2.300	2.400
A1	0.000		0.127
b	0.640	0.690	0.740
c(电镀后)	0.460	0.520	0.580
D	6.500	6.600	6.700
D1	5.334 REF		
D2	4.826 REF		
D3	3.166REF		
E	6.000	6.100	6.200
e	2.286 TYP		
h	0.000	0.100	0.200
L	9.900	10.100	10.300
L1	2.888 REF		
L2	1.400	1.550	1.700
L3	1.600 REF		
L4	0.600	0.800	1.000
Φ	1.100	1.200	1.300
θ	0°		8°
θ1	9° TYP		
θ2	9° TYP		

单击下面可查看定价，库存，交付和生命周期等信息

>>SiliconWisdom(矽睿半导体)