

**FEATURES**

- LIN 2.x/ISO 17987-4:2016 (12V)/SAE J2602 compliant
- AEC-Q100 qualified
- Compatible with K line
- Integrated over-temperature protection function (thermal shutdown)
- Integrated 30kΩ bus pull-up slave resistor
- Bus current limiting protection function
- Battery power failure detection function
- Very low power consumption sleep mode and standby mode
- Support remote wake-up
- Baudrate up to 20 kBd
- Low ElectroMagnetic Emissions (EME)
- Available in SOP8 and DFN3\*3-8 packages

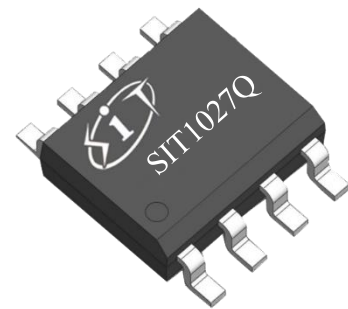
**PRODUCT APPEARANCE**

Fig 1. Provide environmentally friendly lead-free package

**DESCRIPTION**

SIT1027Q is a local interconnect network (LIN) physical layer transceiver that complies with LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A, ISO 17987-4:2016 (12V) and SAE J2602 standards. It is mainly suitable for in-vehicle networks with a transmission rate of 1kbps to 20kbps. SIT1027Q controls the state of the LIN bus through the TXD pin, and can convert the data stream sent by the protocol controller into a bus signal with the best slew rate and waveform shaping to minimize electromagnetic radiation emission (EME). The LIN bus output pin has an internal pull-up resistor. Only when used as a master node, the LIN bus port needs to be pulled up to  $V_{BAT}$  through an external resistor in series with a diode. SIT1027Q receives the data stream on the bus through the LIN pin, and transmits the data to the external microcontroller through the receiver's output pin RXD.

SIT1027Q can operate in the range of 5.5V~27V and supports 12V applications. SIT1027Q has an extremely low quiescent current consumption in sleep mode and standby mode. It can quickly minimize power consumption in the event of a failure. The device can be placed in normal mode via a signal on the pin SLP\_N.

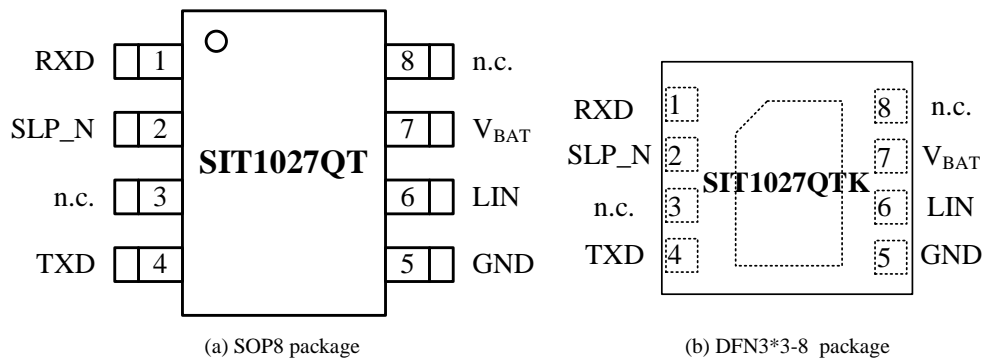
**PIN CONFIGURATION**


Fig 2. SIT1027Q pin configuration diagrams

**PIN DESCRIPTION**

Table 1. Pin description

Pin	Symbol	Description
1	RXD	Receive data output (open-drain); active LOW after a wake-up event.
2	SLP_N	Sleep control input (active LOW); controls inhibit output; resets wake-up source flag on TXD and wake-up request on RXD.
3	n.c.	Not connected.
4	TXD	Transmit data input.
5	GND	Ground.
6	LIN	LIN bus line input/output.
7	V <sub>BAT</sub>	Battery supply voltage.
8	n.c.	Not connected.

NOTE: In the DFN3\*3-8 package, the pad on the back is connected to the GND pin of the chip. In order to obtain better heat dissipation performance, the pad on the back can be connected to a suitable “ground” on the PCB board.

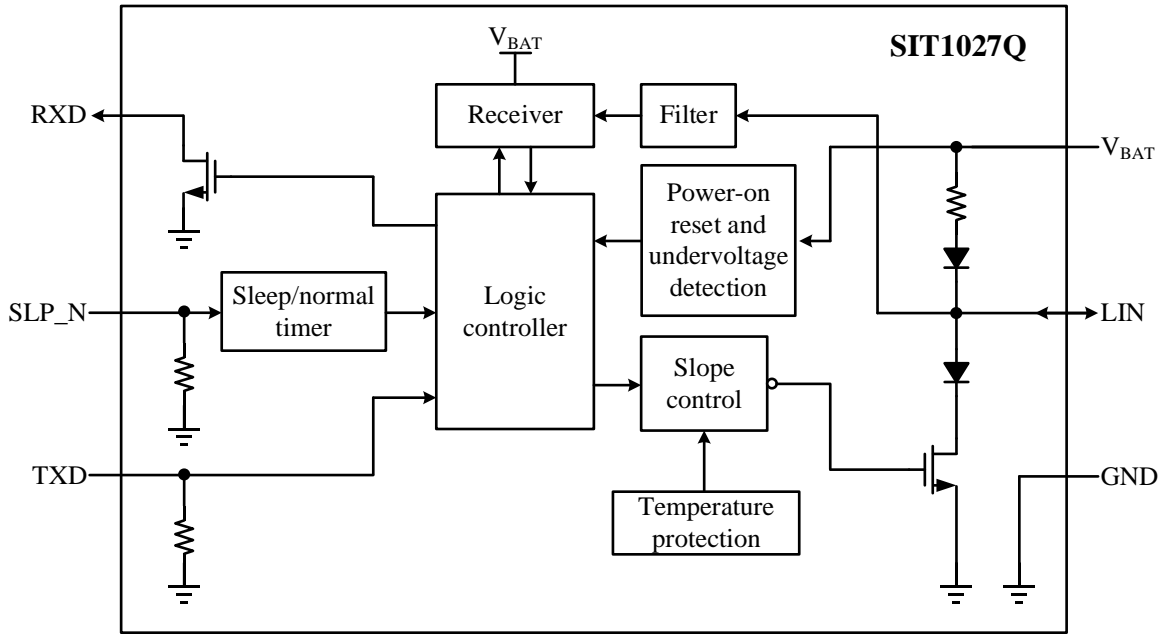


Fig 3. Block diagram

## FEATURE DESCRIPTION

### 1 Overview

The SIT1027Q is an interface device used between the LIN protocol controller and the physical bus. It can be used in in-vehicle and industrial control with a data rate up to 20kBd. The SIT1027Q receives the data stream sent by protocol controller at the pin TXD, and converts it into a bus signal with appropriate slew rate and waveform shaping. The input data on LIN bus is output to external microcontroller by pin RXD. This device is compliant with LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A, ISO 17987-4:2016 (12V) and SAE J2602 standards.

### 2 Short-circuit protection

Pin TXD provides an internal pull-down to GND to apply a predefined level on TXD when it is not enabled. The pin SLP\_N also provides an internal pull-down to force the transceiver to enter sleep mode when SLP\_N is not enabled.

Pin RXD will be left floating and limit the output current of transmitter to prevent a short-circuit between LIN and  $V_{BAT}$  or GND if the supply on pin  $V_{BAT}$  is turned off. There is no reverse current at the bus terminal, and the connection between LIN supply can be shut off without affecting the bus.

### 3 Thermal Shutdown

In normal mode, the over-temperature protection circuit will disable the output driver when the junction temperature of SIT1027Q exceeds the shutdown junction temperature  $T_{j(sd)}$ . The over-temperature protection

circuit will disable the output driver; when the junction temperature is lower than the hysteresis temperature, the driver is enabled again.

#### 4 Undervoltage detection on V<sub>BAT</sub>

If V<sub>BAT</sub> is lower than V<sub>th(VBATL)</sub>L during use, the protection circuit will disable the output driver; when V<sub>BAT</sub> > V<sub>th(VBATL)</sub>H, the driver will be enabled again.

#### 5 Operating modes

As shown in [Fig 4](#), the SIT1027Q supports four functional modes for normal operation (Normal mode), power-up (Power-on mode), standby operation (Standby mode) and very-low-power operation (Sleep mode). The operating states in each mode are shown in [Table 2](#).

**Sleep mode:** This mode is the most power saving mode of the SIT1027Q. It can be awakened remotely via pin LIN, or activated directly via pin SLP\_N. In order to prevent SIT1027Q from waking up due to accidental wake-up events caused by automotive transients or EMI, filters are designed at the receiver's input (LIN pin) and SLP\_N pin. The necessary condition for SIT1027Q to be awakened in sleep mode is: the time to wake it up remotely through the LIN pin must be greater than t<sub>wake(dom)LIN</sub> (the wake-up time of LIN); the time to wake up directly through the SLP\_N pin must be greater than t<sub>gotonorm</sub>.

In normal mode, when SLP\_N pin has a falling edge and SLP\_N remains low for longer than t<sub>gotosleep</sub>, SIT1027Q enters sleep mode.

**Standby mode:** SIT1027Q has very low static power consumption in this mode. When SIT1027Q is in sleep mode, if a remote wake-up event is detected, the device will automatically enter standby mode immediately, and the low level on the RXD pin will indicate that the wake-up process is used to send an interrupt flag to the MCU.

Setting pin SLP\_N high during Standby mode results in the following events:

- (1) A change into Normal mode if the high level on pin SLP\_N has been maintained for a certain time period (t<sub>gotonorm</sub>).
- (2) An immediate reset of the wake-up request signal on pin RXD.

**Normal mode:** Only in Normal mode the receiver and transmitter are active and the SIT1027Q is able to transmit and receive data via the LIN bus. The high level of bus represents recessive and low level represents dominant. The receiver detects the data stream on the LIN bus and outputs it to the microcontroller via pin RXD. Normal mode is entered as a high level on pin SLP\_N and maintained for a time of at least t<sub>gotonorm</sub> while the SIT1027Q is in Sleep, Power-up or Standby mode. The Sleep mode is entered by setting pin SLP\_N low for longer than t<sub>gotosleep</sub>.

**Power-on mode:** If the voltage on  $V_{BAT}$  is less than the low-level reset threshold  $V_{th(VBAT)L}$  when powering on, the SIT1027Q is in power-on reset mode and all input and output functions are disabled; when the voltage on  $V_{BAT}$  is greater than the high-level reset threshold  $V_{th(VBAT)H}$ , SIT1027Q enters sleep mode.

## 6 Wake Up Events

In sleep mode, the device can be awakened by the following two ways:

- (1) Remote wake-up via pin LIN;
- (2) Wake up directly via mode transition. If SLP\_N is held HIGH for  $t_{gotonorm}$ , the device will switch from sleep mode to normal mode.

## 7 Remote Wake Up Events

LIN pin remote wake-up: When the LIN pin is pulled down to a low level through a falling edge, a rising edge appears at the next moment, and the low-level hold time between the rising edge and the falling edge at the previous moment is greater than  $t_{wake (dom) LIN}$ , the process is regarded as effective remote wake-up (as shown in [Fig 5](#)).

After the remote wake-up, the wake-up request event interrupts the microcontroller with the low level of the RXD pin as the indicator signal.

## 8 Fail-safe

- A pull-down to GND on pin TXD prevents an undefined floating state of the TXD pin.
- A pull-down to GND on pin SLP\_N forces the transceiver in to Sleep mode when pin SLP\_N is floating.
- A loss of power has no impact on the bus port. There is no reverse current on the bus port.
- Bus driver output stage current limiting to protect the driver against the short circuits to pin  $V_{BAT}$ .
- To avoid the effects of the TXD pin being forced permanently low due to hardware and/or software application failures, after switching to normal mode, the LIN driver is enabled only when high TXD power is detected.

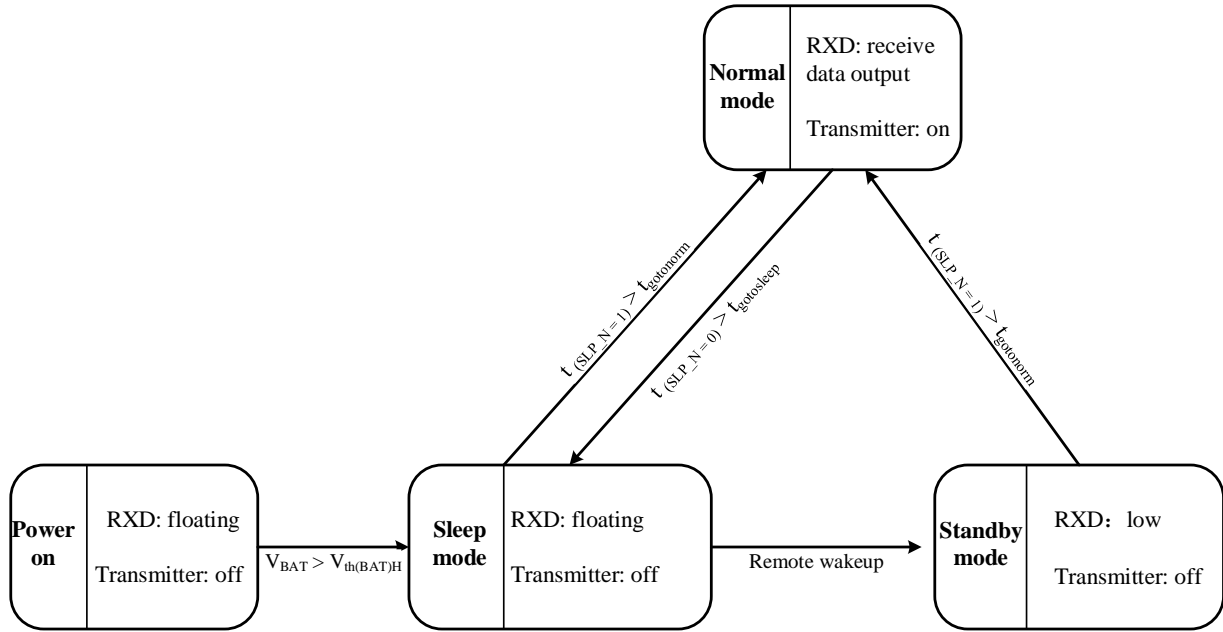


Fig 4. State diagram

Table 2. Working status of SIT1027Q in each mode

Mode	SLP_N	RXD	Transmitter	Remarks
Sleep	low	floating	off	no wake-up request detected
Standby	low	low	off	wake-up request detected
Normal	high	recessive: high dominant: low	on	Enable bus signal shaping
Power-on	low	floating	off	Disable all input and output functions

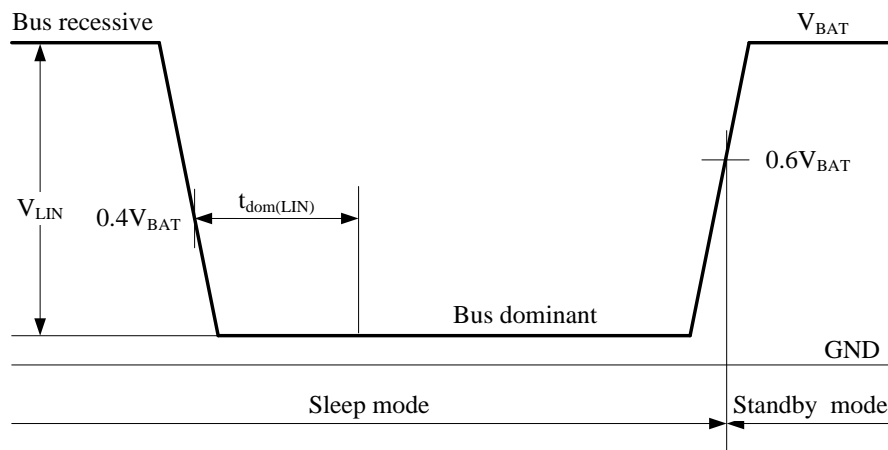


Fig 5. Remote wake-up behavior

**LIMITING VALUES**

Parameter	Symbol	Conditions	Range	Unit
battery supply voltage	$V_{BAT}$	with respect to GND	-0.3 ~ +42	V
voltage on pin TXD	$V_{TXD}$	$I_{SLP\_N}$ no limitation	-0.3 ~ +6	V
		$I_{SLP\_N} < 500\mu A$	-0.3 ~ +7	
voltage on pin RXD	$V_{RXD}$	$I_{SLP\_N}$ no limitation	-0.3 ~ +6	V
		$I_{SLP\_N} < 500\mu A$	-0.3 ~ +7	
voltage on pin SLP_N	$V_{SLP\_N}$	$I_{SLP\_N}$ no limitation	-0.3 ~ +6	V
		$I_{SLP\_N} < 500\mu A$	-0.3 ~ +7	
voltage on pin LIN	$V_{LIN}$	with respect to GND	-42 ~ +42	V
virtual junction temperature	$T_j$		-40 ~ 150	°C
ambient temperature	$T_{amb}$		-40 ~ 125	°C
storage temperature	$T_{stg}$		-55 ~ 150	°C
ESD, IEC61000-4-2	$V_{ESD}$	on pins LIN and $V_{BAT}$	±4	kV
ESD, human body model		on pins LIN and $V_{BAT}$	±8	kV
ESD, human body model		on pins TXD, RXD and SLP_N	±4	kV
ESD, charge device model		All pins	±1000	V
ESD, machine model		All pins	±400	V

The maximum limit parameters mean that exceeding these values may cause irreversible damage to the device. Under these conditions, it is not conducive to the normal operation of the device. The continuous operation of the device at the maximum allowable rating may affect the reliability of the device. The reference point for all voltages is ground.



**STATIC CHARACTERISTICS**

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>Supply</b>						
Battery supply voltage	$V_{BAT}$		5.5	12	27	V
battery supply current	$I_{BAT}$	Sleep mode bus recessive ( $V_{LIN}=V_{BAT}$ ; $V_{SLP\_N}=0V$ )	1	4	20	$\mu A$
		Sleep mode bus dominant ( $V_{LIN}=V_{BAT}$ ; $V_{SLP\_N}=0V$ )	100	350	1000	$\mu A$
		Standby mode; bus recessive ( $V_{LIN}=V_{BAT}$ ; $V_{SLP\_N}=0V$ )	1	4	20	$\mu A$
		Standby mode; bus dominant ( $V_{BAT}=12V$ ; $V_{LIN}=0V$ ; $V_{SLP\_N}=0V$ )	100	350	1000	$\mu A$
		Normal mode; bus recessive ( $V_{LIN}=V_{BAT}$ ; $V_{TXD}=5V$ ; $V_{SLP\_N}=5V$ )	50	160	300	$\mu A$
		Normal mode; bus dominant ( $V_{BAT}=12V$ ; $V_{TXD}=0V$ ; $V_{SLP\_N}=5V$ )	0.5	1.6	3	mA
<b>Power-on reset</b>						
LOW-level $V_{BAT}$ reset threshold voltage	$V_{th}(V_{BATL})L$		3.9	4.4	4.7	V
HIGH-level $V_{BAT}$ reset threshold voltage	$V_{th}(V_{BATL})H$		4.2	4.7	5.1	V
$V_{BAT}$ reset hysteresis voltage	$V_{hys}(V_{BATL})$		0.15	0.3	0.6	V
<b>Pin TXD</b>						

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
HIGH-level input voltage	$V_{IH}$		2		7	V
LOW-level input voltage	$V_{IL}$		-0.3		+0.8	V
hysteresis voltage	$V_{hys}$		50	200	400	mV
pull-down resistance on pin TXD	$R_{PD(TXD)}$	$V_{TXD}=5V$	50	125	400	k $\Omega$
<b>Pin SLP_N</b>						
HIGH-level input voltage	$V_{IH}$		2		7	V
LOW-level input voltage	$V_{IL}$		-0.3		0.8	V
hysteresis voltage	$V_{hys}$		50	200	400	mV
pull-down resistance on pin SLP_N	$R_{PD(SLP\_N)}$	$V_{SLP\_N}=5V$	100	250	650	k $\Omega$
<b>Pin RXD</b>						
LOW-level output current	$I_{OL}$	Normal mode; $V_{RXD}=0.4V$ ; $V_{LIN}=0V$	2	-	-	mA
HIGH-level leakage current	$I_{LH}$	Normal mode; $V_{RXD}=5V$ ; $V_{LIN}=V_{BAT}$	-5	-	5	$\mu A$
<b>Pin LIN</b>						
current limitation for driver dominant state	$I_{BUS\_LIM}$	$V_{TXD}=0V$ ; $V_{LIN}=V_{BAT}=18V$	40	-	100	mA
receiver recessive input leakage current	$I_{BUS\_PAS\_rec}$	$V_{TXD}=5V$ ; $V_{LIN}=27V$ ; $V_{BAT}=5.5V$	-	-	10	$\mu A$
receiver dominant input leakage current including pull-up resistor	$I_{BUS\_PAS\_dom}$	Normal mode; $V_{TXD}=5V$ ; $V_{LIN}=0V$ ; $V_{BAT}=12V$	-600	-	-	$\mu A$
loss-of-ground bus current	$I_{BUS\_NO\_GND}$	$V_{BAT}=27V$ ; $V_{LIN}=0V$	-1000	-	10	$\mu A$
loss-of-battery bus current	$I_{BUS\_NO\_BAT}$	$V_{BAT}=0V$ ; $V_{LIN}=27V$	-	-	10	$\mu A$
receiver dominant input voltage	$V_{th(dom)RX}$				$0.4V_{BAT}$	V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
receiver recessive input voltage	$V_{th(rec)RX}$		$0.6V_{BAT}$			V
receiver center voltage	$V_{th(RX)cntr}$	$V_{th(RX) cntr} = (V_{th(rec)RX} + V_{th(dom)RX})/2$	$0.475V_{BAT}$	$0.5 V_{BAT}$	$0.525V_{BAT}$	V
receiver hysteresis voltage	$V_{th(hys)RX}$	$V_{th(hys)RX} = V_{th(rec)RX} - V_{th(dom)RX}$			$0.175V_{BAT}$	V
slave resistance	$R_{slave}$	connected between pins LIN and $V_{BAT}$ ; $V_{LIN}=0V$ ; $V_{BAT}=12V$ ; $V_{TXD}=V_{SLP\_N}=5V$	20	30	60	k $\Omega$
capacitance on pin LIN	$C_{LIN}$				20	pF
dominant output voltage	$V_{o(dom)}$	Normal mode; $V_{TXD}=0V$ ; $V_{BAT}=7V$			1.4	V
		Normal mode; $V_{TXD}=0V$ ; $V_{BAT}=18V$			2.0	V
<b>Thermal shutdown</b>						
shutdown junction temperature	$T_{j(sd)}$		150		200	$^{\circ}C$

(Unless specified otherwise;  $5.5V \leq V_{BAT} \leq 27V$ ,  $-40^{\circ}C \leq T_j \leq 150^{\circ}C$ ; typical in  $V_{BAT}=12V$ ,  $T_{amb}=25^{\circ}C$ .)

**DYNAMIC CHARACTERISTICS**

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>Duty cycles</b>						
duty cycle 1	$\delta 1$ <sup>[1][2]</sup>	$V_{th(rec)(max)}=0.744 \times V_{BAT}$ ; $V_{th(dom)(max)}=0.581 \times V_{BAT}$ ; $t_{bit}=50\mu s$ ; $V_{BAT}=7V \sim 18V$ , <a href="#">Fig 6</a>	0.396			
		$V_{th(rec)(max)}=0.76 \times V_{BAT}$ ; $V_{th(dom)(max)}=0.593 \times V_{BAT}$ ; $t_{bit}=50\mu s$ ; $V_{BAT}=5.5V \sim 7V$ , <a href="#">Fig 6</a>	0.396			
duty cycle 2	$\delta 2$ <sup>[2][3]</sup>	$V_{th(rec)(min)}=0.422 \times V_{BAT}$ ; $V_{th(dom)(min)}=0.284 \times V_{BAT}$ ; $t_{bit}=50\mu s$ ; $V_{BAT}=7.6V \sim 18V$ , <a href="#">Fig 6</a>			0.581	
		$V_{th(rec)(min)}=0.41 \times V_{BAT}$ ; $V_{th(dom)(min)}=0.275 \times V_{BAT}$ ; $t_{bit}=50\mu s$ ; $V_{BAT}=6.1V \sim 7.6V$ , <a href="#">Fig 6</a>			0.581	
duty cycle 3	$\delta 3$ <sup>[1][2]</sup>	$V_{th(rec)(max)}=0.778 \times V_{BAT}$ ; $V_{th(dom)(max)}=0.616 \times V_{BAT}$ ; $t_{bit}=96\mu s$ ; $V_{BAT}=7V \sim 18V$ , <a href="#">Fig 6</a>	0.417			
		$V_{th(rec)(max)}=0.797 \times V_{BAT}$ ; $V_{th(dom)(max)}=0.630 \times V_{BAT}$ ; $t_{bit}=96\mu s$ ; $V_{BAT}=5.5V \sim 7V$ , <a href="#">Fig 6</a>	0.417			
duty cycle 4	$\delta 4$ <sup>[2][3]</sup>	$V_{th(rec)(min)}=0.389 \times V_{BAT}$ ; $V_{th(dom)(min)}=0.251 \times V_{BAT}$ ; $t_{bit}=96\mu s$ ; $V_{BAT}=7.6V \sim 18V$ , <a href="#">Fig 6</a>			0.590	
		$V_{th(rec)(min)}=0.378 \times V_{BAT}$ ; $V_{th(dom)(min)}=0.242 \times V_{BAT}$ ; $t_{bit}=96\mu s$ ; $V_{BAT}=6.1V \sim 7.6V$ , <a href="#">Fig 6</a>			0.590	
<b>Timing characteristics</b>						
receiver propagation delay	$t_{PD(RX)}$ <sup>[4]</sup>				6	$\mu s$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
receiver propagation delay symmetry	$t_{PD(RX)sym}$ [4]		-2		2	$\mu s$
LIN dominant wake-up time	$t_{wake(dom)LIN}$	Sleep mode	30	80	150	$\mu s$
go to normal time	$t_{gotonorm}$		2	6	10	$\mu s$
go to sleep time	$t_{gotosleep}$		2	6	10	$\mu s$

(Unless specified otherwise;  $5.5V \leq V_{BAT} \leq 27V$ ,  $-40^{\circ}C \leq T_j \leq 150^{\circ}C$ ; typical in  $V_{BAT}=12V$ ,  $T_{amb}=25^{\circ}C$ .)

[1]  $\delta 1, \delta 3 = \frac{t_{bus(rec)(min)}}{2 \times t_{bit}}$ ;

[2] Bus load conditions are: (1)  $C_L=1nF$ ,  $R_L=1k\Omega$ ; (2)  $C_L=6.8nF$ ,  $R_L=660\Omega$ ; (3)  $C_L=10nF$ ,  $R_L=500\Omega$ ;

[3]  $\delta 2, \delta 4 = \frac{t_{bus(rec)(max)}}{2 \times t_{bit}}$ ;

[4] Load condition pin RXD:  $C_{TXD}=20pF$ ,  $R_{RXD}=2.4k\Omega$ .

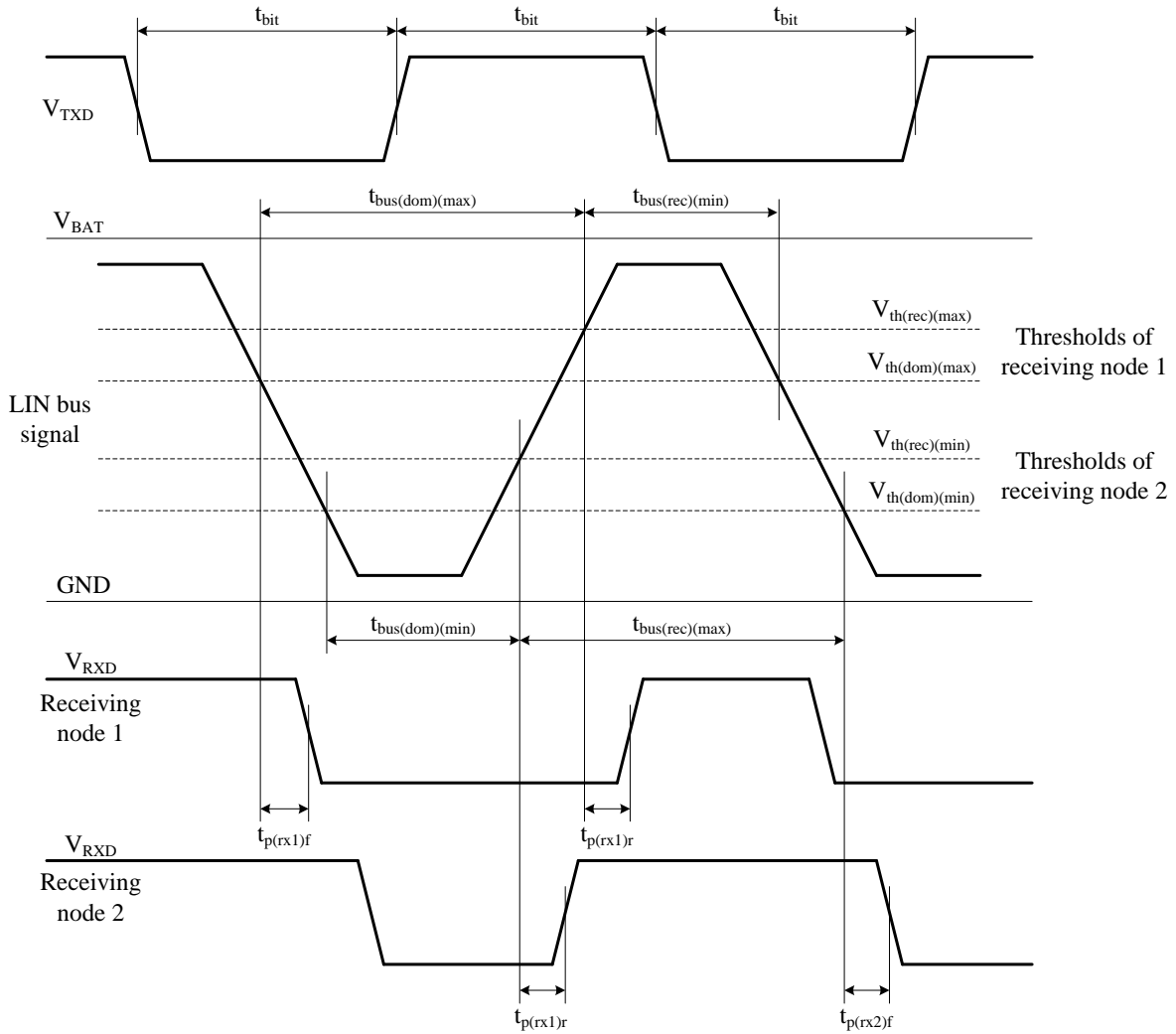


Fig 6. Timing diagram LIN transceiver

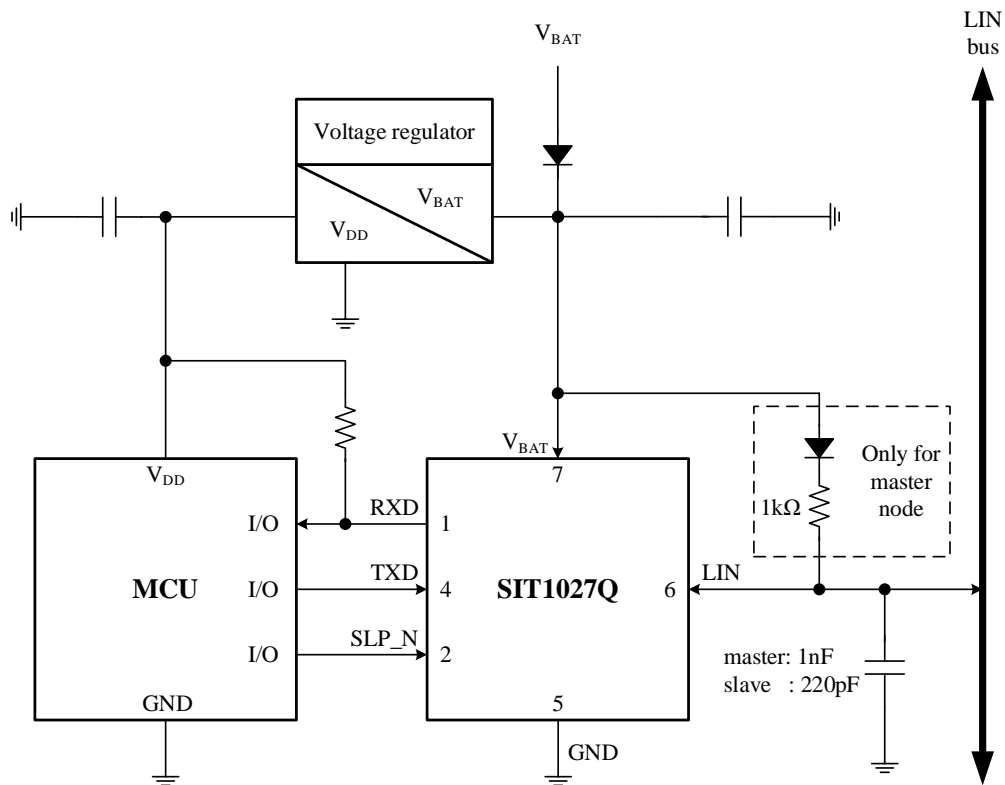
**TYPICAL APPLICATION**


Fig 7. Typical application of the SIT1027Q

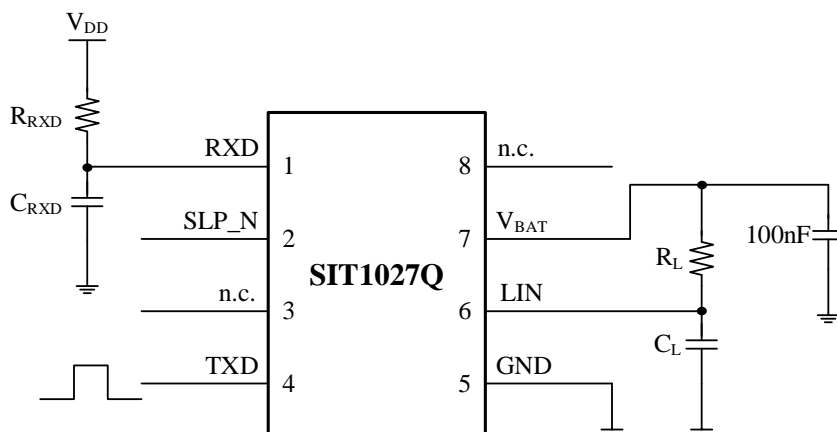
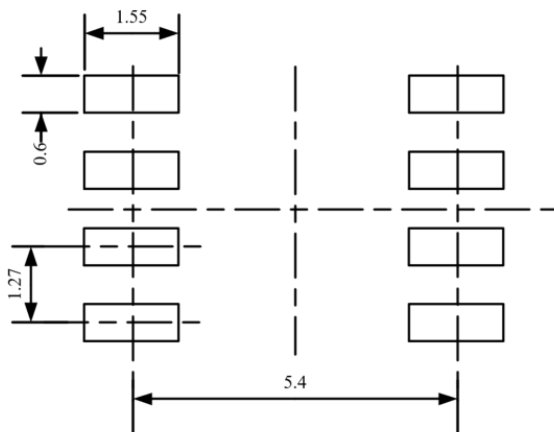
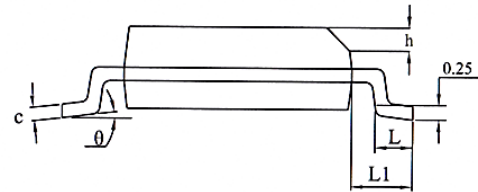
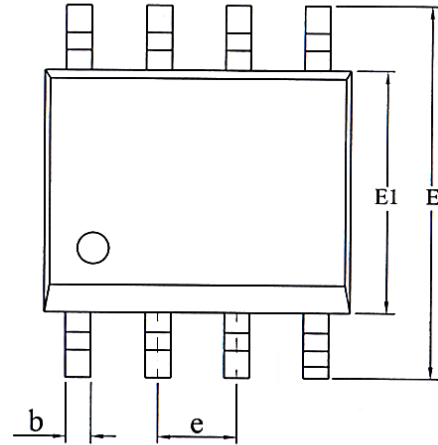
**TIMING TEST CIRCUIT**


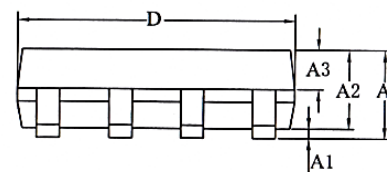
Fig 8. Timing test circuit for LIN transceiver

**SOP8 DIMENSIONS**
**PACKAGE SIZE**

SYMBOL	MIN./mm	TYP./mm	MAX./mm
A	1.40	-	1.80
A1	0.10	-	0.25
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.38	-	0.51
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	-	0.50
L	0.40	0.60	0.80
L1	1.05REF		
c	0.20	-	0.25
$\theta$	0°	-	8°



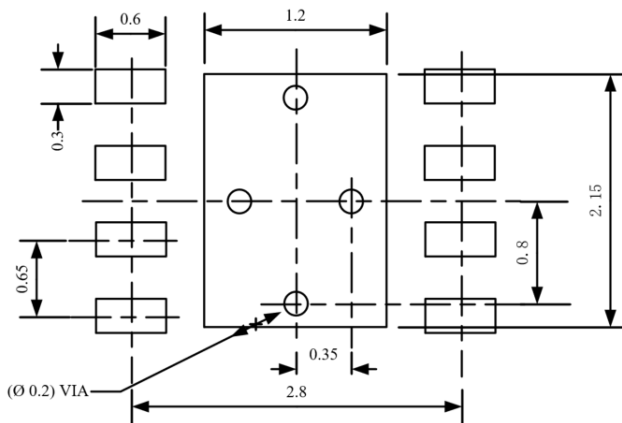
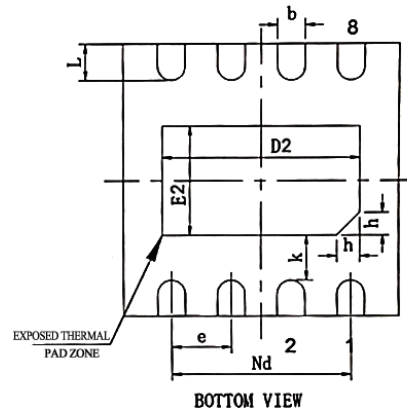
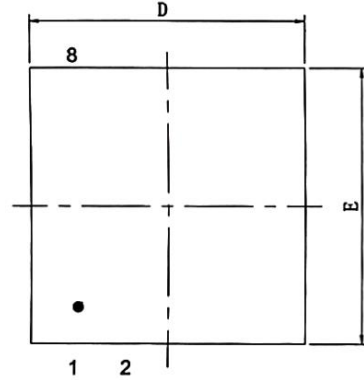
LAND PATTERN EXAMPLE (Unit: mm)



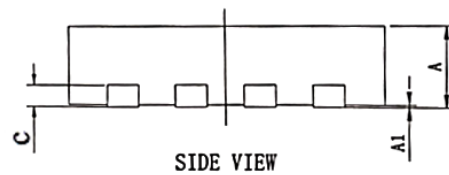


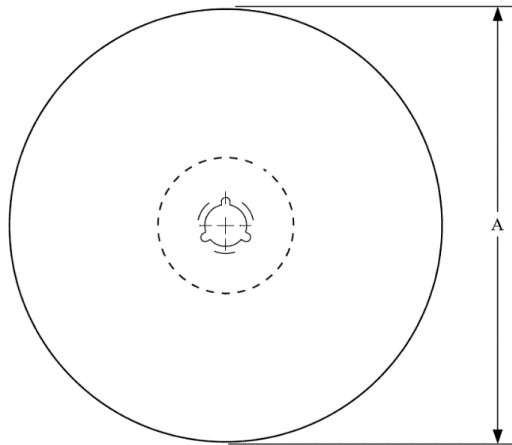
**DFN3\*3-8 DIMENSIONS**
**PACKAGE SIZE**

SYMBOL	MIN/mm	TYP /mm	MAX/mm
A	0.70	0.75	0.80
A1	0	0.02	0.05
c	0.203 REF		
D	2.90	3.00	3.10
E	2.90	3.00	3.10
D2	2.05	2.15	2.25
Nd	1.95BSC		
E2	1.10	1.20	1.30
b	0.25	0.30	0.35
e	0.65 TYP		
k	0.50REF		
L	0.35	0.4	0.45
h	0.20	0.25	0.30

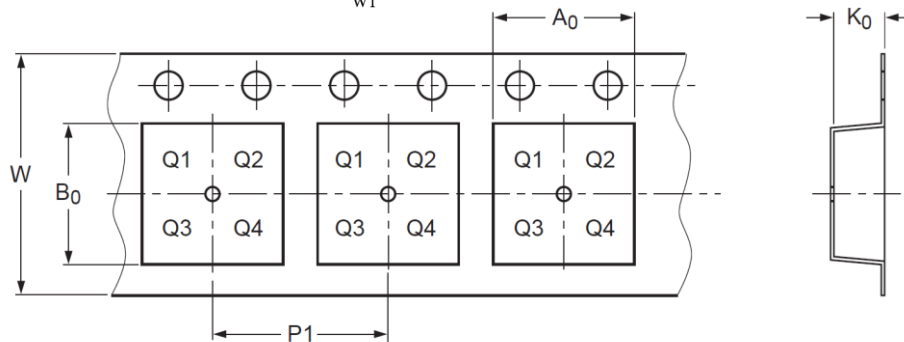
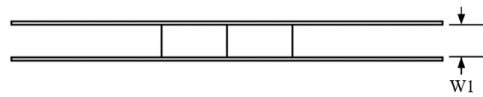


LAND PATTERN EXAMPLE (Unit: mm)



**TAPE AND REEL INFORMATION**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



Direction of Feed →

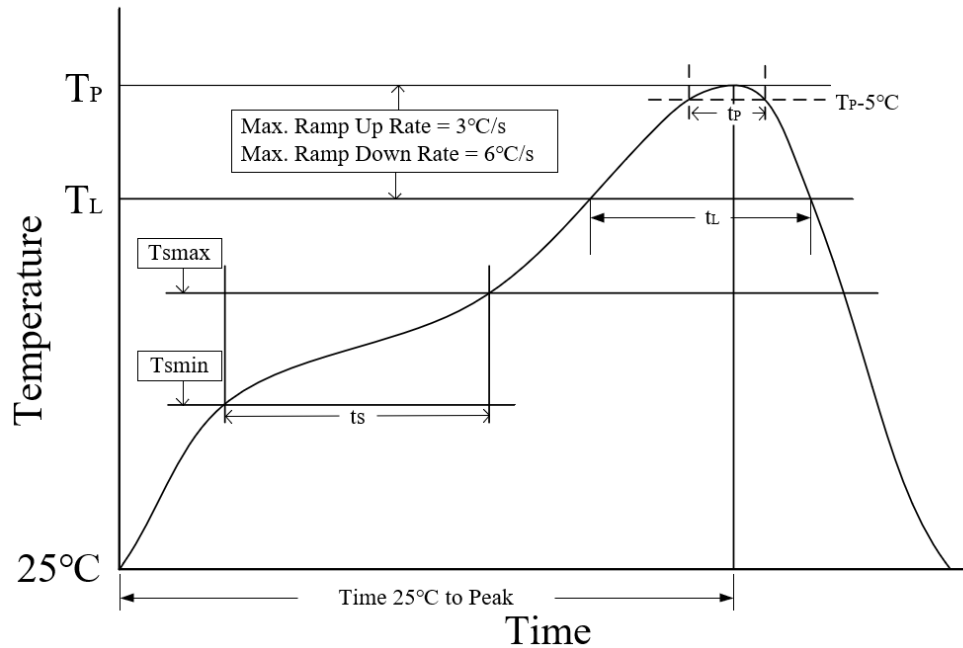
PIN1 is in quadrant 1

Package type	Reel diameter A (mm)	Tape width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)
SOP8	330±1	12.4	6.60±0.1	5.30±0.10	1.90±0.1	8.00±0.1	12.00±0.1
DFN3*3-8	329±1	12.4	3.30±0.1	3.30±0.1	1.10±0.1	8.00±0.1	12.00±0.3

**ORDERING INFORMATION**

TYPE NUMBER	PACKAGE	PACKING
SIT1027QT	SOP8	Tape and reel
SIT1027QTK	DFN3*3-8, small outline package, no leads	Tape and reel

SOP8 is packed with 2500 pieces/disc in braided packaging. Leadless DFN3\*3-8 is packed with 6000 pieces/disc in braided packaging.

**REFLOW SOLDERING**


Parameter	Lead-free soldering conditions
Ave ramp up rate ( $T_L$ to $T_P$ )	3 °C/second max
Preheat time $t_s$ ( $T_{smin}=150$ °C to $T_{smax}=200$ °C)	60-120 seconds
Melting time $t_L$ ( $T_L=217$ °C)	60-150 seconds
Peak temp $T_P$	260-265 °C
5°C below peak temperature $t_p$	30 seconds
Ave cooling rate ( $T_P$ to $T_L$ )	6 °C/second max
Normal temperature 25°C to peak temperature TP time	8 minutes max

**Important statement**

SIT reserves the right to change the above-mentioned information without prior notice.

**REVISION HISTORY**

Version number	Data sheet status	Revision Date
V1.0	Initial version.	September 2022
V1.1	Added SIT1027QTK pin configuration.	November 2022
V1.2	Added AEC-Q100 qualified; Added the limiting value of $T_{amb}$ ; Adjusted format.	July 2023
V1.3	Added the ESD limiting values; Updated the range of $V_{BAT}$ ; Updated static and dynamic characteristics.	February 2024

单击下面可查看定价，库存，交付和生命周期等信息

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