SiT3372

1 MHz to 220 MHz Ultra-low Jitter Differential VCXO

Description

The SiT3372 is a 1 MHz to 220 MHz differential MEMS VCXO engineered for low-jitter applications. Utilizing SiTime's unique DualMEMS® temperature sensing and TurboCompensation® technology, the SiT3372 delivers exceptional dynamic performance by providing resistance to airflow, thermal gradients, shock and vibration. This device also integrates multiple on-chip regulators to filter power supply noise, eliminating the need for a dedicated external LDO.

The SiT3372 can be factory programmed for any combination of frequency, stability, voltage, output signaling, and pull range. Programmability enables designers to optimize clock configurations while eliminating long lead times and customization costs associated with quartz devices where each frequency is custom built.

The wide frequency range and programmability makes this device ideal for telecom, networking, and industrial applications that require a variety of pullable frequencies and operate in noisy environments.

Refer to Manufacturing Notes for proper reflow profile, tape and reel dimension, and other manufacturing related information.

Features

- Any frequency between 1 MHz and 220 MHz accurate to 6 decimal places
  (For frequencies 220.000001 MHz to 725 MHz, refer to SiT3373)
- Widest pull range options: ±25, ±50, ±80, ±100, ±150, ±200, ±400, ±800, ±1600, ±3200 ppm
- 0.225 ps RMS phase jitter (typ) over 12 kHz to 20 MHz bandwidth
- Frequency stability as low as ±15 ppm
- Wide temperature range support from -40°C to 105°C
- Industry-standard packages: 7.0 x 5.0 mm, 5.0 x 3.2 mm, 3.2 x 2.5 mm packages

Applications

- Cable Modem Termination System (CMTS), Video, Broadcasting System, Audio, Industrial Sensors, Remote Radio Head (RRH)
- SATA, SAS, 10/40/100/400 Gbps Ethernet, Fibre Channel, PCI-Express

Block Diagram

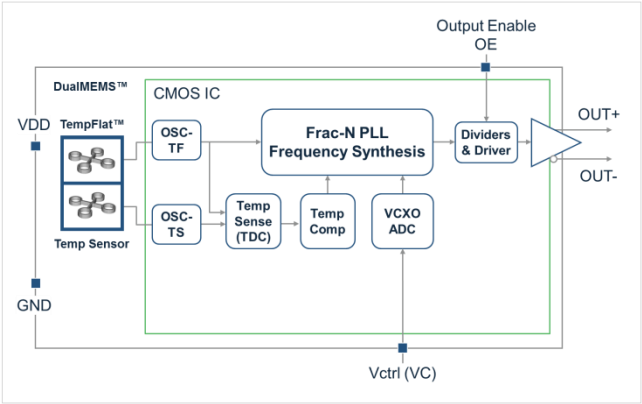


Figure 1. SiT3372 Block Diagram

3.2 x 2.5 mm Package Pinout

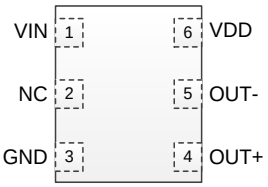
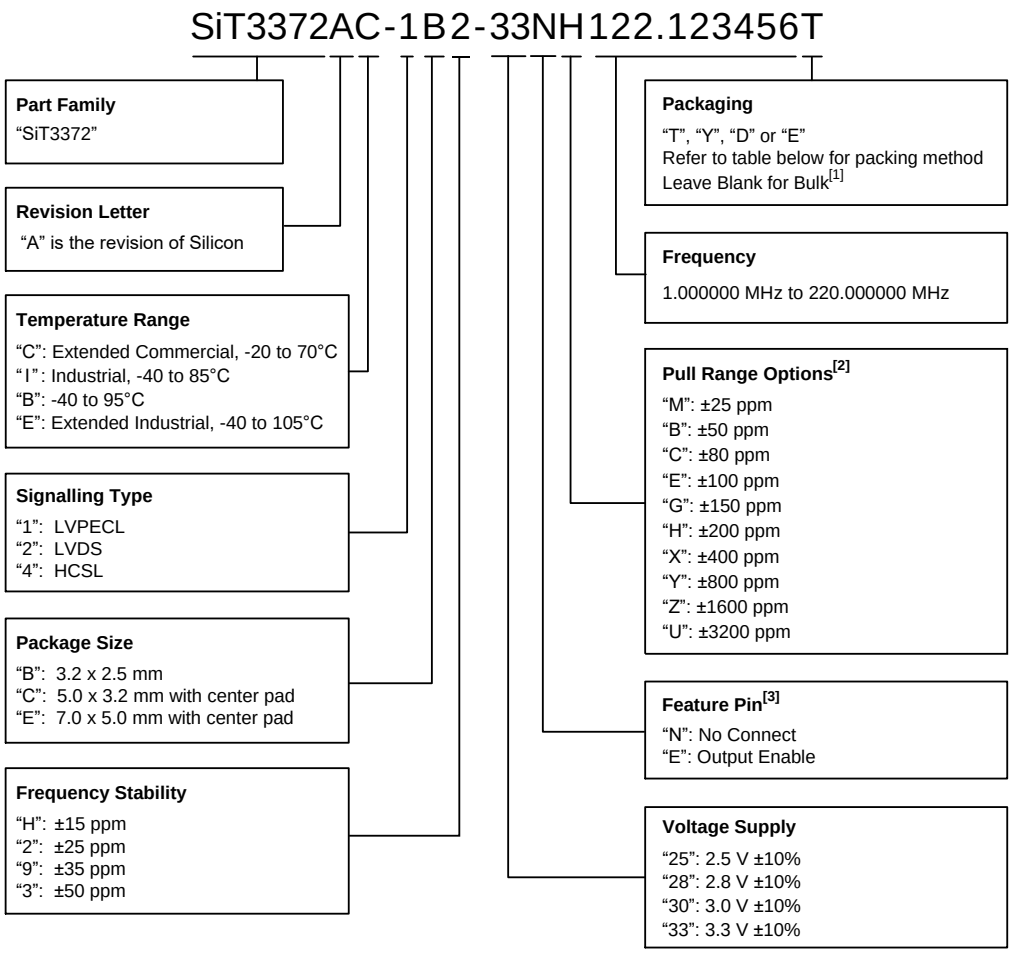


Figure 2. Pin Assignments (Top view)
(Refer to Table 6 for Pin Descriptions)

Ordering Information



Notes:

1. Bulk is available for sampling only.
2. Contact SiTime for custom pull range options.
3. "E": Output Enable function is only available in 7.0 x 5.0 mm and 5.0 x 3.2 mm packages.

Table 1. Ordering Codes for Supported Tape & Reel Packing Method

Device Size (mm x mm)	8 mm T&R (3ku)	8 mm T&R (1ku)	12 mm T&R (3ku)	12 mm T&R (1ku)	16 mm T&R (3ku)	16 mm T&R (1ku)
7.0 x 5.0	–	–	–	–	T	Y
5.0 x 3.2	–	–	T	Y	–	–
3.2 x 2.5	D	E	T	Y	–	–

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Electrical Characteristics

Table 2. Electrical Characteristics – Common to LVPECL, LVDS and HCSL

All Min and Max limits in the Electrical Characteristics tables are specified over temperature and rated operating voltage with standard output termination shown in the termination diagrams. Typical values are at 25°C and nominal supply voltage.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Frequency Range						
Output Frequency Range	f	1	–	220	MHz	Accurate to 6 decimal places
Frequency Stability						
Frequency Stability	F_stab	-15	–	+15	ppm	Inclusive of initial tolerance, operating temperature, rated power supply voltage, load variations, and first year aging at 25 °C, with VIN voltage at Vdd/2. ±15 ppm is only guaranteed for pull range up to ±100 ppm.
		-25	–	+25	ppm	
		-35	–	+35	ppm	
		-50	–	+50	ppm	
Temperature Range						
Operating Temperature Range	T_use	-20	–	+70	°C	Extended Commercial
		-40	–	+85	°C	Industrial
		-40	–	+95	°C	
		-40	–	+105	°C	Extended Industrial
Supply Voltage						
Supply Voltage	Vdd	2.97	3.3	3.63	V	
		2.7	3.0	3.3	V	
		2.52	2.8	3.08	V	
		2.25	2.5	2.75	V	
Voltage Control Characteristics						
Pull Range	PR	±25, ±50, ±80, ±100, ±150, ±200, ±400, ±800, ±1600, ±3200			ppm	See the APR (Absolute Pull Range) Table 11. Contact SiTime for custom pull range options
Upper Control Voltage	VC_U	90%	–	–	Vdd	Voltage at which maximum frequency deviation is guaranteed
Lower Control Voltage	VC_L	–	–	10%	Vdd	Voltage at which minimum frequency deviation is guaranteed
Control Voltage Input Impedance	VC_z	–	10	–	MΩ	
Control Voltage Input Bandwidth	V_c	–	10	–	kHz	Contact SiTime for other input bandwidth options
Pull Range Linearity	Lin	–	–	1.0	%	
Frequency Change Polarity	–	Positive Slope		–		
Input Characteristics						
Input Voltage High	VIH	70%	–	–	Vdd	Pin 2, OE
Input Voltage Low	VIL	–	–	30%	Vdd	Pin 2, OE
Input Pull-up Impedance	Z_in	–	100	-	kΩ	Pin 2, OE logic high or logic low
Output Characteristics						
Duty Cycle	DC	45	–	55	%	
Startup and OE Timing						
Startup Time	T_start	–	–	3.0	ms	Measured from the time Vdd reaches its rated minimum value
OE Enable/Disable Time	T_oe	–	–	3.8	µs	f = 156.25 MHz. Measured from the time OE pin reaches rated VIH and VIL to the time clock pins reach 90% of swing and high-Z. See Figure 9 and Figure 10

Table 3. Electrical Characteristics – LVPECL Specific

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption						
Current Consumption	Idd	–	78	92	mA	Excluding Load Termination Current, Vdd = 3.3 V or 2.5 V
OE Disable Supply Current	I_OE	–	53	61	mA	OE = Low
Output Disable Leakage Current	I_leak	–	0.15	–	µA	OE = Low
Maximum Output Current	I_driver	–	–	33	mA	Maximum average current drawn from OUT+ or OUT-
Output Characteristics						
Output High Voltage	VOH	Vdd-1.15	–	Vdd-0.7	V	See Figure 5
Output Low Voltage	VOL	Vdd-2.0	–	Vdd-1.5	V	See Figure 5
Output Differential Voltage Swing	V_Swing	1.2	1.6	2.0	V	See Figure 6
Rise/Fall Time	Tr, Tf	–	225	290	ps	20% to 80%, see Figure 6
Jitter – 7.0 x 5.0 mm package						
RMS Period Jitter[4]	T_jitt	–	1.0	1.6	ps	f = 100, 156.25 or 212.5 MHz, Vdd = 3.3 V or 2.5 V
RMS Phase Jitter (random)	T_phj	–	0.225	0.270	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels, includes spurs, pull range = ±100 ppm. Temperature ranges -20 to 70°C and -40 to 85°C
		–	0.225	0.300	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels, includes spurs, pull range = ±100 ppm. Temperature ranges -40 to 95°C and -40 to 105°C
		–	0.1	–	ps	f = 156.25 MHz, IEEE802.3-2005 10 GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, includes spurs, all Vdd levels
Jitter – 5.0 x 3.2 mm and 3.2 x 2.5 mm package						
RMS Period Jitter[4]	T_jitt	–	1.0	1.6	ps	f = 100, 156.25 or 212.5 MHz, Vdd = 3.3 V or 2.5 V
RMS Phase Jitter (random)	T_phj	–	0.225	0.275	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels, includes spurs, pull range = ±100 ppm. Temperature ranges -20 to 70°C and -40 to 85°C
		–	0.225	0.340	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels, includes spurs, pull range = ±100 ppm. Temperature ranges -40 to 95°C and -40 to 105°C
		–	0.1	–	ps	f = 156.25 MHz, IEEE802.3-2005 10 GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, includes spurs, all Vdd levels

Notes:

4. Measured according to JESD65B.

Table 4. Electrical Characteristics – LVDS

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption						
Current Consumption	Idd	–	73	84	mA	Excluding Load Termination Current, Vdd = 3.3 V or 2.5 V
OE Disable Supply Current	I_OE	–	55	62	mA	OE = Low
Output Disable Leakage Current	I_leak	–	0.15	–	µA	OE = Low
Output Characteristics						
Differential Output Voltage	VOD	250	–	450	mV	See Figure 7
Delta VOD	ΔVOD	–	–	50	mV	See Figure 7
Offset Voltage	VOS	1.125	–	1.375	V	See Figure 7
Delta VOS	ΔVOS	–	–	50	mV	See Figure 7
Rise/Fall Time	Tr, Tf	–	400	470	ps	Measured with 2 pF capacitive loading to GND, 20% to 80%, see Figure 8
Jitter – 7.0 x 5.0 mm package						
RMS Period Jitter[5]	T_jitt	–	1.0	1.6	ps	f = 100, 156.25 or 212.5 MHz, Vdd = 3.3 V or 2.5 V
RMS Phase Jitter (random)	T_phj	–	0.215	0.265	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels, includes spurs, pull range = ±100 ppm. Temperature ranges -20 to 70°C and -40 to 85°C
		–	0.215	0.300	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels, includes spurs, pull range = ±100 ppm. Temperature ranges -40 to 95°C and -40 to 105°C
		–	0.1	–	ps	f = 156.25 MHz, IEEE802.3-2005 10 GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, includes spurs, all Vdd levels
Jitter – 5.0 x 3.2 mm and 3.2 x 2.5 mm package						
RMS Period Jitter[5]	T_jitt	–	1.0	1.6	ps	f = 100, 156.25 or 212.5 MHz, Vdd = 3.3 V or 2.5 V
RMS Phase Jitter (random)	T_phj	–	0.235	0.275	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels, includes spurs, pull range = ±100 ppm. Temperature ranges -20 to 70°C and -40 to 85°C
		–	0.235	0.320	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels, includes spurs, pull range = ±100 ppm. Temperature ranges -40 to 95°C and -40 to 105°C
		–	0.1	–	ps	f = 156.25 MHz, IEEE802.3-2005 10 GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, includes spurs, all Vdd levels

Notes:
5. Measured according to JESD65B.

Table 5. Electrical Characteristics – HCSL

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption						
Current Consumption	Idd	–	83	97	mA	Excluding Load Termination Current, Vdd = 3.3 V or 2.5 V
OE Disable Supply Current	I_OE	–	55	62	mA	OE = Low
Output Disable Leakage Current	I_leak	–	0.15	–	µA	OE = Low
Output Characteristics						
Output High Voltage	VOH	0.60	–	0.90	V	See Figure 5
Output Low Voltage	VOL	-0.05	–	0.08	V	See Figure 5
Output Differential Voltage Swing	V_Swing	1.2	1.4	1.80	V	See Figure 6
Rise/Fall Time	Tr, Tf	–	360	495	ps	Measured with 2 pF capacitive loading to GND, 20% to 80%, See Figure 6
Jitter – 7.0 x 5.0 mm package						
RMS Period Jitter[6]	T_jitt	–	1.0	1.6	ps	f = 100, 156.25 or 212.5 MHz, Vdd = 3.3 V or 2.5 V
RMS Phase Jitter (random)	T_phj	–	0.220	0.270	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels, includes spurs, pull range = ±100 ppm. Temperature ranges -20 to 70°C and -40 to 85°C
		–	0.220	0.300	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels, includes spurs, pull range = ±100 ppm. Temperature ranges -40 to 95°C and -40 to 105°C
		–	0.1	–	ps	f = 156.25 MHz, IEEE802.3-2005 10 GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, includes spurs, all Vdd levels
Jitter – 5.0 x 3.2 mm and 3.2 x 2.5 mm package						
RMS Period Jitter[6]	T_jitt	–	1.0	1.6	ps	f = 100, 156.25 or 212.5 MHz, Vdd = 3.3 V or 2.5 V
RMS Phase Jitter (random)	T_phj	–	0.230	0.275	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels, includes spurs, pull range = ±100 ppm. Temperature ranges -20 to 70°C and -40 to 85°C
		–	0.230	0.340	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels, includes spurs, pull range = ±100 ppm. Temperature ranges -40 to 95°C and -40 to 105°C
		–	0.1	–	ps	f = 156.25 MHz, IEEE802.3-2005 10 GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, includes spurs, all Vdd levels

Notes:
6. Measured according to JESD65B.

Table 6. Pin Description

Pin	Symbol	Functionality	
1	VIN	Input	Control Voltage
2	NC/OE	No Connect (NC)	No Connect: Leave floating or connect to GND for better heat dissipation. NC for all 3.2 x 2.5 mm package options.
		Output Enable (OE)	H[7,8]: specified frequency output L: output is high impedance. Only output driver is disabled. OE function only available on 7050 package. Pin 2 on 3225 package is NC.
3	GND	Power	Vdd Power Supply Ground
4	OUT+	Output	Oscillator output
5	OUT-	Output	Complementary oscillator output
6	VDD	Power	Power supply voltage[9]

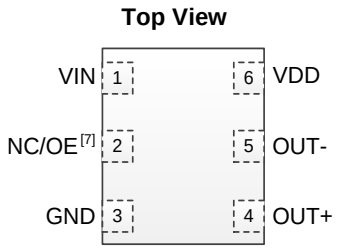


Figure 3. Pin Assignments (7.0 x 5.0 mm and 5.0 x 3.2 mm packages)

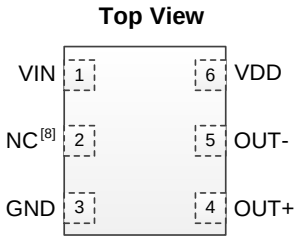


Figure 4. Pin Assignments (3.2 x 2.5 mm package)

Notes:

7. A pull-up resistor of 10 kΩ or less is recommended if pin 1 is not externally driven.
8. OE mode is only available in the 7050 and 5032 packages. 3225 package is NC.
9. A capacitor of value 0.1 µF or higher between VDD and GND is required. An additional 10 µF capacitor between VDD and GND is required for the best phase jitter performance.

Table 7. Absolute Maximum Ratings

Attempted operation outside the absolute maximum ratings may cause permanent damage to the part.
Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Min.	Max.	Unit
Continuous Power Supply Voltage Range (Vdd)	-0.5	4.0	V
Input Voltage, Maximum (any input pin)		Vdd + 0.3V	V
Input Voltage, Minimum (any input pin)	-0.3		V
Storage Temperature	-65	150	°C
Maximum Junction Temperature		145	°C
Soldering Temperature (follow standard Pb-free soldering guidelines)		260	°C

Table 8. Thermal Considerations[10]

Package	θ_{JA}, 4 Layer Board (°C/W)	θ_{JC}, Bottom (°C/W)
3225, 6-pin	80	30
5032, 6-pin	53[11]	20
7050, 6-pin	52[11]	19

Notes:

10. Refer to JESD51 for θ_{JA} and θ_{JC} definitions, and reference layout used to determine the θ_{JA} and θ_{JC} values in the above table.
11. Value for θ_{JA} assumes the center pad is soldered down.

Table 9. Maximum Operating Junction Temperature[12]

Max Operating Temperature (ambient)	Maximum Operating Junction Temperature: 3225 Package	Maximum Operating Junction Temperature: 5032, 7050 Packages
70°C	105°C	95°C
85°C	130°C	110°C
95°C	130°C	120°C
105°C	145°C	130°C

Notes:

12. Datasheet specifications are not guaranteed if junction temperature exceeds the maximum operating junction temperature.

Table 10. Environmental Compliance

Parameter	Test Conditions	Value	Unit
Mechanical Shock Resistance	**MIL-STD-883F, Method 2002**	10,000	*g*
Mechanical Vibration Resistance	**MIL-STD-883F, Method 2007**	70	*g*
Soldering Temperature (follow standard Pb free soldering guidelines)	**MIL-STD-883F, Method 2003**	260	°C
Moisture Sensitivity Level	**MSL1 @ 260°C**		
Electrostatic Discharge (HBM)	**HBM, JESD22-A114**	2,000	V
Charge-Device Model ESD Protection	**JESD220C101**	750	V
Latch-up Tolerance	**JESD78 Compliant**		

Waveform Diagrams

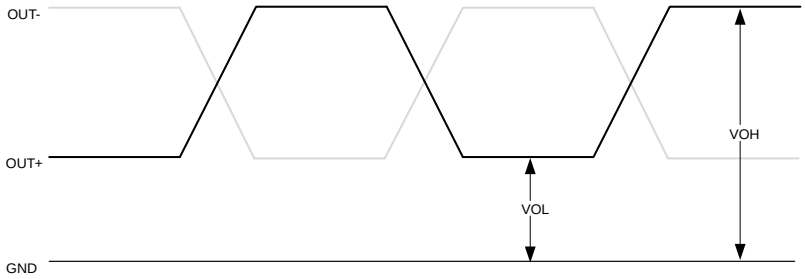


Figure 5. LVPECL, HCSL Voltage Levels per Differential Pin (i.e. OUT+, or OUT-)

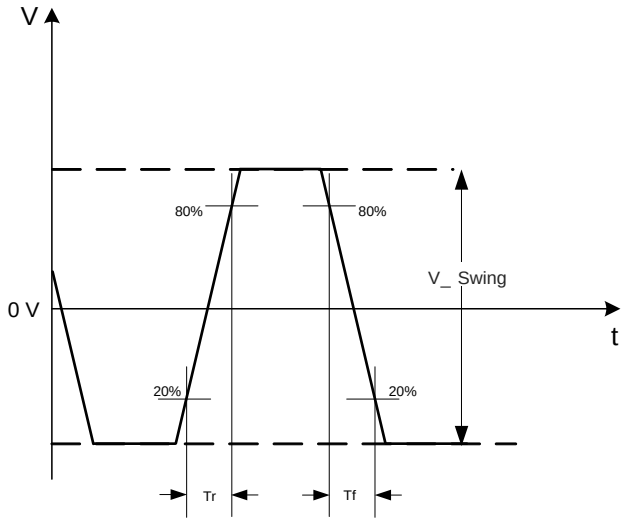


Figure 6. LVPECL, HCSL Voltage Levels across Differential Pair (i.e. OUT+ minus OUT-)

Waveform Diagrams (continued)

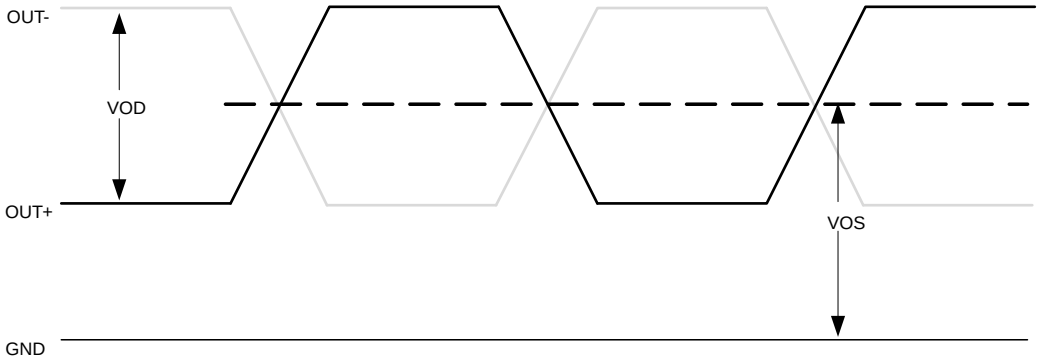


Figure 7. LVDS Voltage Levels per Differential Pin (OUT+, or OUT-)

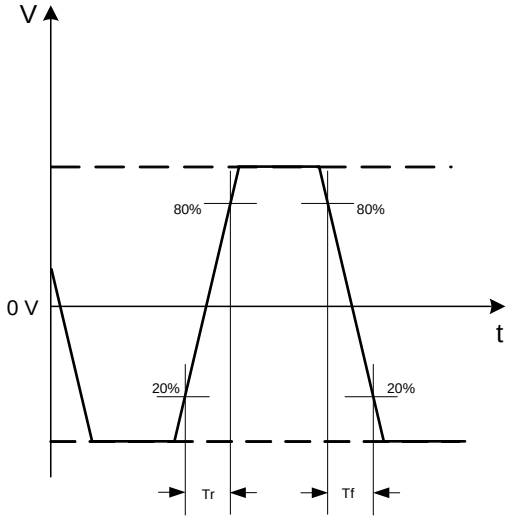


Figure 8. LVDS Differential Waveform (i.e. OUT+ minus OUT-)

Timing Diagrams

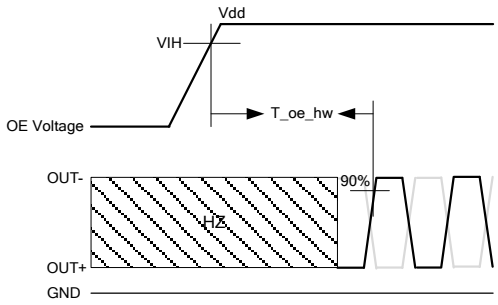


Figure 9. Hardware OE Enable Timing

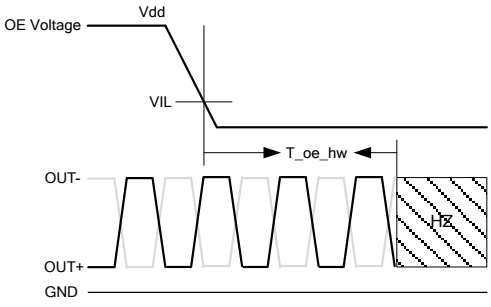


Figure 10. Hardware OE Disable Timing

Termination Diagrams

LVPECL

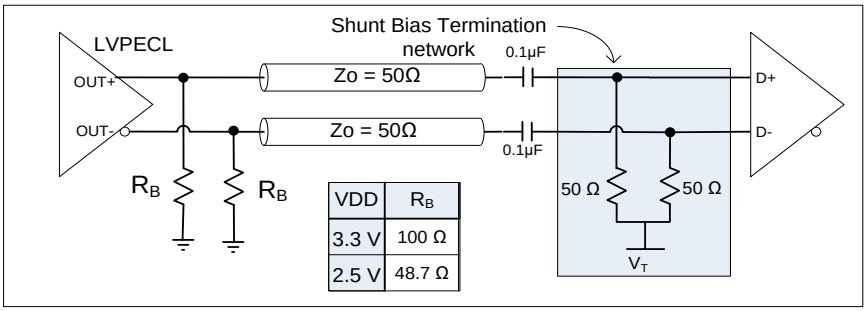


Figure 11. LVPECL with AC-coupled termination

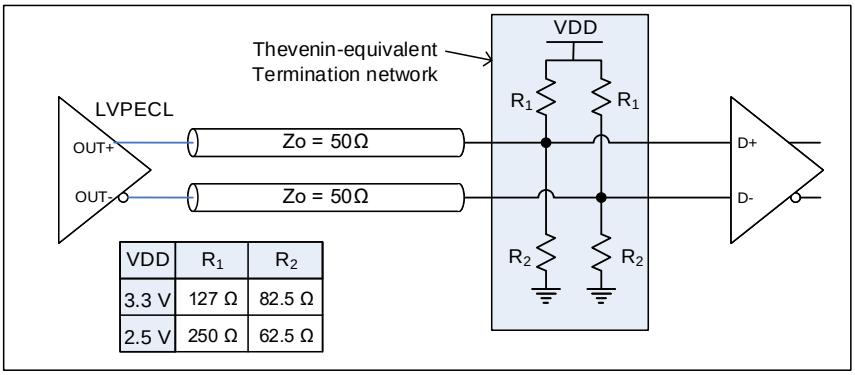


Figure 12. LVPECL DC-coupled load termination with Thevenin equivalent network

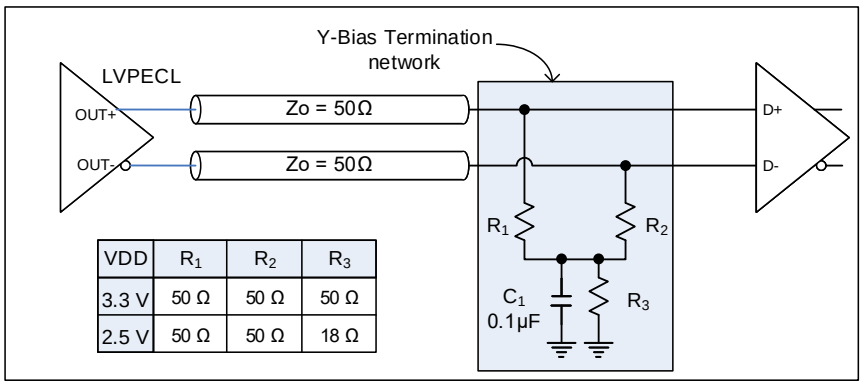


Figure 13. LVPECL with Y-Bias termination

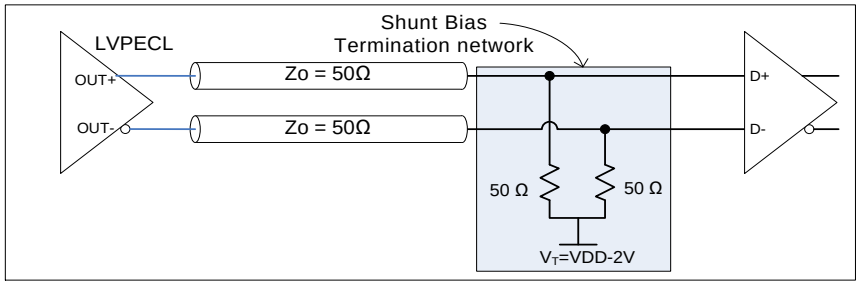


Figure 14. LVPECL with DC-coupled parallel shunt load termination

Termination Diagrams (continued)

LVDS

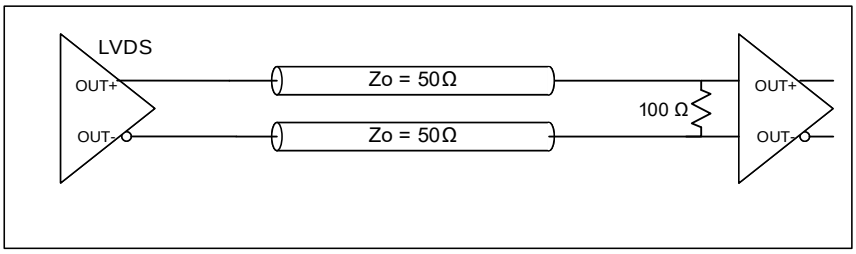


Figure 15. LVDS single DC termination at the load

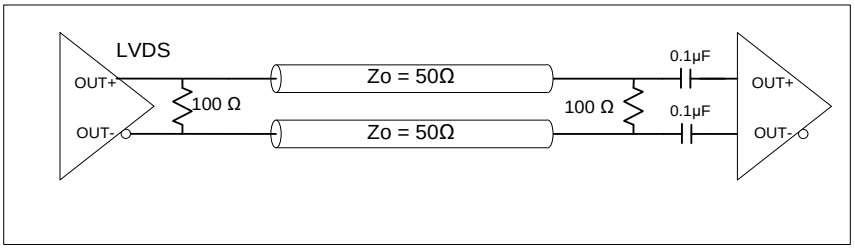


Figure 16. LVDS double AC termination with capacitor close to the load

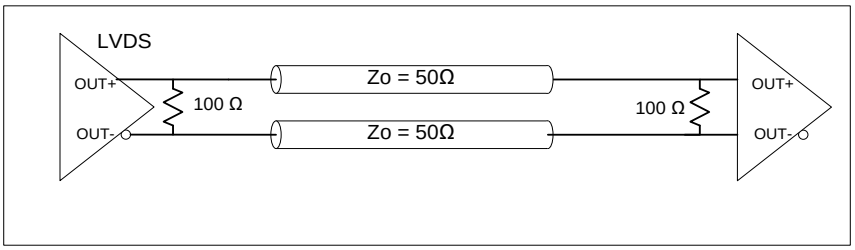


Figure 17. LVDS double DC termination

HCSL

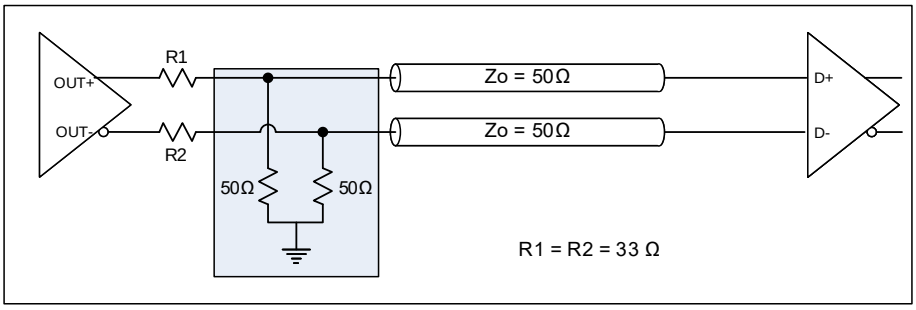
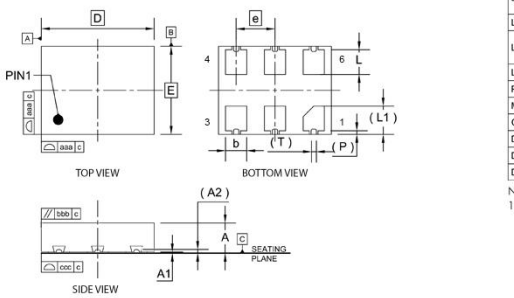


Figure 18. HCSL interface termination

Dimensions and Patterns — 3.2 x 2.5 mm

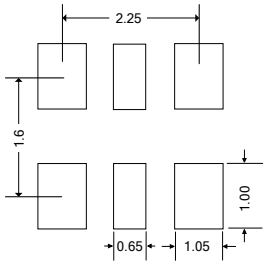
Package Size – Dimensions (Unit: mm)[13]	Recommended Land Pattern (Unit: mm)[14]
3.2 x 2.5 x 0.85 mm	**3.2 x 2.5 x 0.85 mm**



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.800	0.850	0.900
STAND OFF		A1	0.000	0.035	0.050
BODY SIZE	X	D		3.200 BSC	
	Y	E		2.500 BSC	
LEAD WIDTH		b	0.550	0.600	0.650
LEAD LENGTH		L	0.650	0.700	0.750
		L1		0.800 REF	
LEAD PITCH		e		1.100 BSC	
PACKAGE TOLERNCE		aaa		0.100	
MOLD FLATNESS		bbb		0.100	
COPLANARITY		ccc		0.080	
DIMPLE WIDTH		T		0.150 REF	
DIMPLE LENGTH		P		0.150 REF	
DIMPLE DEPTH		A2		0.100 REF	

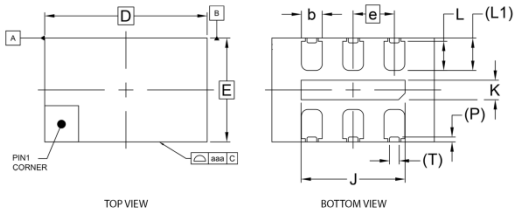
Notes
1. All dimensions are in millimeters

Package Outline	
6L PQFD	POD-038-PQFD-006-C03225
3.200x2.500x0.850 mm	SiTime
2021/07/15 Rev C00	



Dimensions and Patterns — 5.0 x 3.2 mm

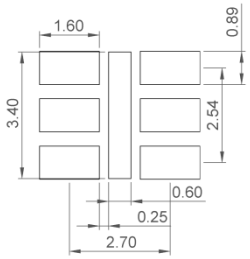
Package Size – Dimensions (Unit: mm)[13]	Recommended Land Pattern (Unit: mm)[14]
5.0 x 3.2 x 0.85 mm[15]	**5.0 x 3.2 x 0.85 mm[15]**



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.800	0.850	0.900
STAND OFF		A1	0.000	0.035	0.050
BODY SIZE	X	D		5.000 BSC	
	Y	E		3.200 BSC	
EP SIZE	X	J	3.100	3.200	3.300
	Y	K	0.500	0.600	0.700
LEAD WIDTH		b	0.590	0.640	0.690
LEAD LENGTH		L	0.850	0.900	0.950
		L1		1.000 REF	
LEAD PITCH		e		1.270 BSC	
PACKAGE TOLERANCE		aaa		0.100	
MOLD FLATNESS		bbb		0.100	
COPLANRITY		ccc		0.080	
DIMPLE WIDTH		T		0.300 REF	
DIMPLE LENGTH		P		0.150 REF	
DIMPLE DEPTH		A2		0.100 REF	

Notes
1. Dimensioning and tolerancing conform to ASME Y14.5-2009
2. All dimensions are in millimeters

Package Outline	
6L PQFV	POD-PQFV-006-C05032-039
5.000x3.200x0.850 mm	SiTime
2019/03/13 Rev B00	



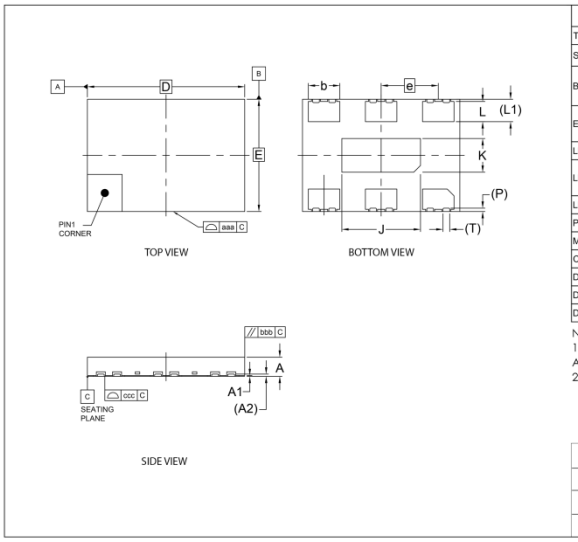
Notes:

13. Top Marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of "Y" will depend on the assembly location of the device.
14. A capacitor of value 0.1 µF or higher between VDD and GND is required. An additional 10 µF capacitor between VDD and GND is required for the best phase jitter performance.
15. The center pad is internally connected to the GND pin. Soldering down the center pad to the GND is recommended for best thermal dissipation, but is optional.

Dimensions and Patterns — 7.0 x 5.0 mm

Package Size – Dimensions (Unit: mm)[16]	Recommended Land Pattern (Unit: mm)[17]

7.0 x 5.0 x 0.85 mm[18]

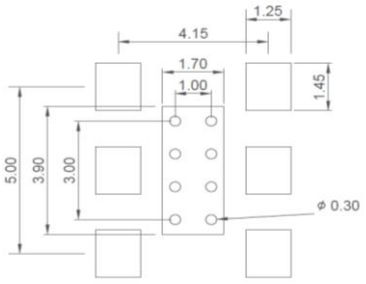


		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.800	0.850	0.900
STAND OFF		A1	0.000	0.035	0.050
BODY SIZE	X	D		7.000 BSC	
	Y	E		5.000 BSC	
EP SIZE	X	J	3.400	3.500	3.600
	Y	K	1.400	1.500	1.600
LEAD WIDTH		b	1.350	1.400	1.450
LEAD LENGTH		L	0.850	0.900	0.950
		L1		1.000 REF	
LEAD PITCH		e		2.540 BSC	
PACKAGE TOLERANCE		aaa		0.100	
MOLD FLATNESS		bbb		0.100	
COPLANRITY		ccc		0.080	
DIMPLE WIDTH		T		0.300 REF	
DIMPLE LENGTH		P		0.150 REF	
DIMPLE DEPTH		A2		0.100 REF	

Notes
1. Dimensioning and tolerancing conform to ASME Y14.5-2009
2. All dimensions are in millimeters

Package Outline	
6L PQFV	POD-PQFV-006-C07050-037
7.000x5.000x0.850 mm	SiTime
2019/03/13 Rev B00	

7.0 x 5.0 x 0.85 mm[18]



Note:
Circles in center pad are thermal vias, recommended to improve thermal performance

Notes:

16. Top Marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of “Y” will depend on the assembly location of the device.
17. A capacitor of value 0.1 µF or higher between VDD and GND is required. An additional 10 µF capacitor between VDD and GND is required for the best phase jitter performance.
18. The center pad is internally connected to the GND pin. Soldering down the center pad to the GND is recommended for best thermal dissipation, but is optional.

Table 11. APR Table

Absolute pull range (APR) = Nominal pull range (PR) - frequency stability (F_stab)-aging[19]

Nominal Pull Range	Frequency Stability			
	±15	±25	±35	±50
	APR (ppm)			
±25	±5	–	–	–
±50	±30	±20	±10	–
±80	±60	±50	±40	±25
±100	±80	±70	±60	±45
±150	–	±120	±110	±95
±200	–	±170	±160	±145
±400	–	±370	±360	±345
±800	–	±770	±760	±745
±1600	–	±1570	±1560	±1545
±3200	–	±3170	±3160	±3145

Note:
19. Aging includes solder down shift and 20-year aging.

Additional Information

Table 12. Additional Information

Document	Description	Download Link
ECCN #: EAR99	Five character designation used on the commerce Control List (CCL) to identify dual use items for export control purposes.	—
HTS Classification Code: 8542.39.0000	A Harmonized Tariff Schedule (HTS) code developed by the World Customs Organization to classify/define internationally traded goods.	—
Part number Generator	Tool used to create the part number based on desired features.	https://www.sitime.com/part-number-generator
Time Machine II	MEMS oscillator programmer	http://www.sitime.com/support/time-machine-oscillator-programmer
Manufacturing Notes	Tape & Reel dimension, reflow profile and other manufacturing related info	https://www.sitime.com/sites/default/files/gated/Manufacturing-Notes-for-SiTime-Products.pdf
Qualification Reports	RoHS report, reliability reports, composition reports	http://www.sitime.com/support/quality-and-reliability
Performance Reports	Additional performance data such as phase noise, current consumption and jitter for selected frequencies	http://www.sitime.com/support/performance-measurement-report
Termination Techniques	AN10029 Termination design recommendations	http://www.sitime.com/support/application-notes
Layout Techniques	AN10006 Layout recommendations	http://www.sitime.com/support/application-notes
Evaluation Boards	SiT6085EB, SiT6086EB and SiT6097EB for Differential Oscillators	https://www.sitime.com/support/user-guides

Revision History

Table 13. Revision History

Revision	Release Date	Change Summary
1.0	13-Oct-2017	Initial release
1.03	10-May-2018	Updated the Part Ordering info with added 5.0 x 3.2 mm package
1.04	29-Oct-2018	±15 ppm option
1.05	7-Jun-2020	Formatting updates Corrected typos Updated package Dimensions Drawings Updated Table 8 Thermal Considerations for 5032 package Added Evaluation Boards SiT6085EB reference in Additional Information Rearranged layout, added Description, Block Diagram and TOC Added HTS classification code Clarified ±15 ppm pull range up to ±100 ppm Modified maximum junction temperatures Removed I_driver HCSL specification as not applicable
1.06	17-Mar-2021	Updated L1 and Dimple Width package dimensions for 3.2 x 2.5 mm package Updated trademarks and changed rev table date format
1.07	20-Jul-2021	Updated pin direction in package dimensions for 3.2 x 2.5 mm package

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单击下面可查看定价，库存，交付和生命周期等信息

>>SiTime(赛特时脉)