



# SC8915 High Efficiency, Synchronous, Bi-Directional Buck-Boost Charge Converter with I2C Interface

## 1 Description

SC8915 is a synchronous buck-boost Li-ion battery charger which also supports reverse discharging operation. It integrates two power MOSFETs and can support up to 36V battery voltage and up to 26V VBUS. It can be used to effectively manage the charging process for 1~6 cell Li-ion batteries no matter adapter voltage is higher, lower or equal to the battery voltage. When a system needs to generate an output from the battery, SC8915 can also discharge the cells and delivers desired output no matter it is higher, lower or equal to the battery voltage.

Through its I2C interface, user can set the charging / discharging mode easily, and program the charging current, charging voltage, reserve output voltage, current limits, switching frequency and other parameters flexibly. Besides that, SC8915 integrates 10-bit ADC, so user can read the VBUS / VBAT voltage and current in real time, simplifying the system design.

SC8915 supports internal current limit, over voltage protection, output short protection and over temperature protections to ensure safety under different abnormal conditions.

SC8915 adopts 40 pin QFN 6x6 package.

## 3 Applications

- Power Bank
- USB Power Delivery
- Type C Hub
- Industrial Power Supplies

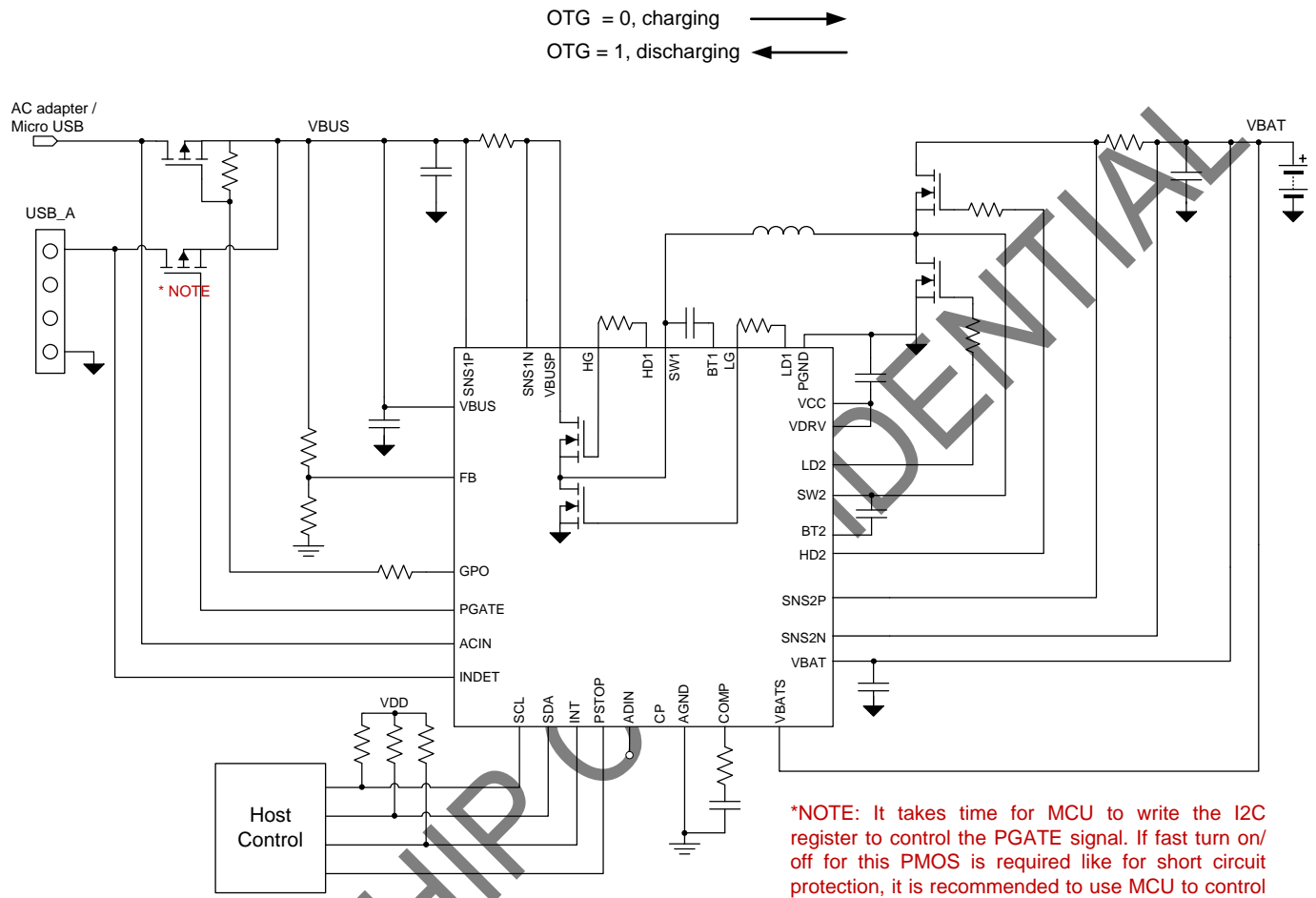
## 2 Features

- Buck-Boost Battery Charger for 1 to 6 Cell Batteries
- Charging Management including Trickle Charge, CC Charge, CV Charge and Charge Termination
- Buck-Boost Reverse Discharging Mode
- Integrates Two Power MOSFETs
- Wide V<sub>BAT</sub> Range: 2.5 V to 36 V, 40V sustainable
- Wide V<sub>BUS</sub> Range: 2.5 V to 26 V, 30V sustainable
- I2C Programmable Charging Current and Voltage
- I2C Programmable Discharging Output Voltage
- I2C Programmable Input / Output Current Limit
- I2C Programmable Switching Frequency
- High Efficiency Buck-Boost Conversion
- 10-bit ADC resources
- Charging Status Indication
- Event Detections, including Automatic Adapter Insert and Automatic Load Insert Detection
- Power Path Control
- Under Voltage Protection, Over Voltage Protection, Over Current Protection, Short Circuit Protection and Thermal Shutdown Protection
- QFN-40 Package

## 4 Device Information

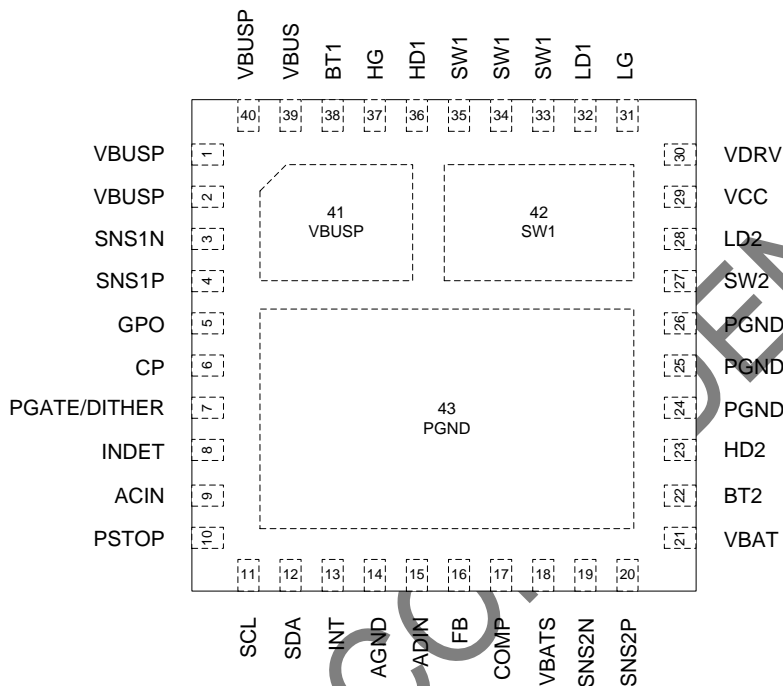
Part Number	Package	Dimension
SC8915QDHR	40 pin QFN	6.0mm x 6.0mm x 0.75mm

## 5 Typical Application Circuit



## 6 Terminal Configuration and Functions

**SC8915**  
Top View



TERMINAL		I/O	DESCRIPTION
NUMBER	NAME		
1, 2, 40	VBUSP	I/O	Power node of VBUS. Connect to adapter input port or USB port. Work as the power input of the converter when in charging mode, and power output in discharging mode.
3	SNS1N	I	Negative input of a current sense amplifier. Connect to one pad of the current sense resistor (typical 10 mΩ) on the power path to sense the current into or out from VBUS.
4	SNS1P	I	Positive input of a current sense amplifier. Connect to one pad of the current sense resistor (typical 10 mΩ) on the power path to sense the current into or out from VBUS.
5	GPO	O	Open drain output for general purpose. It is controlled by GPO_CTRL bit. User can use this pin to drive external PMOS with a pull up resistor.
6	CP	O	Driver for external charge pump circuit. <b>(CHARGE PUMP NOT RECOMMENDED. It is suggested to leave this pin floating, and connect VDRV with VCC. Consult local FAE if charge pump is needed)</b>
7	PGATE/DITHER	IO	PMOS gate driver controlled by PGATE bit, used to control the external PMOS on the power path. This pin can be configured through I2C for switching frequency dithering function. Connect a ceramic capacitor (typical 100nF) from this pin to ground when for frequency dither function.
8	INDET	I	Connect this pin to a USB-A port to detect the load insertion event. When an insertion event is

			detected, the IC sets INDET bit and outputs an INT interrupt pulse to inform MCU.
9	ACIN	I	Connect this pin to AC adapter input node or micro-USB port to detect an AC adapter insertion event. When an insertion event is detected, the IC sets AC_OK bit and outputs an INT interrupt pulse to inform MCU.
10	PSTOP	I	Power stop control. Pull this pin to logic low to enable the power blocks; pull this pin to logic high to disabled the power blocks, and the IC enters into Standby mode. In Standby mode, only the AC adapter and load insert detection functions and the I2C circuits keep working.  This pin is internally pulled low.
11	SCL	I	I2C interface clock. Connect SCL to the logic rail through a pull up resistor (typical 10 kΩ). The IC works as a slave, and the I2C address is 0x74H.
12	SDA	I/O	I2C interface data. Connect SDA to the logic rail through a pull up resistor (typical 10 kΩ).
13	INT	O	An open drain output for interrupt signal. The IC sends a logic low pulse at INT pin to inform the host if an interrupt event happens.
14	AGND	I/O	Analog ground. Connect PGND and AGND together at the thermal pad under IC.
15	ADIN	I	ADC input pin. Apply an analog signal ( $\leq 2.048V$ ) to this pin, the internal 10-bit ADC can convert this analog signal to digital signals, and store the digital values in a register.
16	FB	I	Feedback node for VBUS voltage. Connect a resistor divider from VBUS to FB to set the VBUS discharging output voltage in external way. The FB reference can also be programmed through I2C.
17	COMP	I	Connect resistor and capacitor at this pin to compensate the control loop.
18	VBATS	I	Sense node for VBAT voltage. Connect to VBAT rail if internal way is selected for VBAT charging termination voltage setting; connect a resistor divider at VBATS if external way is selected.
19	SNS2N	I	Negative input of a current sense amplifier. Connect to one pad of the current sense resistor (typical 10 mΩ) on the power path to sense the current into or out from battery.
20	SNS2P	I	Positive input of a current sense amplifier. Connect to the other pad of the current sense resistor (typical 10 mΩ) on the power path to sense the current into or out from battery.
21	VBAT	I	Power supply to the IC. Connect to the battery positive node. Place a 1 μF capacitor from this pin to PGND as close to the IC as possible.
22	BT2	I	Connect a 100nF capacitor between BT2 pin and SW2 pin to bootstrap a bias voltage for high side MOSFET driver.
23	HD2	O	Gate driver output to control the external high side power MOSFET.
24-26	PGND	I/O	Power ground. Connect PGND and AGND together at the PGND thermal pad under IC.
27	SW2	I/O	Switching node. Connect to the inductor.
28	LD2	O	Gate driver output to control the external low side power MOSFET.
29	VCC	O	Output of an internal 5V linear regulator. Connect a 1 μF capacitor from VCC pin to PGND as close to the IC as possible.
30	VDRV	I	Power supply input for internal driver circuits. One way of getting the power supply is to connect VCC to this pin directly. Another way is to use the CP driver to implement a charge pump between VCC and VDRV pin. <b>(CHARGE PUMP WAY IS NOT RECOMMENDED. CONSULT LOCAL FAE IF CHARGE PUMP IS USED)</b>



31	LG	I	Gate input of the integrated low side MOSFET. Connect to LD1 pin with or without a driving resistor in between.
32	LD1	O	Gate driver output to the integrated low side MOSFET. User can short LD1 pin and LG pin directly, or connect a driving resistor between LD1 and LG pins to limit the driver current.
33 – 35	SW1	I/O	Switching Node. Connect to the inductor.
36	HD1	O	Gate driver output to the integrated high side MOSFET. User can short HD1 pin and HG pin directly, or connect a driving resistor between HD and HG pins to limit the driver current.
37	HG	I	Gate input of the integrated high side MOSFET. Connect to HD1 pin with or without a driving resistor in between.
38	BT1	I	Connect a 100nF capacitor between BT1 pin and SW1 pins to bootstrap a bias voltage for high side MOSFET driver.
39	VBUS	I	Power supply to the IC. Connect to the VBUS rail. Place a 1 $\mu$ F capacitor from this pin to PGND as close to the IC as possible.
41	VBUSP	I/O	VBUSP thermal pad under IC. Connect to VBUSP pins together.
42	SW1	I/O	Switching thermal pad under IC. Connect to SW1 pins together.
43	PGND	I/O	PGND thermal pad under IC. Connect to PGND pins together. Connect AGND and PGND together at this thermal pad.

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

		MIN	MAX	Unit
Voltage range at terminals <sup>(2)</sup>	CP, VCC, VDRV, LD1, LD2, LG, HD1 to SW1, HG to SW1, BT1 to SW1, BT2 to SW2, HD2 to SW2	-0.3	6.5	V
	PSTOP	-0.3	6	V
	SCL, SDA, INT, ADIN, COMP	-0.3	5	V
	VBUSP, SNS1N, SNS1P, FB, SW1	-0.3	30	V
	VBUS to SNS1P, SNS1N	-0.3	11	V
	VBAT to SNS2P, SNS2N	-0.3	11	V
	SNS1P to SNS1N	-10	10	V
	SNS2P to SNS2N	-10	10	V
	HD1, BT1	-0.3	35	V
	GPO, PGATE, INDET, ACIN, VBATS, SNS2N, SNS2P, VBAT, SW2	-0.3	40	V
	HD2, BT2	-0.3	45	V
	BT1 to HD1, BT2 to HD2	-0.3	6.5	V
T <sub>J</sub>	Operating junction temperature range	-40	150	°C
T <sub>stg</sub>	Storage temperature range	-65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

### 7.2 Thermal Information

THERMAL RESISTANCE <sup>(1)</sup>		QFN-40 (6mmX6mm)	UNIT
θ <sub>JA</sub>	Junction to ambient thermal resistance	58	°C/W
θ <sub>JC</sub>	Junction to case resistance	5	°C/W

(1) Measured on JESD51-7, 4-layer PCB.

### 7.3 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
ESD <sup>(1)</sup>	Human body model (HBM) ESD stress voltage <sup>(2)</sup>	-2	2	kV
	Charged device model (CDM) ESD stress voltage <sup>(3)</sup>	-750	750	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.4 Recommended Operating Conditions

		MIN	MAX	UNIT

V <sub>BUS</sub>	VBUS voltage range	2.7	26	V
V <sub>BAT</sub>	VBAT voltage range	2.6	36	V
C <sub>BUS</sub> , C <sub>BAT</sub>	Bulk capacitor for VBUS/VBAT (effective value)	30		μF
L	Inductance	2.2	10	μH
R <sub>SNS1/2</sub>	Current Sensing Resistor	5	10	mΩ
T <sub>A</sub>	Operating ambient temperature	-40	85	°C
T <sub>J</sub>	Operating junction temperature	-40	125	°C

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## 7.5 Electrical Characteristics

T<sub>J</sub> = 25°C and V<sub>BUS</sub> = 5V, V<sub>BAT</sub> = 10.8V unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
<b>SUPPLY VOLTAGE</b>						
V <sub>UVLO_VBUS</sub>	VBUS under-voltage lockout threshold	Rising edge	2.5	2.7	V	
		Hysteresis	170		mV	
V <sub>UVLO_VBAT</sub>	VBAT under-voltage lockout threshold	Rising edge	2.4	2.6	V	
		Hysteresis	170		mV	
I <sub>Q_VBAT</sub>	Quiescent current into VBAT	VBUS = 5V PSTOP = L, non-switching	2.4	4	mA	
		VBUS = 5V PSTOP = L, after charging termination	2.4	4	mA	
I <sub>Q_VBUS</sub>	Quiescent current into VBUS	PSTOP = L, non-switching	25	40	μA	
I <sub>SB_VBAT</sub>	Standby current into VBAT	VBUS open PSTOP = H, AD_START = 0	17	40	μA	
		VBUS open PSTOP = H, AD_START = 1	0.65	1.2	mA	
I <sub>SB_VBUS</sub>	Standby current into VBUS	PSTOP = H, AD_START = 0	12	50	μA	
<b>VCC, DRIVER AND POWER SWITCH</b>						
V <sub>CC</sub>	VCC regulation voltage	PSTOP = L, VBUS = 9V	5.0	5.3	V	
		PSTOP = L, VBUS = 5V	4.96	5	V	
		PSTOP = H, VBAT = 3.6V		3	V	
I <sub>VCC_LIM</sub>	VCC current limit	PSTOP = L VBUS = 5V, VCC = 4.5V	17	25	30	mA
		PSTOP = L VBUS = 9V, VCC = 4.5V		160		mA
		PSTOP = H			1	mA
V <sub>DRV</sub>	VDRV regulation voltage	change pump connected VBUS = 5V, IDRIV = 0mA	5.8	6.2	6.5	V
		change pump connected VBUS = 9V, IDRIV = 30mA	5.7	6.1	6.4	V
R <sub>HLS_PU</sub>	High/low side MOS driver pull up resistor		4		Ω	
R <sub>HLS_PD</sub>	High/low side MOS driver pull down resistor		1		Ω	
R <sub>DSon_HS</sub>	High side MOS on resistance	VDRV = 6V	9	10	mΩ	
R <sub>DSon_LS</sub>	Low side MOS on resistance	VDRV = 6V	9	10	mΩ	
<b>REFERENCE VOLTAGE IN CHARGING MODE</b>						
V <sub>BATS_ext</sub>	VBATS reference voltage for external setting	VBAT_SEL = 1	1.197	1.203	1.209	V
V <sub>BATS_int</sub>	VBATS accuracy for internal setting, over VBATS target	VBAT_SEL = 0, CSEL = 00 VCELL_SET = 000~111	-0.5		0.5	%
V <sub>TRICKLE_int</sub>	Trickle charge threshold voltage for internal setting	VBAT_SEL = 0, Cell number = N VCELL_SET = 000~1111, TRICKLE_SET = 0	2.73*N	2.94*N	3.15*N	V





		VBAT_SEL = 0, Cell number = N VCELL_SET = 000~1111, TRICKLE_SET = 1	2.31*N	2.52*N	2.73*N	V
V <sub>TRICKLE_ext</sub>	Trickle charge threshold for external setting, over VBAT target	VBAT_SEL = 1, TRICKLE_SET = 0	65	70	75	%
		VBAT_SEL = 1, TRICKLE_SET = 1	55	60	65	%
V <sub>EOC</sub>	EOC voltage threshold, over VBAT target	VBAT_SEL = 0/1	97%	98%	99%	
V <sub>RECH</sub>	Recharge threshold voltage, over VBAT target	VBAT_SEL = 0/1	94.8%	95.8%	96.8%	
V <sub>VINREG</sub>	VINREG reference voltage	4.5V target VINREG_SET = 0x2C, VINREG_RATIO = 0	4.3	4.5	4.7	V
		15V target VINREG_SET = 0x95, VINREG_RATIO = 0	14.7	15	15.3	V
		4.48V target VINREG_SET = 0x6F, VINREG_RATIO = 1	4.4	4.5	4.6	V
		10V target VINREG_SET = 0xF9, VINREG_RATIO = 1	9.8	10	10.2	V
V <sub>BAT_OVP</sub>	VBAT OVP threshold, over VBAT target	VBAT_SEL = 0/1	103%	105.5%	108%	
V <sub>CLAMP</sub>			125			mV
<b>REFERENCE VOLTAGE IN DISCHARGING MODE</b>						
V <sub>FB</sub>	FB reference voltage for external setting	FB_SEL = 1, VBUSREF_E_REF target from 0.5V to 2.048V	-2%		2%	
V <sub>VBUS</sub>	VBUS reference voltage accuracy for internal setting	FB_SEL = 0 VBUS_RATIO = 1 (5x) VBUS = 3.6 ~10.24V	-2%		2%	
		FB_SEL = 0 VBUS_RATIO = 0 (12.5x) VBUS = 9 ~ 24V	-2%		2%	
V <sub>VBUS_OVP</sub>	VBUS OVP threshold, rising edge	VBUSREF_I_SET = 1V VBUSREF_E_SET = 1V	107.3%	110%	113%	
	Hysteresis	VBUSREF_I_SET = 1V VBUSREF_E_SET = 1V	3%			
<b>CURRENT LIMIT</b>						
I <sub>BUS_LIM</sub>	IBUS current limit accuracy	Charging mode, 6A target IBUS_RATIO = 01 (6x) IBUS_LIM = 0x7F	-10%		10%	
		Charging mode, 3A target IBUS_RATIO = 10 (3x) IBUS_LIM = 0x7F	-10%		10%	
		Discharging mode, 6A target IBUS_RATIO = 01 (6x) IBUS_LIM = 0x7F	-10%		10%	
		Discharging mode, 3A target IBUS_RATIO = 10 (3x)	-10%		10%	



		IBUS_LIM = 0x7F				
IBAT_LIM	IBAT current limit accuracy	Charging mode, 6A target IBAT_RATIO = 0 (6x) IBAT_LIM = 0xFF	-10%	10%		
		Charging mode, 12A target IBAT_RATIO = 1 (12x) IBAT_LIM = 0xFF	-10%	10%		
		Discharging mode, 6A target IBAT_RATIO = 0 (6x) IBAT_LIM = 0xFF	-15%	15%		
		Discharging mode, 12A target IBAT_RATIO = 1 (12x) IBAT_LIM = 0xFF	-15%	15%		
ITRICKLE	Trickle charge current, over IBAT_LIM setting			10%		
	Trickle charge current, over IBUS_LIM setting			22%		
IEOC	EOC current threshold, over IBUS_LIM / IBAT_LIM setting	EOC_SET = 0		4%		
		EOC_SET = 1		10%		
<b>ERROR AMPLIFIER</b>						
Gm <sub>EA</sub>	Error amplifier gm		0.12	0.15	0.18	mS
R <sub>OUT</sub>	Error amplifier output resistance <sup>(1)</sup>			20		MΩ
I <sub>SINK_COMP</sub>	COMP sink current	LOOP_SET = 0/1		25		μA
I <sub>SRC_COMP</sub>	COMP source current	LOOP_SET = 0		18		μA
		LOOP_SET = 1		32		μA
I <sub>BIAS_FB</sub>	FB pin input bias current	FB_SEL = 1 FB in regulation			50	nA
<b>SWITCHING</b>						
f <sub>SW</sub>	Switching frequency	FREQ_SET = 00 (150kHz)	140	155	170	kHz
		FREQ_SET = 01 (300kHz)	270	305	330	kHz
		FREQ_SET = 11 (450kHz)	400	450	500	kHz
<b>POWER PATH MANAGEMENT</b>						
R <sub>PU_PGATE</sub>	PGATE pin pull up resistor	EN_PGATE = 0		20		kΩ
R <sub>PD_PGATE</sub>	PGATE pin pull down resistor	EN_PGATE = 1		6		kΩ
V <sub>CLAMP</sub>	Clamp voltage from VBUS to PGATE pin	EN_PGATE = 1	6.9	7.35	7.7	V
R <sub>RD_GPO</sub>	GPO pin pull down resistor	GPO_CTRL = 1		6		kΩ
<b>DETECTION</b>						
V <sub>AC_DET</sub>	AC detection threshold		2.9	3.1	3.4	V
V <sub>SHORT</sub>	Short circuit detection threshold		0.95	1	1.05	V
<b>I2C AND LOGIC CONTROL</b>						
R <sub>PD</sub>	PSTOP pin internal pull down resistor		0.75	1	1.25	MΩ
V <sub>IL</sub>	PSTOP, SCL, SDA input low voltage				0.4	V
V <sub>IH</sub>	PSTOP, SCL, SDA input high voltage		1.2			V



$I_{SINK\_INT}$	INT pin sink current	$V_{INT} = 0.4V$	0.3	0.375	0.45	mA
$I_{SINK\_SCL/SDA}$	SCL/SDA pin sink current	$V_{SCL/SDA} = 0.4V$		100		mA
$t_{PULSE}$	Interrupt pulse width (logic low)		0.6	1	1.5	ms
<b>SOFTSTART</b>						
$t_{deglitch}$	Deglintch time for charging	PSTOP = L, OTG_SET = 0 VBUS = 5V, from PSTOP low to IC starting charging		220		ms
$t_{SS}$	Internal soft-start time	VBUS from 0V to 5V in discharging mode VBUS_Ratio = 1 (5x)		12		ms
<b>THERMAL SHUTDOWN</b>						
$T_{SD}$	Thermal shutdown temperature <sup>(1)</sup>			165		°C
	Thermal shutdown hysteresis <sup>(1)</sup>			15		°C

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## 8 Detailed Description

### 8.1 Charging Mode

Charging mode and discharging mode is selected by EN\_OTG bit.

When EN\_OTG bit is 0, the IC works in charging mode. The current flows from VBUS to VBAT to charge the battery cells.

When in charging mode, the IC charges the battery cells according to below typical charging profile. When battery voltage is lower than trickle charge threshold, the IC charges the cells with small charging current; when cell voltage is higher than the threshold, the IC enters into Constant Current charging phase, and charges the cells with constant current set by IBUS limit or IBAT limit. When the cell voltage reaches the termination voltage target, the IC enters into Constant Voltage charge phase, and charges the cells with gradually decreased current until the current is lower than termination current threshold. Once termination voltage and termination current conditions are satisfied, the IC enters into End of Charge phase. In this phase the IC can either terminate the charging or keep charging the cells.

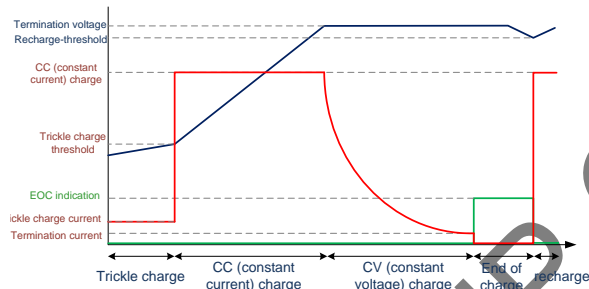


Figure 1 Typical Charging Profile

#### 8.1.1 Trickle Charge

The trickle charge voltage threshold can be set to 60% or 70% of 4.2V/cell by TRICKLE\_SET bit. When in trickle charge phase, the charging current is reduced to a small value for the good of battery cells. If ICHAR\_SEL bit is 0, the IBUS is reduced to 22% of the IBUS current limit set value; if ICHAR\_SEL bit is 1, the IBAT is reduced to 10% of IBAT current limit set value.

If trickle charging phase is not needed, the user can set DIS\_TRICKLE bit to 1 to disable it.

#### 8.1.2 CC Charge (Constant Current Charge)

When cell voltage is higher than the trickle threshold, the IC charges the battery cells with constant current set by IBUS limit or IBAT limit, which are set respectively through IBUS\_LIM\_SET and IBAT\_LIM\_SET registers. The current limit value can be changed dynamically, and is also related to the current sense resistor and ratio bits. Please see Register Map section for details.

In charging mode, the IC regulates the current which reaches its current limit value first. For example, if IBUS current limit

is set to 3A, IBAT limit is set to 10A, and when IBUS reaches 3A, IBAT is only 6A, which is much lower than IBAT limit 10A, then the IC limits the IBUS at 3A.

It is not allowed to set any of the current limits to 0A. Keep the minimum current limit above 0.3A.

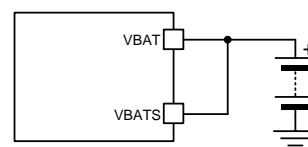
#### 8.1.3 CV Charge (Constant Voltage Charge)

The battery target voltage can be set internally, by CSEL bits and VCELL\_SET bits. The CSEL bits set the battery cell numbers connected in series, and VCELL\_SET bits set the battery voltage per cell. For example, if the battery cells are in xp2s connection (several cells are connected in parallel, and two cells in series) and the cell voltage is 4.3V, the user should set CSEL to 01 (2S), and set VCELL\_SET bits to 011 (4.3V).

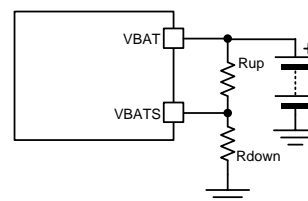
When the battery charging voltage is set internally, the user should connect VBATS pin to VBAT terminal to sense the battery voltage, and the VBAT\_SEL bit should be set to 0.

If VBAT\_SEL is set to 1, it means the battery voltage is set externally. Under this condition, the user should use resistor divider at VBATS pin to set the target voltage as below. VCELL\_SET and CSEL bits don't work. The reference voltage of VBATS is 1.2V.

$$VBAT = V_{BATS\_REF} \times \left(1 + \frac{R_{UP}}{R_{DOWN}}\right)$$



A. VBAT\_SEL = 0



B. VBAT\_SEL = 1

Figure 2 Battery voltage setting

When the battery cell voltage reaches 98% of the cell target voltage, the IC enters into CV charge phase. In this phase, the VBAT voltage is regulated at target value, and the charging current reduces gradually.

#### 8.1.4 EOC (End of Charge)

When both of below voltage condition and current condition for EOC detection are satisfied, the IC enters into EOC phase, and informs the MCU through EOC interrupt bit.

1. the cell voltage is higher than 98% of set value

2. the IBUS or IBAT current (decided by ICHAR\_SEL bit) is lower than 1/10 or 1/25 (decided by EOC\_SET bit) of its current limit value

In EOC phase, the IC can terminate the charging process or keep charging the battery cells, which can be set by DIS\_TERM bit. If IC keeps charging, it regulates the battery cell voltage at set value.

### 8.1.5 Recharge

If the IC terminates the charging process after EOC is detected, the battery voltage may drop slowly due to leakage or operation current from battery cells. Once the VBAT voltage drops below 95% of the set voltage, the EOC bit is cleared, and the IC enters into CC charge phase and recharges the battery.

### 8.1.6 Self-adaptive Charging Current (VINREG)

The IC features dynamic power management. The allowed minimum VBUS operation voltage is VINREG threshold, which can be set by VINREG\_SET register and VINREG\_RATIO bit dynamically. During charging, if the IBUS charging current is higher than adapter's current capability, the adapter will be overloaded and the VBUS voltage is pulled low. Once the IC detects the VBUS voltage drops at VINREG threshold, it reduces the charging current automatically and regulates the VBUS voltage at VINREG threshold.

### 8.1.7 Battery Impedance Compensation

The IC provides the function of battery impedance compensation. User can set the impedance through IRCOMP bits, then the VBAT target voltage in CV phase is compensated as

$$VBAT\_cmp = VBAT\_set + \min(IBAT\_IRCOMP, VCLAMP)$$

Where,

VBAT\_cmp is the compensated battery voltage target; VBAT\_set is the originally set battery termination target; IBAT is the charging current at battery side; IRCOMP is the resistance compensation value set by IRCOMP bits; VCLAMP is the allowed maximum compensation value, fixed at 125mV.

User should carefully evaluate the real battery impedance. If the value set by IRCOMP bits is higher than the real value, it will cause over charge.

## 8.2 Discharging Mode

When EN\_OTG bit is set to 1, the IC enters into discharging mode. In discharging mode, the battery (VBAT) is discharged and the current flows from VBAT to VBUS.

If FB\_SEL is set to 0, the VBUS output voltage is set internally, through VBUSREF\_I\_SET and VBUSREF\_I\_SET2 registers and the VBUS\_RATIO bit. The VBUS can be changed dynamically, and the recommended VBUS voltage range is from 3.5V to 25.6V. When VBUS is lower than 10.24V, it is suggested to set the VBUS\_RATIO to 5x, and so

the minimum changing step is 10mV/step; when VBUS is higher than 10.24V, VBUS\_RATIO should be set to 12.5x, and the minimum changing step is 25mV/step.

If FB\_SEL is set to 1, the VBUS voltage target is set externally, that is, by the resistor divider connected at FB pin, and can be calculated as below.

$$VBUS = VBUSREF\_E \times \left(1 + \frac{RUP}{RDOWM}\right)$$

Even if VBUS is set externally, the user can still change the VBUS voltage dynamically by changing the reference voltage VBUSREF\_E through VBUSREF\_E\_SET and VBUSREF\_E\_SET2 registers. The default VBUSREF\_E is 1V, and recommended VBUSREF\_E voltage range is from 0.7V to 2.048V.

Please see Register Map section for details.

The IBUS current limit and IBAT current limit are still functional in discharging mode and can be changed dynamically.

It is not allowed to set any of the current limits to 0A. Keep the minimum current limit above 0.3A.

### 8.2.1 Soft Start

The IC integrates soft-start control to generate VBUS voltage in discharging mode. When VBUS is lower than V<sub>SHORT</sub> (typ. 1V), both IBUS and IBAT current limits are fold back to 1/10 of the setting value. Meanwhile, the IC ramps up the internal reference voltage gradually (~10ms) to avoid inrush current.

If there is a load at VBUS at the beginning of the startup, the IC may fail to boost the VBUS voltage beyond V<sub>SHORT</sub> due to the 1/10 current limits for both IBUS and IBAT. If startup with loading is required, user shall set the DIS\_ShortFoldBack bit to 1 to disable the current limit fold back function. After startup, the user can set DIS\_ShortFoldBack bit back to 0, so to enable this function for short circuit protection. See VBUS Short Protection section for details.

### 8.2.2 Slew Rate Setting

When the VBUS voltage is changed dynamically through reference voltage (VBUSREF\_I\_SET and VBUSREF\_I\_SET2 registers or VBUSREF\_E\_SET and VBUSREF\_E\_SET2 registers), the reference voltage change rate can be controlled through SLEW\_SET bits. For example, the VBUS is set in internal way with 5x ratio, and the VBUSREF\_I = 1V at first (VBUS = 5V), then the user sets the VBUSREF\_I voltage to 1.6V to get 8V output. If the slew rate is 2mV/μs, the VBUS voltage will increase to 8V in 600mV / 2mV/μs = 300μs.

### 8.2.3 PFM Operation

The IC supports PFM operation in discharging mode by setting EN\_PFM bit to 1. In PWM mode, the IC always works with constant switching frequency for the whole load range. This helps achieve the best output voltage performance, but the efficiency is low at light load condition because of the high switching loss.

In PFM mode, the IC still works with constant switching frequency under heavy load condition, but under light load condition, the IC automatically changes to pulse frequency modulation operation to reduce the switching loss. The efficiency can be improved under light load condition while output voltage ripple will be a little larger compared with PWM operation. Below figure shows the output voltage behavior of PFM mode.

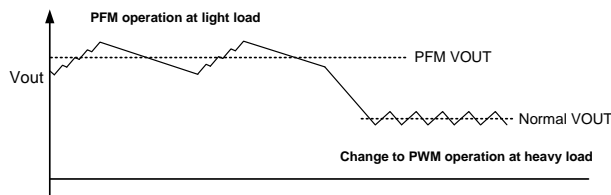


Figure 3 PFM mode illustration

### 8.3 ADC for Voltage and Current Monitor

The IC integrates a 10-bit ADC, so the IC can monitor the VBUS/VBAT voltages and IBUS/IBAT current no matter in charging mode or discharging mode. Besides these, the IC provides an analog input: ADIN pin for 10-bit ADC sampling. The maximum voltage the ADC can sample at ADIN pin is 2.048V, and the sampling resolution is 2mV/step. The ADC function is enabled after AD\_START bit is set to 1. When ADC is enabled in standby mode, the IC will 0.5mA~1mA operation current. Please see Register Map section for details.

### 8.4 Power Path Management

The IC offers power path management function at PGATE and GPO pins. The PGATE pin can be used to drive PMOS connected at VBUS. The PGATE pin is connected to a 6 kΩ pull down resistor internally when EN\_PGATE is set to 1, and the maximum voltage between VBUS and PGATE is clamped at 7.35V; when EN\_PGATE is set to 0, PGATE pin is connected to VBUS rail through a 20 kΩ pull up resistor internally.

The GPO pin is an open drain output, so external pull up resistor is needed. When GPO\_CTRL bit is set to 0, GPO outputs high impedance; when GPO\_CTRL is set to 1, GPO is pulled down internally and the pull down resistance is 6 kΩ.

User can use PGATE pin and GPO pin to control the isolation MOSFETs between adapter input and USB output as shown in Typical Application Circuit. However, the MCU or system controller controls the bits through I2C interface, which takes time for communication, so the PMOS may not be turned on/off very quickly. In the application where the isolation PMOS needs to be controlled very fast, it is suggested to use the I/O pins of MCU to control the PMOS on/off directly.

### 8.5 Phone Insert Detection

If connecting INDET pin to USB-A port as shown in Typical Application Circuit, the IC can detect the phone detection.

Once the IC detects a phone is inserted, it sets the INDET interrupt bit to inform MCU. The INDET bit is cleared after it is read by MCU.

### 8.6 Adapter Attachment / Detachment Detection

If connecting ACIN pin to Micro-USB port as shown in Typical Application Circuit, the IC can detect the attachment / detachment of the adapter.

Once the ACIN pin voltage is higher than 3V, which means the adapter is inserted, the IC sets the AC\_OK interrupt bit to inform MCU about the attachment. If the ACIN pin voltage is lower than 3V, which means the adapter is removed, the IC clears AC\_OK bit to inform the MCU about the detachment.

### 8.7 Switching and Frequency Dithering

The IC switches in fixed frequency which can be adjusted through FREQ\_SET bits. The switching dead time can also be set through DT\_SET pins. Please see Register Map section for details.

The IC also offers frequency dithering function. This function can be enabled by setting EN\_DITHER bit to 1. When the function is enabled, the switching frequency is not fixed, but varies within +/- 5% range. For example, if the switching frequency is set to 300kHz (FREQ\_SET = 01), the frequency will change from 285kHz to 315kHz gradually and then back to 285kHz back and forth. The time it varies from the lowest to the highest frequency or from highest to lowest frequency can be controlled by a capacitor connected at PGATE/DITHER pin as below equation shows. For example, if 100nF capacitor is connected, the time is 1.2 ms.

$$T_{\text{dither}} = \frac{120 \text{ mV} \times C}{10 \text{ } \mu\text{A}}$$

When EN\_DITHER is set to 1, the PGATE driver function is disabled, and the PGATE/DITHER pin only operates for dithering function.

### 8.8 VCC Regulator and Driver Supply

The IC integrates a regulator and generates a 5V voltage at VCC pin with typically 25 mA driving capability. The regulator is powered by the higher voltage of VBUS or VBAT.

When in Standby mode (PSTOP is pulled high), the VCC regulator is shutdown, so VCC voltage is reduced and has very limited current capability. It is not suggested to use VCC in Standby mode.

The internal driving circuit is powered from VDRV pin, and user should provide a supply at VDRV pin to power the circuit. The user can connect VCC to VDRV directly, or connect an external power supply to VDRV. Besides the two ways, the IC offers a charge pump driver at CP pin, which can pump the VCC voltage to power VDRV pin. With charge pump circuit, the IC can regulate the VDRV voltage. at 6V.

**Charge pump is not recommended for VDRV. Consult local FAE if charge pump is used.**



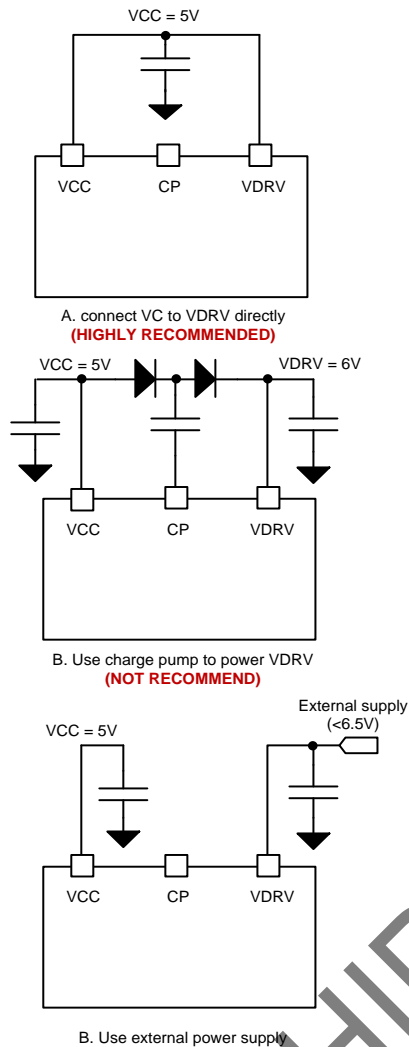


Figure 4 Supply for VDRV

## 8.9 Standby Mode

When PSTOP signal is high, the IC enters into Standby mode. In this mode, the IC stops switching to save the quiescent current. The other functions are still valid, and the MCU can still control the IC through I2C. However, if ADC function is enabled in Standby mode, the quiescent current will be increased to 0.5mA~1mA.

## 8.10 Protection

### 8.10.1 VBUS Over Voltage Protection

User can enabled / disable VBUS over voltage protection in discharging mode by DIS\_OVP bit. When OVP is enabled, the IC stops switching when VBUS is higher than the target voltage by 10%.

### 8.10.2 VBAT Over Voltage Protection

The IC implements VBAT over voltage protection in both

charging mode and discharging mode. Once the VBAT voltage is higher than target voltage by 10%, the IC stops switching.

### 8.10.3 VBUS Short Protection

In discharging mode, if the VBUS voltage is detected lower than  $V_{SHORT}$  (typ. 1V), the IC sets the VBUS\_SHORT interrupt bit to inform the MCU. In the same time, the IBUS current limiting value and IBAT current limiting value were reduced to 22% and 10% of setting value respectively to protect the IC. If DIS\_ShortFoldBack bit is set to 1, the IBUS and IBAT current limit will not be reduced.

### 8.10.4 Over Temperature Protection

When the IC detects the junction temperature is higher than  $165^{\circ}\text{C}$ , the IC stops switching to protect the chip, and sets the OTP interrupt bit to inform the MCU. It resumes switching once the temperature drops below  $15^{\circ}\text{C}$ .

## 8.11 I2C and Interrupt

### 8.11.1 I2C Interface

The IC features I2C interface, so the MCU or controller can control the IC flexibly. The 7-bit I2C address of the chip is 0x74 (8-bit address is 0xE8 for write command, 0xE9 for read command). The SDA and SCL pins are open drain and must be connected to the positive supply voltage via a current source or pull-up resistor. When the bus is free, both lines are HIGH. The I2C interface supports both standard mode (up to 100kbits) and fast mode (up to 400k bits with 5 k $\Omega$  pull up resistor at SCL pin and SDA pin respectively).

#### 8.11.1.1 Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. One clock pulse is generated for each data bit transferred.

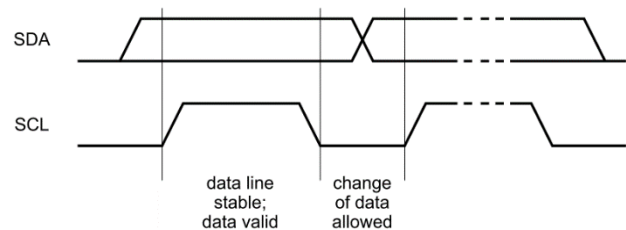


Figure 5 Bit transfer on the I2C bus

#### 8.11.1.2 START and STOP Conditions

All transactions begin with a START (S) and are terminated by a STOP (P). A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition.

START and STOP conditions are always generated by the master. The bus is considered to be busy after the START

condition. The bus is considered to be free again a certain time after the STOP condition.

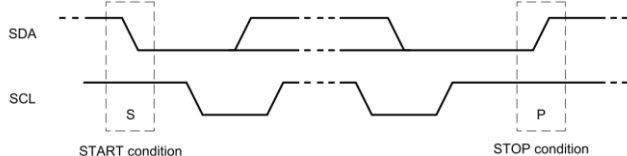


Figure 6 START and STOP conditions

### 8.11.1.3 Byte Format

Every byte put on the SDA line must be eight bits long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte must be followed by an Acknowledge bit. Data is transferred with the Most Significant Bit (MSB) first. If a slave cannot receive or transmit another complete byte of data until it has performed some other function, for example servicing an internal interrupt, it can hold the clock line SCL LOW to force the master into a wait state. Data transfer then continues when the slave is ready for another byte of data and releases clock line SCL.

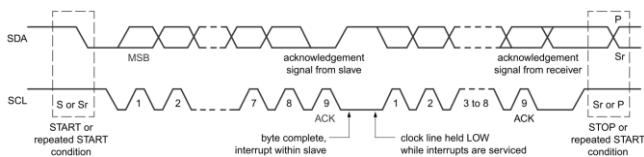


Figure 7 Data transfer on the I2C bus

### 8.11.1.4 Acknowledge (ACK) and Not Acknowledge (NACK)

The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. During data is transferred, the master can either be the transmitter or the receiver. No matter what it is, the master generates all clock pulses, including the acknowledge ninth clock pulse.

The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line LOW and it remains stable LOW during the HIGH period of this clock pulse.

When SDA remains HIGH during this ninth clock pulse, this is defined as the Not Acknowledge signal. The master can then generate either a STOP condition to abort the transfer, or a repeated START condition to start a new transfer.

### 8.11.1.5 The slave address and R/W bit

Data transfers follow the format shown in below. After the START condition (S), a slave address is sent. This address is seven bits long followed by an eighth bit which is a data direction bit (R/W) — a 'zero' indicates a transmission (WRITE), a 'one' indicates a request for data (READ). A data transfer is always terminated by a STOP condition (P) generated by the master. However, if a master still wishes to communicate on the bus, it can generate a repeated START condition (Sr) and address another slave without first

generating a STOP condition.

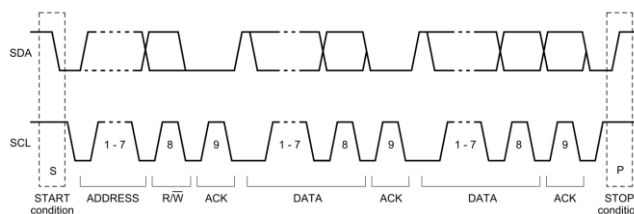


Figure 8 A complete data transfer



Figure 9 The first byte after the START procedure

### 8.11.1.6 Single Read and Write

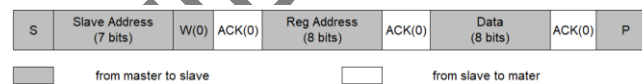


Figure 10 Single Write

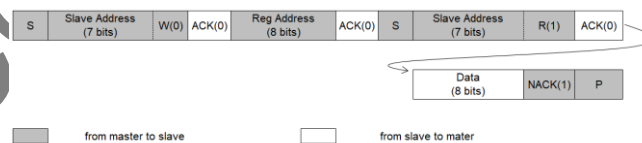


Figure 11 Single Read

If the register address is not defined, the charger IC send back NACK and go back to the idle state.

### 8.11.1.7 Multi-Read and Multi-Write

The IC supports multi-read and multi-write for continuous registers.

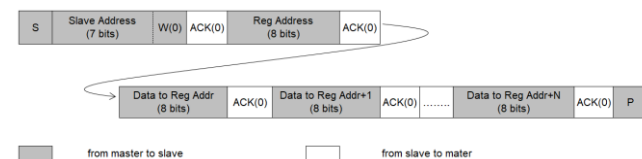


Figure 12 Multi-Write

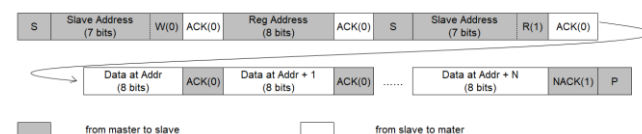


Figure 13 Multi-Read



### 8.11.2 Interrupt

When AC\_OK/VBUS\_SHORT/OTP/EOC is set to 1, or clear to 0, the IC sends an interrupt pulse as below at INT pin to inform MCU. But when INDET only is set to 1, the IC sends an interrupt pulse. It is summarized as below:

Status Signal	Interrupt Triggering Mechanism
Reserved	
AC_OK	Rising edge or falling edge triggers 1ms_pulse INT
INDET2	Only rising edge triggers 1ms_pulse INT
INDET1	Only rising edge triggers 1ms_pulse INT
VBUS_SHORT	Logic high triggers continuous INT
OTP	Rising edge or falling edge triggers 1ms_pulse INT
EOC	Rising edge or falling edge triggers 1ms_pulse INT
Reserved	

The interrupt pulse at INT pin is as follow:

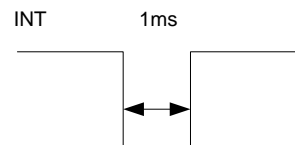


Figure 14 Interrupt pulse at INT pin

The INDET bit is read and clear type. Except INDET, all other bits in Status register represent the real time status. User can mask the interrupt output of any bit by setting its corresponding bit in Mask register. When the mask bit is set, the corresponding status bit is still set, but the IC doesn't send the interrupt at INT pin.

## 9 Application Information

### 9.1 Capacitor Selection

The switching frequency of the IC is in the range of 150kHz ~ 450kHz. Since MLCC ceramic capacitor has good high frequency filtering with low ESR, above 60μF X5R or X7R capacitors with higher voltage rating than operating voltage with margin is recommended. For example, if the highest operating Vin/Vout voltage is 12V, select at least 16V capacitor and to secure enough margin, 25V voltage rating capacitor is recommended.

The high capacitance polymer capacitor or tantalum capacitor can be used for input and output but capacitor voltage rating must be higher than the highest operating voltage with enough margin. The high frequency characteristics of these capacitors are not as good as ceramic capacitor, so at least 10μF ceramic capacitor should be placed in parallel to reduce high frequency ripple.

### 9.2 Inductor Selection

2.2 μH to 4.7 μH inductor is recommended for loop stability. The peak inductor current in discharging mode can be calculated as

$$I_{L\_peak} = I_{BAT} + \frac{V_{BAT} \cdot (V_{BUS} - V_{BAT} \cdot \eta)}{2 \cdot f_{sw} \cdot L \cdot V_{BUS}} \quad (V_{BUS} \geq V_{BAT})$$

$$I_{L\_peak} = I_{BUS} + \frac{V_{BUS} \cdot (V_{BAT} - V_{BUS})}{2 \cdot f_{sw} \cdot L \cdot V_{BAT} \cdot \eta} \quad (V_{BUS} < V_{BAT})$$

where  $I_{BAT}$  is the battery current at  $V_{BAT}$  side, and can be calculated as

$$I_{BAT} = \frac{V_{BUS} \cdot I_{BUS}}{\eta \cdot V_{BAT}}$$

$\eta$  is the power conversion efficiency. User can use 90% for calculation.

$f_{sw}$  is the switching frequency

$L$  is the inductor value

The peak inductor current in charging mode can be calculated as

$$I_{L\_peak} = I_{BAT} + \frac{V_{BAT} \cdot (V_{BUS} - V_{BAT})}{2 \cdot f_{sw} \cdot L \cdot V_{BUS} \cdot \eta} \quad (V_{BUS} > V_{BAT})$$

$$I_{L\_peak} = I_{BUS} + \frac{V_{BUS} \cdot (V_{BAT} - V_{BUS} \cdot \eta)}{2 \cdot f_{sw} \cdot L \cdot V_{BAT}} \quad (V_{BUS} \leq V_{BAT})$$

where  $I_{BAT}$  is the battery charging current at  $V_{BAT}$  side, and can be calculated as

$$I_{BAT} = \frac{V_{BUS} \cdot I_{BUS} \cdot \eta}{V_{BAT}}$$

$\eta$  is the power conversion efficiency. User can use 90% for calculation.

$f_{sw}$  is the switching frequency

$L$  is the inductor value

When selecting inductor, the inductor saturation current must be higher than the peak inductor current with enough margin (20% margin is recommended). The rating current of the inductor must be higher than the battery current.

The inductor DC resistance value (DCR) affects the conduction loss of switching regulator, so low DCR inductor is recommended especially for high power application. The conductor loss of inductor can be calculated roughly as

$$P_{L\_DC} = I_{L}^2 \cdot DCR$$

$I_L$  is the average value of inductor current, and it equals to  $I_{BAT}$  or  $I_{BUS}$ .

Besides DC power loss, there are also inductor AC winding loss and inductor core loss, which are related to inductor peak current. Normally, higher peak current causes higher AC loss and core loss. The user can consult with the inductor vendor to select the inductors which have small ESR at high frequency and small core loss.

### 9.3 Current Sense Resistor

The  $RSNS1$  and  $RSNS2$  are current sense resistors. 10 mΩ should be used for  $RSNS1$  to sense  $I_{BUS}$  current, 5 mΩ or 10 mΩ used for  $RSNS2$  to sense  $I_{BAT}$  current (10 mΩ supports higher battery current limit accuracy, and 5 mΩ supports higher efficiency). Resistor of 1% or higher accuracy and low temperature coefficient is recommended.

Note: If the user wants to use other resistor values, please contact factory for support.

The resistor power rating and temperature coefficient should be considered. The power dissipation is roughly calculated as  $P=I^2R$ , and  $I$  is the highest current flowing through the resistor. The resistor power rating should be higher than the calculated value.

Normally the resistor value is varied if the temperature increased and the variation is decided by temperature coefficient. If high accuracy of current limit is required, select lower temperature coefficient resistor as much as possible.

### 9.4 MOSFET Selection

The IC integrates two power MOSFETs, and the user should add two external power MOSFETs at  $V_{BAT}$  side.

The  $V_{DS}$  of MOSFET should be higher than the highest operating voltage with enough margin (recommend more than 10V higher). For example, if the highest operating voltage is 20V, at least 30V rated  $V_{DS}$  MOSFET should be selected; If the highest operating voltage is 24V, 40V  $V_{DS}$  voltage rating should be selected.

The  $V_{GS}$  voltage rating of MOSFET should be selected higher than 8V. Considering PCB parasitic parameters during operation, MOSFET  $V_{GS}$  voltage might be higher than  $V_{DRV}$  voltage due to transient overshoot, so 10V  $V_{GS}$  is recommended to secure sufficient margin.

The MOSFET current  $I_D$  should be higher than the highest

battery current with enough margin.

To ensure the sufficient current capability in relatively high temperature circumstance, the current rate at  $T_A=70^{\circ}\text{C}$  or  $T_C = 100^{\circ}\text{C}$  should be considered. In addition, the power dissipation value  $P_D$  should also be considered and higher  $P_D$  is better in applications. Make sure that MOSFET power consumption must not exceed  $P_D$  value.

The MOSFET  $R_{DS(ON)}$  and input capacitor  $C_{ISS}$  impact power efficiency directly. Typically, lower  $R_{DS(ON)}$  MOSFET has higher  $C_{ISS}$ . The  $R_{DS(ON)}$  is related to conduction loss. Higher  $R_{DS(ON)}$  results in higher conduction loss, thus lower efficiency and higher thermal dissipation; the  $C_{ISS}$  is related to MOSFET switch on/off time, and longer on/off time results in higher switching loss and lower efficiency. The proper MOSFET should be selected based on tradeoff between the  $R_{DS(ON)}$  and  $C_{ISS}$ .

If high  $C_{ISS}$  MOSFET is selected, the switching on and off time become longer, then the dead time should be adjusted to avoid simultaneous turn on for both high side and low side MOSFETs.

### 9.5 Driver Resistor and SW Snubber Circuit

To adjust MOSFET switching time and switching overshoot for EMI debugging, it is recommended to add series resistor (0603 size) for gate driving signal (HD1 to HG, LD1 to LG, LD2 to MOS gate, and HD2 to MOS gate), and RC snubber (0603 size) circuit at SWx, as shown below.

The driver resistor should be placed near MOS. At first, use 0Ω resistors; if switching overshoot is big, increase the resistor value to slow down the switching speed. It is suggested to keep the resistor value < 10 Ω. While the switching speed gets slower, the default dead time may not be enough to avoid overshoot of the power MOSFETs. So if higher than 10Ω is needed, user should increase the dead time if necessary.

The RC snubber circuit at SWx node is also helpful in absorbing the high frequency spike at SWx node, so to improve EMC performance. User can leave RC components as NC at the beginning, and adjust the value to improve the EMC performance if necessary. Normally user can try 2.2Ω and 1nF for the snubber. If EMC should be improved further, reduce the resistor value (like 1 Ω or even lower) and increase the capacitor value (like 2.2nF or even higher).

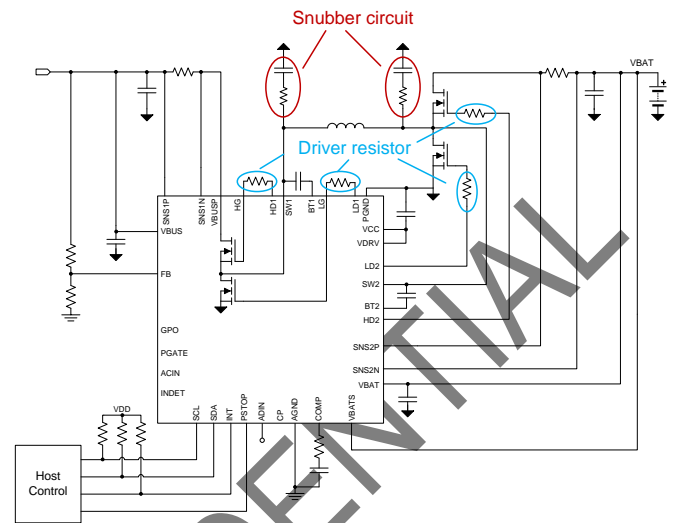


Figure 15 Driver resistor and snubber circuit

### 9.6 Layout Guide

1. The capacitors connected at VBUS/VBAT/VCC/VDRV pins should be placed near the IC, and their ground connection to the ground pins should be as short as possible.

#### a. component(s) on schematic:

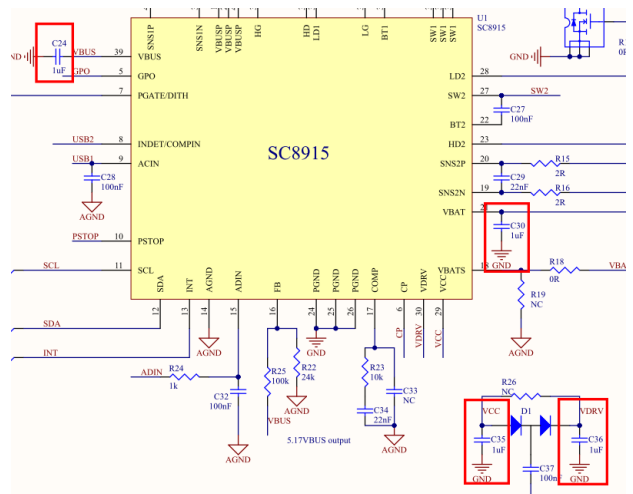


Figure 16 Schematic

- Layout example:** put the four capacitors near IC but on the bottom layer. Connect the capacitors to each pin through vias, and connect the capacitors to ground pins by the ground pour.

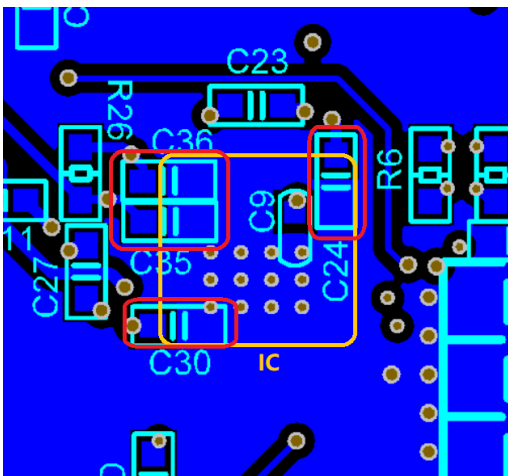


Figure 17 Bottom layer (flip view)

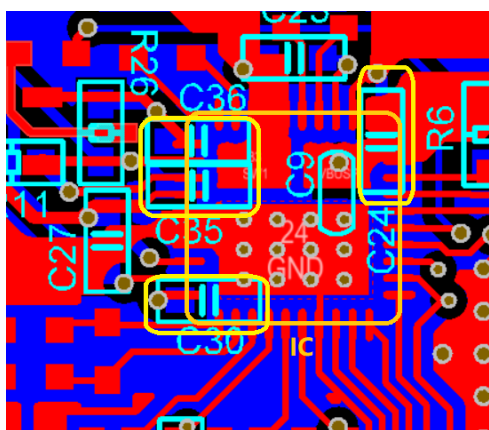


Figure 18 Top layer (flip view)

2. Between IBUS current sense resistor and VBUSP pins, add a 100nF 0402 capacitor to PGND. It is helpful to suppress high frequency noise. Put it very close to VBUSP pins and PGND pins.

**a. component(s) on schematic**

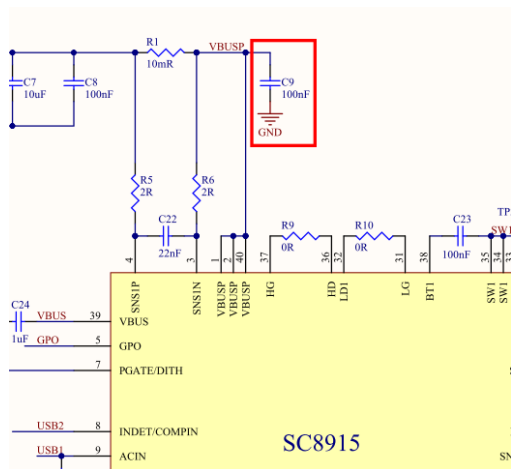


Figure 19 Schematic

- b. **Layout example:** the capacitor is put on the bottom of the IC, just from the VBUSP pad to PGND pad.

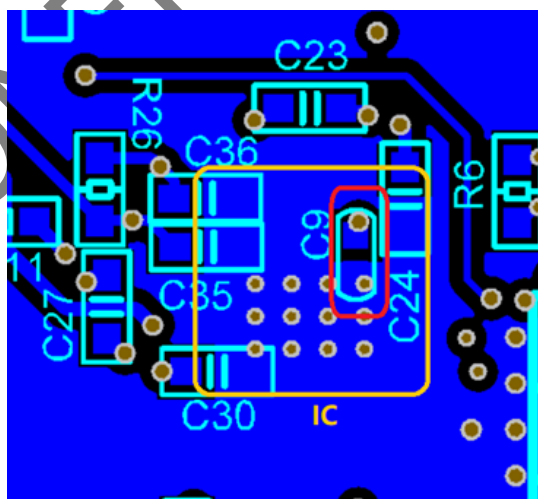


Figure 20 Bottom layer (flip view)

3. Put IBUS current sense resistor and bulk capacitor at VBUS side should be placed very close to VBUSP pins and PGND pins.

**a. component(s) on schematic**

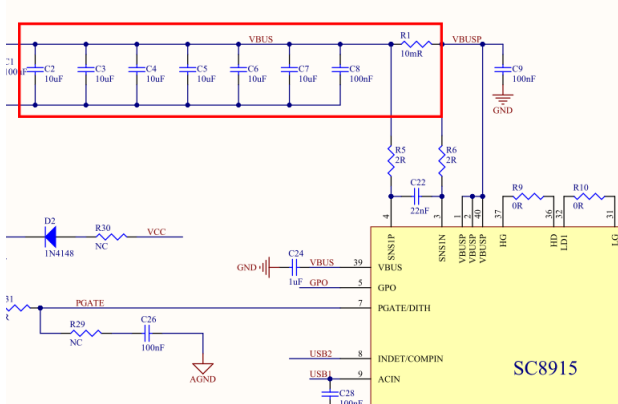


Figure 21 Schematic

- b. **Layout example:** put the current sense resistor just near the IC on the top layer, and connect to the bulk capacitors through wide copper on the top layer. The bulk capacitors are connected to PGND pins through vias and ground pour on the bottom layer. Keep the ground pour as wide as possible.

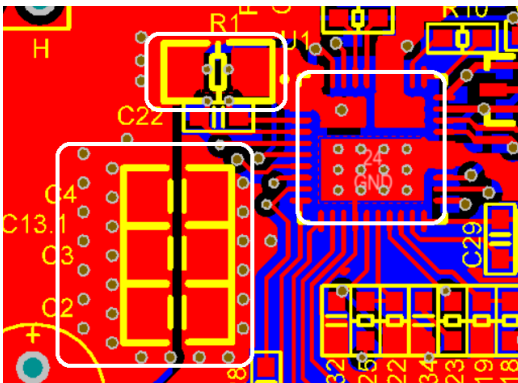


Figure 22 Top layer view

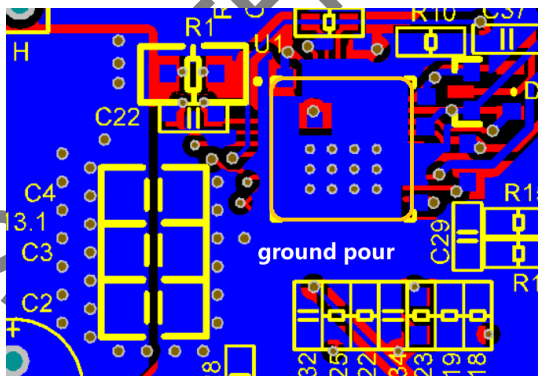


Figure 23 Bottom layer view

capacitor at VBAT side as close as possible. And the low side MOSFET and bulk capacitors should be very close to PGND pins. Between current sense resistor and high side MOS, add a 100nF 0402 capacitor to PGND. It is helpful to suppress high frequency noise. Put it very close to MOS and PGND pins.

a. **component(s) on schematic**

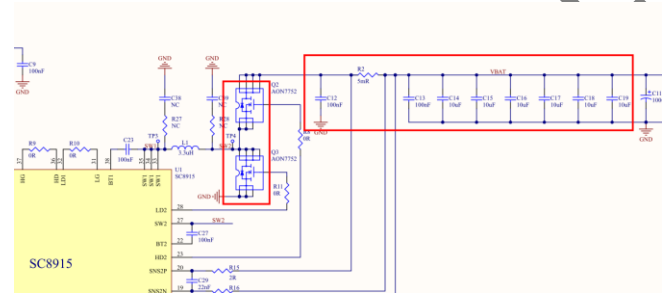


Figure 24 Schematic

- b. **Layout example:** put all these components on the top layer as a group, and the VBAT and PGND power paths should be as wide as possible. The low side MOS, 100nF capacitor and the bulk capacitors connected to PGND pins through ground pour on both top layer and bottom layer.

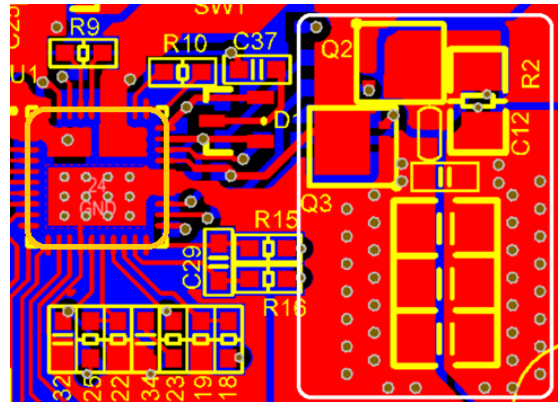


Figure 25 Top layer view

4. Put IBAT current sense resistor, MOSFETs and bulk

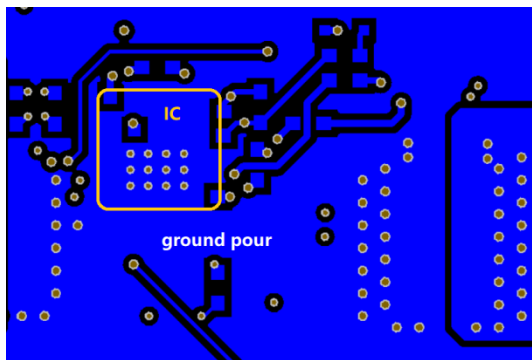


Figure 26 Bottom layer view

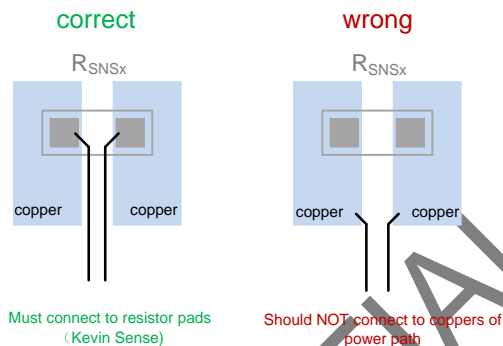


Figure 28 Current sense

- The driver signals (LD2 / HD2 / SW2) as shown below should be routed with wide traces ( $\geq 15$  mil). The driver resistors should be placed near MOS. The HD2 and SW2 should be routed in parallel, close to each other; the LD2 should be routed in parallel with PGND traces ( $\geq 15$  mil) or close to PGND pour. There should be wide space filled with PGND between LD2 and HD2 and also wide space from LD2 to SW2 to avoid interference.

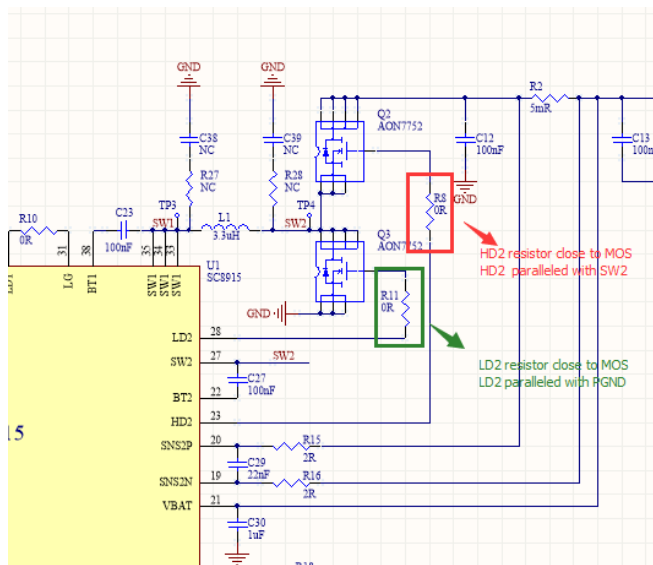


Figure 27 Schematic

- The current sense traces should be connected to the current sense resistor's pads in Kelvin sense way as below, and routed in parallel (differential routing), and add filter for each current sense near the IC.

**a. component(s) on schematic**

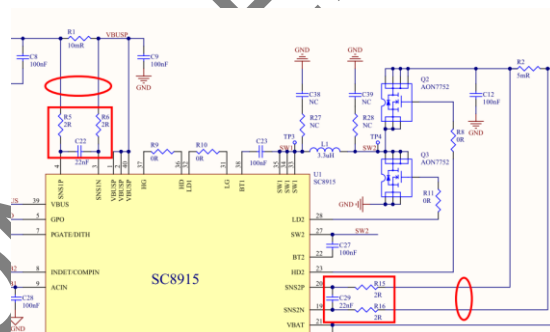


Figure 29 Schematic

- Layout example:** since the R1 should be put near the IC, so the filter components and traces for sense are also placed near the IC. The space for routing is limited, so the resistors of the filter are put on the bottom layer. The current sense resistor R2 should be placed near the power MOSFETs, so it might be far from the IC. The sense filter should be placed near the IC. The traces can be routed on other layer (3<sup>rd</sup> layer in this example), but should route the traces in parallel (differential way), far away from switching signals and isolated them with PGND pour.

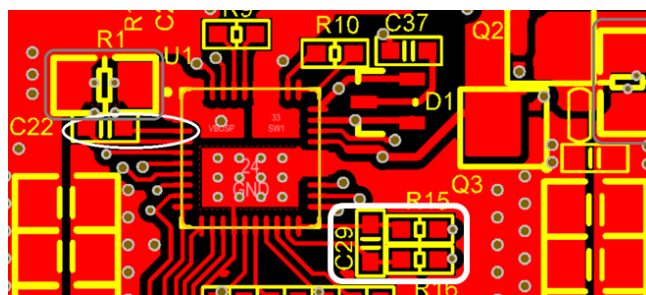


Figure 30 Top layer view





## 10 Register Map

7-bit address: 0x74; 8-bit address: 0xE8 for write command; 0xE9 for read command

Addr	Register	Type	Default value @POR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
00H	VBAT_SET	R/W	0000 0001	IRCOMP		VBAT_SEL	CSEL		VCELL_SET			
01H	VBUSREF_I_SET	R/W	0011 0001	VBUSREF_I_SET								
02H	VBUSREF_I_SET2	R/W	11xx xxxx	VBUSREF_I_SET_2		Reserved						
03H	VBUSREF_E_SET	R/W	0111 1100	VBUSREF_E_SET								
04H	VBUSREF_E_SET2	R/W	11xx xxxx	VBUSREF_E_SET_2		Reserved						
05H	IBUS_LIM_SET	R/W	1111 1111	IBUS_LIM setting								
06H	IBAT_LIM_SET	R/W	1111 1111	IBAT_LIM setting								
07H	VINREG_SET	R/W	0010 1100	VINREG voltage setting								
08H	RATIO	R/W	0011 1000	Reserved			IBAT_RATIO	IBUS_RATIO		VBAT_MON_RATIO	VBUS_RATIO	
09H	CTRL0_SET	R/W	0000 0100	EN_OTG	Reserved	Reserved	VINREG_RATIO	FREQ_SET		DT_SET		
0AH	CTRL1_SET	R/W	0000 0001	ICHAR_SEL	DIS_TRICKLE	DIS_TERM	FB_SEL	TRICKLE_SET	DIS_OVP	Reserved	Reserved	
0BH	CTRL2_SET	R/W	0000 0001	Reserved				FACTORY	EN_DITHER	SLEW_SET		
0CH	CTRL3_SET	R/W	0000 0010	EN_PGATE	GPO_CTRL	AD_START	ILIM_BW_SEL	LOOP_SET	DIS_ShortFoldBack	EOC_SET	EN_PFM	
0DH	VBUS_FB_VALUE	R	0000 0000	VBUS_FB_value								
0EH	VBUS_FB_VALUE2	R	0000 0000	VBUS_FB_value2		Reserved						
0FH	VBAT_FB_VALUE	R	0000 0000	VBAT_FB_value								
10H	VBAT_FB_VALUE2	R	0000 0000	VBAT_FB_value2		Reserved						
11H	IBUS_VALUE	R	0000 0000	IBUS_value								
12H	IBUS_VALUE2	R	0000 0000	IBUS_value2		Reserved						
13H	IBAT_VALUE	R	0000 0000	IBAT_value								
14H	IBAT_VALUE2	R	0000 0000	IBAT_value2		Reserved						
15H	ADIN_VALUE	R	0000 0000	ADIN_value								
16H	ADIN_VALUE_2	R	0000 0000	ADIN_value2		Reserved						
17H	STATUS	R	0000 0000	Reserved	AC_OK	INDET	Reserved	VBUS_SHORT	OTP	EOC	Reserved	
18H	Reserved	R	0000 0000	Reserved								
19H	MASK	R/W	1000 0000	Reserved	AC_OK_Mask	INDET_Mask	Reserved	VBUS_SHORT_Mask	OTP_Mask	EOC_Mask	Reserved	
1AH	Reserved	R/W	0000 0000	Reserved								
1BH	Reserved	R/W	xxx0 0000	Reserved								



Table 1 0x00H VBAT\_SET Register

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7-6	R/W	IRCOMP	00	Battery IR compensation setting: 00: 0 mΩ (default) 01: 20 mΩ 10: 40 mΩ 11: 80 mΩ	Set this bit during PSTOP pin is high
5	R/W	VBAT_SEL	0	VBAT voltage setting selection: 0: internal setting (default) 1: external setting	Set this bit during PSTOP pin is high
4-3	R/W	CSEL	00	Battery cell selection, only valid for internal VBAT voltage setting: 00: 1S battery (default) 01: 2S battery 10: 3S battery 11: 4S battery	Set this bit during PSTOP pin is high
2-0	R/W	VCELL_SET	001	Battery voltage setting per cell, only valid for internal VBAT voltage setting: 000: 4.1V 001: 4.2V (default) 010: 4.25V 011: 4.3V 100: 4.35V 101: 4.4V 110: 4.45V 111: 4.5V	Set this bit during PSTOP pin is high

Table 2 0x01H VBUSREF\_I\_SET Register

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7-0	R/W	VBUSREF_I_SET	0011 0001	Reference voltage programming for internal VBUS voltage setting. When FB_SEL = 0 (internal VBUS setting), set the highest 8-bit of the reference voltage for VBUS (total 10-bit programming). The internal reference voltage is calculated as $VBUSREF\_I = (4 \times VBUSREF\_I\_SET + VBUSREF\_I\_SET2 + 1) \times 2 \text{ mV}$ The VBUS output voltage is calculated as $VBUS = VBUSREF\_I \times VBUS\_RATIO$ VBUSREF_I_SET range: 0 ~ 255 0000 0000: 0 0000 0001: 1 0000 0010: 2 ....	

			0011 0001: 49 (default) .... 1111 1111: 255 The default reference voltage is $(4 \times 49 + 3 + 1) \times 2 \text{ mV} = 400 \text{ mV}$ ; the default VBUS output voltage with $\text{FB\_SEL} = 0$ is $400\text{mV} \times 12.5 = 5\text{V}$	
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Table 3 0x02H VBUSREF\_I\_SET\_2 Register

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7-6	R/W	VBUSREF_I_SET2	11	Reference voltage programming for internal VBUS voltage setting. When $\text{FB\_SEL} = 0$ (internal VBUS setting), set the lowest 2-bit of the reference voltage for VBUS (total 10-bit programming). The internal reference voltage is calculated as $\text{VBUSREF\_I} = (4 \times \text{VBUSREF\_I\_SET} + \text{VBUSREF\_I\_SET2} + 1) \times 2 \text{ mV}$ The VBUS output voltage is calculated as $\text{VBUS} = \text{VBUSREF\_I} \times \text{VBUS\_RATIO}$ VBUSREF_I_SET2 range: 0 ~ 3 00: 0 01: 1 10: 2 11: 3 (default)	
5-0		Reserved	xx xxxx		

Table 4 0x03H VBUSREF\_E\_SET Register

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7-0	R/W	VBUSREF_E_SET	0111 1100	Reference voltage programming for external VBUS voltage setting. When $\text{FB\_SEL} = 1$ (external VBUS setting), set the highest 8-bit of the reference voltage for VBUS (total 10-bit programming). The external reference voltage is calculated as $\text{VBUSREF\_E} = (4 \times \text{VBUSREF\_E\_SET} + \text{VBUSREF\_E\_SET2} + 1) \times 2 \text{ mV}$ The VBUS output voltage is calculated as $\text{VBUS} = \text{VBUSREF\_E} \times \left(1 + \frac{\text{RUP}}{\text{RDOWM}}\right)$ VBUSREF_E_SET range: 0 ~ 255 0000 0000: 0 0000 0001: 1 0000 0010: 2 .... 0111 1100: 124 (default) .... 1111 1111: 255	

				The default reference voltage is $(4 \times 124 + 3 + 1) \times 2 \text{ mV} = 1 \text{ V}$	
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Table 5 0x04H VBUSREF\_E\_SET\_2 Register

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7-6	R/W	VBUSREF_E_SET2	11	<p>Reference voltage programming for external VBUS voltage setting.</p> <p>When FB_SEL = 1 (external VBUS setting), set the lowest 2-bit of the reference voltage for VBUS (total 10-bit programming).</p> <p>The external reference voltage is calculated as</p> $\text{VBUSREF\_E} = (4 \times \text{VBUSREF\_E\_SET} + \text{VBUSREF\_E\_SET}2 + 1) \times 2 \text{ mV}$ <p>The VBUS output voltage is calculated as</p> $\text{VBUS} = \text{VBUSREF\_E} \times \left(1 + \frac{\text{RUP}}{\text{RDOWN}}\right)$ <p>VBUSREF_E_SET2 range: 0 ~ 3</p> <p>00: 0 01: 1 10: 2 11: 3 (default)</p>	
5-0		Reserved	xx xxxx		

Table 6 0x05H IBUS\_LIM\_SET Register

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7-0	R/W	IBUS_LIM_SET	1111 1111	<p>Set IBUS current limit, which is valid for both charging and discharging modes.</p> $\text{IBUS\_LIM (A)} = \frac{(\text{IBUS\_LIM\_SET} + 1)}{256} \times \text{IBUS\_RATIO} \times \frac{10 \text{ m}\Omega}{\text{RS1}}$ <p>RS1 is the current sense resistor at VBUS side.</p> <p>IBUS_LIM_SET range: 0 ~ 255</p> <p>0000 0000: 0 0000 0001: 1 0000 0010: 2 ... 1111 1111: 255 (default)</p> <p>E.g., if RS1 = 10 mΩ, the default IBUS current limit is <math>(255+1)/256 \times 3 \times 10 \text{ m}\Omega / 10 \text{ m}\Omega = 3 \text{ A}</math></p>	<b>IBUS_LIM_SET must be &gt;=300mA</b>

Table 7 0x06H IBAT\_LIM\_SET Register

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7-0	R/W	IBAT_LIM_SET	1111 1111	<p>Set IBAT current limit, which is valid for both charging and discharging modes.</p> $IBAT\_LIM(A) = \frac{IBAT\_LIM\_SET+1}{256} \times IBAT\_RATIO \times \frac{10\text{ m}\Omega}{RS2}$ <p>RS2 is the current sense resistor at VBAT side.</p> <p>IBAT_LIM_SET range: 0 ~ 255</p> <p>0000 0000: 0</p> <p>0000 0001: 1</p> <p>0000 0010: 2</p> <p>...</p> <p>1111 1111: 255 (default)</p> <p>E.g., if RS2 = 10 mΩ, the default IBAT current limit is (255+1)/256 x 12 x 10 mΩ / 10 mΩ = 12 A</p>	IBAT_LIM_SET must be >=300mA

Table 8 0x07H VINREG\_SET Register

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7-0	R/W	VINREG_SET	0010 1100	<p>Set VINREG reference voltage for charging mode.</p> $VINREG = (VINREG\_SET+1) \times VINREG\_RATIO \text{ (mV)}$ <p>VINREG_SET range: 0 ~ 255</p> <p>0000 0000: 0</p> <p>0000 0001: 1</p> <p>...</p> <p>0010 1100: 44 (default)</p> <p>...</p> <p>1111 1111: 255</p> <p>If VINREG_RATIO = 1 (40x), the default VINREG voltage is 1.8V, and the maximum VINREG voltage which can be set is 10.24V;</p> <p>If VINREG_RATIO = 0 (100x), the default VINREG voltage is 4.5V, and the maximum VINREG voltage which can be set is 25.6V.</p>	

Table 9 0x08H RATIO Register

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7-6	R/W	Reserved	00	<b>Internal use. Don't overwrite this bit.</b>	
5	R/W	Reserved	1	<b>Internal use. Don't overwrite this bit.</b>	
4	R/W	IBAT_RATIO	1	<p>IBAT_LIM setting ratio</p> <p>0: 6x</p> <p>1: 12x (default)</p>	Set this bit during PSTOP pin is high

3-2	R/W	IBUS_RATIO	10	IBUS_LIM setting ratio 00: not allowed 01: 6x 10: 3x (default) 11: not allowed	Set this bit during PSTOP pin is high
1	R/W	VBAT_MON_RATIO	0	Ratio setting for VBAT voltage monitor 0: 12.5x (default) 1: 5x  The battery voltage is monitored through ADC and can be calculated as below: $VBAT = (4 \times VBAT\_FB\_VALUE + VBAT\_FB\_VALUE2 + 1) \times VBAT\_MON\_RATIO \times 2 \text{ mV}$ VBAT_FB_VALUE and VBAT_FB_VALUE2 are ADC register values. <b>For 1S and 2S battery applications (VBAT &lt; 9V), set this bit to 1.</b>	Set this bit during PSTOP pin is high
0	R/W	VBUS_RATIO	0	Set the ratio for VBUS voltage setting and VBUS voltage monitor. 0: 12.5x (default) 1: 5x	Set this bit during PSTOP pin is high

Table 10 0x09H CTRL0\_SET Register

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7	R/W	EN_OTG	0	Enable OTG operation 0: set the charger to work in charging mode (default) 1: set the charger to work in discharging mode	
6	R/W	Reserved	0	<b>Internal use. Don't overwrite this bit.</b>	
5	R/W	Reserved	0	<b>Internal use. Don't overwrite this bit.</b>	
4	R/W	VINREG_RATIO	0	VINREG setting ratio 0: 100x (default) 1: 40x <b>Set this bit to 1 when VBUS &lt; 12V.</b>	
3-2	R/W	FREQ_SET	01	Switching frequency setting 00: 150kHz 01: 300kHz (default) 10: 300kHz 11: 450kHz	Set this bit during PSTOP pin is high
1-0	R/W	DT_SET	00	Switching dead time setting 00: 20ns (default) 01: 40ns 10: 60ns 11: 80ns	Set this bit during PSTOP pin is high

Table 11 0x0AH CTRL1\_SET Register

Bit	Mode	Symbol	Default value @POR	Description	Notes
7	R/W	ICHAR_SEL	0	Charging current selection 0: IBUS as charging current, the trickle charging current and termination current will be based on IBUS (default) 1: IBAT as charging current, the trickle charging current and termination current will be based on IBAT	Set this bit during PSTOP pin is high
6	R/W	DIS_TRICKLE	0	Trickle charge control 0: enable trickle charge phase (default) 1: disable trickle charge phase	Set this bit during PSTOP pin is high
5	R/W	DIS_TERM	0	Charging termination control 0: enable auto-termination (default) 1: disable auto-termination	Set this bit during PSTOP pin is high
4	R/W	FB_SEL	0	VBUS voltage setting control, only for discharging mode 0: internal VBUS setting, VBUS output voltage is set by VBUS_RATIO bit and VBUSREF_1_SET bits (default) 1: external VBUS setting, VBUS output voltage is set by resistor divider at FB pin	Set this bit during PSTOP pin is high
3	R/W	TRICKLE_SET	0	Trickle charge phase threshold setting 0: 70% of VBAT voltage setting (default) 1: 60% of VBAT voltage setting	Set this bit during PSTOP pin is high
2	R/W	DIS_OVP	0	OVP protection setting for discharging mode 0: enable OVP protection (default) 1: disable OVP protection	
1	R/W	Reserved	0	<b>Internal use. Don't overwrite this bit.</b>	
0	R/W	Reserved	1	<b>Internal use. Don't overwrite this bit.</b>	

Table 12 0x0BH CTRL2\_SET Register

Bit	Mode	Symbol	Default value @POR	Description	Notes
7-4	R/W	Reserved	0000	<b>Internal use. Don't overwrite this bit.</b>	
3	R/W	FACTORY	0	<b>Factory setting bit. MCU shall write this bit to 1 after power up.</b>	
2	R/W	EN_DITHER	0	Enable switching frequency dithering function at PGATE pin: 0: disable frequency dithering function, PGATE pin used as PMOS gate control (default) 1: enable frequency dithering function, PGATE pin used to set the frequency dithering	Set this bit during PSTOP pin is high
1-0	R/W	SLEW_SET	01	Slew rate setting for VBUS dynamic change in discharging mode 00: 1mV/μs 01: 2mV/μs (default)	Set this bit during PSTOP pin is high

				10: 4mV/μs 11: 8mV/μs	
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Table 13 0x0CH CTRL3\_SET Register

Bit	Mode	Symbol	Default value @POR	Description	Notes
7	R/W	EN_PGATE	0	PGATE control 0: PGATE outputs logic high to turn off PMOS (default) 1: PGATE outputs logic low to turn on PMOS	
6	R/W	GPO_CTRL	0	GPO output control 0: Open drain output (default) 1: Logic low output	
5	R/W	AD_START	0	ADC control 0: stop ADC conversion (default) 1: start ADC conversion, MCU can read the voltage/current values from ADC registers	
4	R/W	ILIM_BW_SEL	0	ILIM loop bandwidth setting: 0: 5kHz (default) 1: 1.25kHz	Set this bit during PSTOP pin is high
3	R/W	LOOP_SET	0	Loop response control 0: Normal loop response (default) 1: Improve the loop response	Set this bit during PSTOP pin is high
2	R/W	DIS_ShortFold Back	0	IBUS and IBAT current foldback control for VBUS short circuit condition, only valid in discharging mode 0: IBUS and IBAT current limit value are fold-back to 22% and 10% of setting value respectively (default) 1: disable fold-back.	
1	R/W	EOC_SET	1	Current threshold setting for End Of Charging (EOC) detection 0: 1/25 of charging current 1: 1/10 of charging current (default)	Set this bit during PSTOP pin is high
0	R/W	EN_PFM	0	PFM control under light load condition, only for discharging mode 0: disable PFM mode (PWM mode enabled) (default) 1: enable PFM mode	

Table 14 0x0DH VBUS\_FB\_VALUE Register

Bit	Mode	Symbol	Default value @POR	Description	Notes
7-0	R	VBUS_FB_VALUE	0000 0000	The highest 8-bit of the ADC reading of VBUS voltage (total 10-bit). VBUS voltage is calculated as $VBUS = (4 \times VBUS\_FB\_VALUE + VBUS\_FB\_VALUE2 + 1) \times VBUS\_RATIO \times 2 \text{ mV}$	

				VBUS_FB_VALUE range: 0 ~ 255 0000 0000: 0 0000 0001: 1 0000 0010: 2 .... 1111 1111: 255	
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Table 15 0x0EH VBUS\_FB\_VALUE\_2 Register

Bit	Mode	Symbol	Default value @POR	Description	Notes
7-6	R	VBUS_FB_VALUE2	00	The lowest 2-bit of the ADC reading of VBUS voltage (total 10-bit). VBUS voltage is calculated as $VBUS = (4 \times VBUS\_FB\_VALUE + VBUS\_FB\_VALUE2 + 1) \times VBUS\_RATIO \times 2 \text{ mV}$ VBUS_FB_VALUE2 range: 0 ~ 3 00: 0 01: 1 10: 2 11: 3	
5-0		Reserved	00 0000		

Table 16 0x0FH VBAT\_FB\_VALUE Register

Bit	Mode	Symbol	Default value @POR	Description	Notes
7-0	R	VBAT_FB_VALUE	0000 0000	The highest 8-bit of the ADC reading of VBAT voltage (total 10-bit). VBAT voltage is calculated as $VBAT = (4 \times VBAT\_FB\_VALUE + VBAT\_FB\_VALUE2 + 1) \times VBAT\_MON\_RATIO \times 2 \text{ mV}$ VBAT_FB_VALUE range: 0 ~ 255 0000 0000: 0 0000 0001: 1 0000 0010: 2 .... 1111 1111: 255	

Table 17 0x10H VBAT\_FB\_VALUE\_2 Register

Bit	Mode	Symbol	Default value @POR	Description	Notes



7-6	R	VBAT_FB_VALUE_2	00	<p>The lowest 2-bit of the ADC reading of VBAT voltage (total 10-bit). VBAT voltage is calculated as</p> $VBAT = (4 \times VBAT\_FB\_VALUE + VBAT\_FB\_VALUE2 + 1) \times VBAT\_MON\_RATIO \times 2 \text{ mV}$ <p>VBAT_FB_VALUE_2 range: 0 ~ 3</p> <p>00: 0 01: 1 10: 2 11: 3</p>	
5-0		Reserved	00 0000		

Table 18 0x11H IBUS\_VALUE Register

Bit	Mode	Symbol	Default value @POR	Description	Notes
7-0	R	IBUS_VALUE	0000 0000	<p>The highest 8-bit of the ADC reading of IBUS current (total 10-bit). IBUS current is calculated as</p> $IBUS(A) = \frac{(4 \times IBUS\_VALUE + IBUS\_VALUE2 + 1) \times 2}{1200} \times IBUS\_RATIO \times \frac{10 \text{ m}\Omega}{RS1}$ <p>IBUS_VALUE range: 0 ~ 255</p> <p>0000 0000: 0 0000 0001: 1 0000 0010: 2 .... 1111 1111: 255</p>	

Table 19 0x12H IBUS\_VALUE\_2 Register

Bit	Mode	Symbol	Default value @POR	Description	Notes
7-6	R	IBUS_VALUE_2	00	<p>The lowest 2-bit of the ADC reading of IBUS current (total 10-bit). IBUS current is calculated as</p> $IBUS(A) = \frac{(4 \times IBUS\_VALUE + IBUS\_VALUE2 + 1) \times 2}{1200} \times IBUS\_RATIO \times \frac{10 \text{ m}\Omega}{RS1}$ <p>IBUS_VALUE2 range: 0 ~ 3</p> <p>00: 0 01: 1 10: 2 11: 3</p>	
5-0		Reserved	00 0000		

Table 20 0x13H IBAT\_VALUE Register

Bit	Mode	Symbol	Default value @POR	Description	Notes
7-0	R	IBAT_VALUE	0000 0000	<p>The highest 8-bit of the ADC reading of IBAT current (total 10-bit).</p> <p>IBAT current is calculated as</p> $IBAT(A) = \frac{(4 \times IBAT\_VALUE + IBAT\_VALUE2 + 1) \times 2}{1200} \times IBAT\_RATIO \times \frac{10\text{ m}\Omega}{RS2}$ <p>IBAT_VALUE range: 0 ~ 255</p> <p>0000 0000: 0</p> <p>0000 0001: 1</p> <p>0000 0010: 2</p> <p>....</p> <p>1111 1111: 255</p>	

Table 21 0x14H IBAT\_VALUE\_2 Register

Bit	Mode	Symbol	Default value @POR	Description	Notes
7-6	R	IBAT_VALUE_2	00	<p>The lowest 2-bit of the ADC reading of IBAT current (total 10-bit).</p> <p>IBAT current is calculated as</p> $IBAT(A) = \frac{(4 \times IBAT\_VALUE + IBAT\_VALUE2 + 1) \times 2}{1200} \times IBAT\_RATIO \times \frac{10\text{ m}\Omega}{RS2}$ <p>IBAT_VALUE2 range: 0 ~ 3</p> <p>00: 0</p> <p>01: 1</p> <p>10: 2</p> <p>11: 3</p>	
5-0		Reserved	00 0000		

Table 22 0x15H ADIN\_VALUE Register

Bit	Mode	Symbol	Default value @POR	Description	Notes
7-0	R	ADIN_VALUE	0000 0000	<p>The highest 8-bit of the ADC reading of ADIN voltage (total 10-bit).</p> <p>ADIN voltage is calculated as</p> $VADIN = (4 \times ADIN\_VALUE + ADIN\_VALUE2 + 1) \times 2\text{ mV}$ <p>ADIN_VALUE range: 0 ~ 255</p> <p>0000 0000: 0</p> <p>0000 0001: 1</p> <p>0000 0010: 2</p> <p>....</p>	

				1111 1111: 255	
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Table 23 0x16H ADIN\_VALUE\_2 Register

Bit	Mode	Symbol	Default value @POR	Description	Notes
7-6	R	ADIN_VALUE_2	00	The lowest 2-bit of the ADC reading of ADIN voltage (total 10-bit). ADIN voltage is calculated as $V_{ADIN} = (4 \times ADIN\_VALUE + ADIN\_VALUE_2 + 1) \times 2 \text{ mV}$ ADIN_VALUE_2 range: 0 ~ 3 00: 0 01: 1 10: 2 11: 3	
5-0		Reserved	00 0000		

Table 24 0x17H STATUS Register

Bit	Mode	Symbol	Default value @POR	Description	Notes
7	R	Reserved	0	Reserved	
6	R	AC_OK	0	1: AC adapter is inserted	
5	R	INDET	0	1: USB-A load insert is detected at INDET pin	
4	R	Reserved	0	Reserved	
3	R	VBUS_SHORT	0	1: VBUS short circuit fault happens in discharging mode	
2	R	OTP	0	1: OTP fault happens	
1	R	EOC	0	1: EOC conditions are satisfied	
0	R	Reserved	0		

Table 25 0x19H MASK Register

Bit	Mode	Symbol	Default value @POR	Description	Notes
7	R/W	Reserved	1	<b>Internal use. Don't overwrite this bit.</b>	
6	R/W	AC_OK_Mask	0	1: Interrupt is disabled	
5	R/W	INDET_Mask	0	1: Interrupt is disabled	

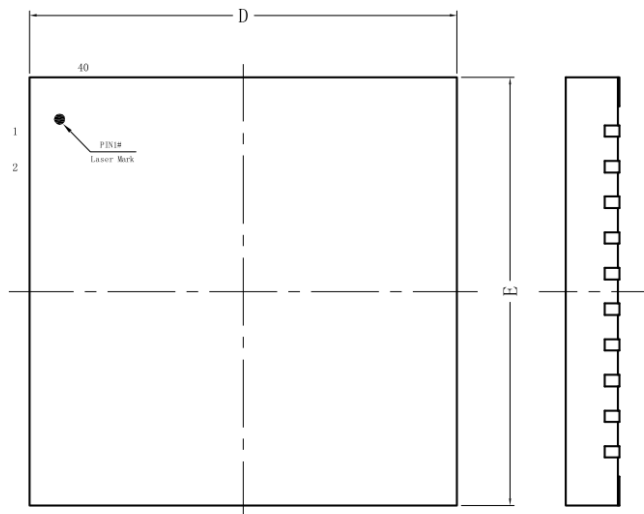


4	R/W	Reserved	0	<b>Internal use. Don't overwrite this bit.</b>	
3	R/W	VBUS_SHORT_Mask	0	1: Interrupt is disabled	
2	R/W	OTP_Mask	0	1: Interrupt is disabled	
1	R/W	EOC_Mask	0	1: Interrupt is disabled	
0	R/W	Reserved	0	<b>Internal use. Write this bit to 1 after power up.</b>	

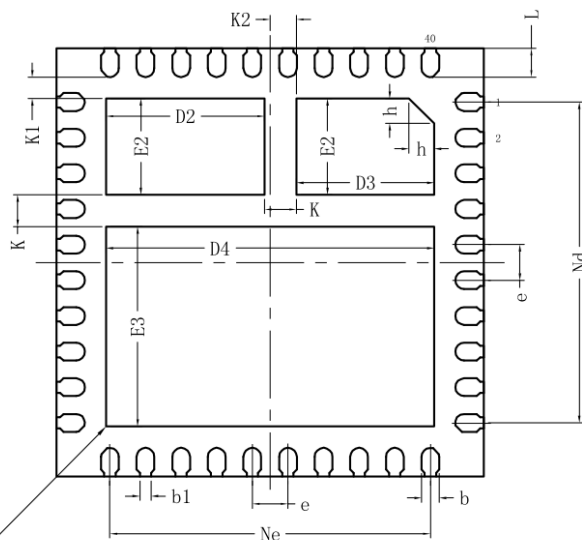
SOUTHCHIP CONFIDENTIAL

MECHANICAL DATA

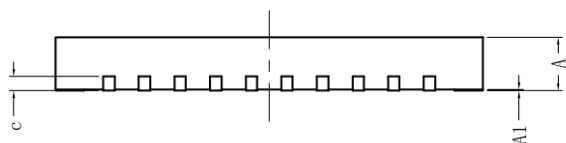
QFN40L(6x6x0.75)



TOP VIEW



BOTTOM VIEW



SIDE VIEW

EXPOSED THERMAL  
PAD ZONE

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.20	0.25	0.30
b1	0.16REF		
c	0.18	0.20	0.25
D	5.90	6.00	6.10
D2	2.12	2.22	2.32
D3	1.83	1.93	2.03
D4	4.50	4.60	4.70
e	0.50BSC		
Ne	4.50BSC		
Nd	4.50BSC		
E	5.90	6.00	6.10
E2	1.25	1.35	1.45
E3	2.70	2.80	2.90
L	0.35	0.40	0.45
h	0.30	0.35	0.40
K	0.40	0.45	0.50
K1	0.25	0.30	0.35
K2	0.32	0.37	0.42

单击下面可查看定价，库存，交付和生命周期等信息

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