SC8902A High Efficiency, Synchronous, Bi-Directional Buck-Boost Charge Converter with Four Integrated MOSFET

1 Description

SC8902A is a synchronous 4-switch buck-boost charger controller which also supports reverse discharging operation. Four switches are integrated to simplify the system design. It is able to effectively manage charging for 1~3 cell batteries no matter input/output voltage is higher, lower or equal to battery voltage. When system needs to discharge from battery, SC8902A will deliver desired output from the battery.

SC8902A supports very wide input and output voltage range. It can support applications from 2.7V to 22V input range and 2.7V to 22V output range. It employs current-mode control and can support bi-directional outputs by controlling DIR pin. It supports input current limit, output current limit, DPM (dynamic power management) function, dynamic output voltage adjustment, internal current limit, output short protection and over temperature protections to ensure safety under different abnormal conditions.

The SC8902A is in a 40 pin 6x6 QFN package.

2 Features

- Buck-Boost Battery Charger for 1 to 3 Cell Batteries
- Charging Management: trickle Charging, CC Charging, CV Charging and Charging Termination
- Buck-Boost Reverse Discharging Mode
- Integrated Four Switches
- Wide VBAT Range: 2.7 V to 14 V, 24V sustainable
- Wide VBUS Range: 2.7 V to 22 V, 24V sustainable
- High Efficiency Buck-Boost Conversion
- DP / DM Handshaking for Fast Charging Mode
- Dynamic Output Voltage Control
- Programmable Input and Output Current Limit
- Dynamic Input Current Limit Control
- Input and Output Current Monitor
- Charging Status Indication and Small Current Indication
- Under Voltage Protection, Over Voltage Protection, Over Current Protection
- Short Protection and Thermal Shutdown Protection
- QFN-40 Package

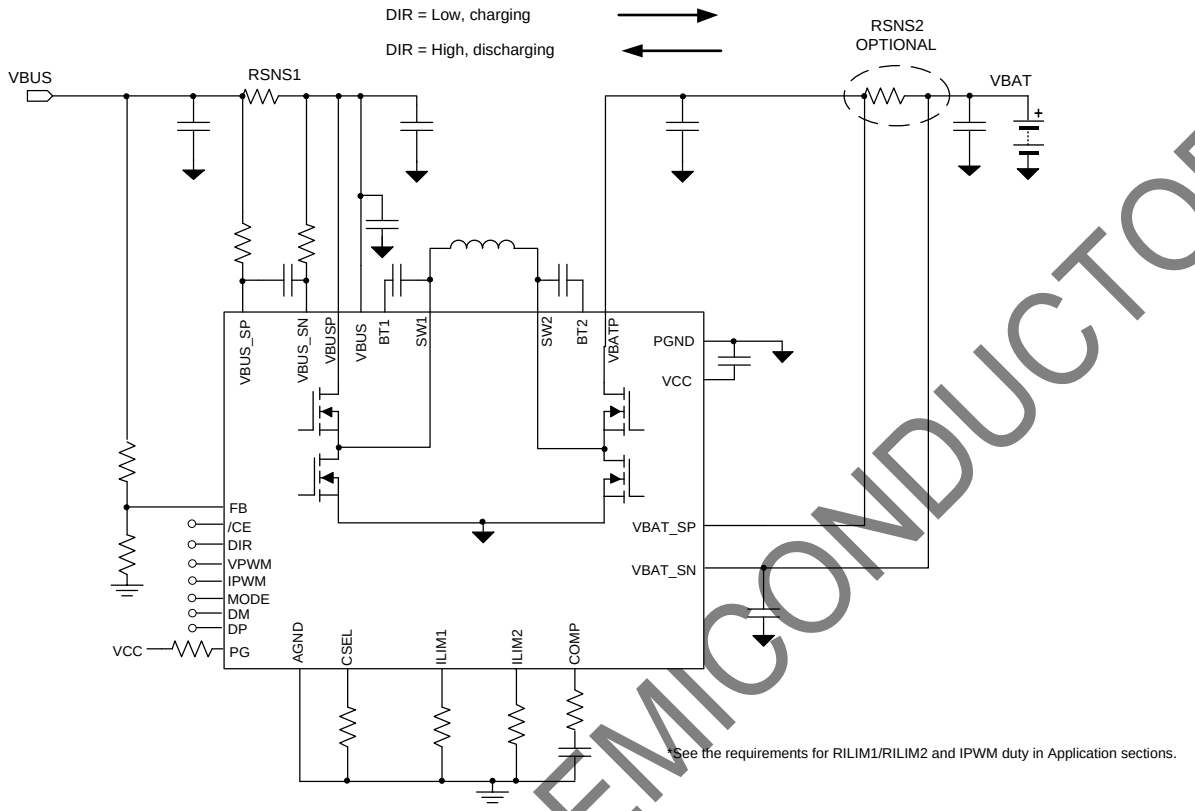
3 Applications

- Power Bank with Fast Charge Function
- USB Power Delivery
- Type C Hub
- Industrial Power Supplies

4 Device Information

Part Number	Package	Dimension
SC8902AQDHR	40 pin QFN	6.0mm x 6.0mm x 0.75mm

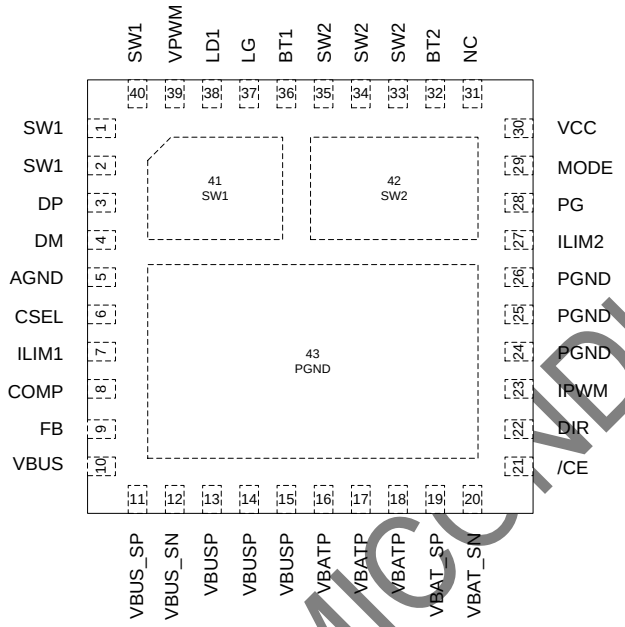
5 Typical Application Circuit



*See the requirements for RILIM1/RILIM2 and IPWM duty in Application sections.

6 Terminal Configuration and Functions

SC8902A
Top View



TERMINAL		I/O	DESCRIPTION
NUMBER	NAME		
1, 2	SW1	I/O	Switching Node 1. Connect to inductor.
3	DP	I/O	Handshaking for 9V fast charging
4	DM	I/O	Handshaking for 9V fast charging
5	AGND	I/O	Analog ground. Connect PGND and AGND together at the thermal pad under IC.
6	CSEL	I	Use this pin to set the battery termination voltage for charging mode.
7	ILIM1	I	Connect a resistor RILIM1 from this pin to AGND to set the VBUS side current limit for both charging mode and discharging mode. See the requirements for RILIM1 in Application sections.
8	COMP	I	Connect a RC network to compensate the control loop.
9	FB	I	Feedback node of VBUS output voltage. Set the VBUS output voltage in discharging mode by the resistor divider connected at this pin.
10	VBUS	P	Connect to VBUS node to provide power supply to the IC. Connect a 1 μF capacitor from this pin to PGND close to IC.
11	VBUS_SP	I	Positive input of an internal current sense amplifier. Connect a current sense resistor (typical 10 mΩ) between VBUS_SP and VBUS_SN to sense the IBUS current.

12	VBUS_SN	I	Negative input of an internal current sense amplifier. Connect a current sense resistor (typical 10 mΩ) between VBUS_SP and VBUS_SN to sense the IBUS current.
13 – 15	VBUSP	P	The power input node of the converter in charging mode (DIR = low), and the power output node of the converter in discharging mode (DIR = high). Normally connect these pins to a USB port.
16 - 18	VBATP	P	The power output node of the converter in charging mode (DIR = low), and the power input node of the converter in discharging mode (DIR = high). Connect these pins to the positive node of battery cells.
19	VBAT_SP	I	Positive input of an internal current sense amplifier. Connect a current sense resistor (typical 10 mΩ) between VBAT_SP and VBAT_SN to sense the IBAT current.
20	VBAT_SN	I	Negative input of an internal current sense amplifier. Connect a current sense resistor (typical 10 mΩ) between VBAT_SP and VBAT_SN to sense the IBAT current.
21	/CE	I	Chip enable pin, active low. That is, pull this pin to logic low to enable the chip. This pin is internally pulled low.
22	DIR	I	Charging/discharging mode control pin. When DIR is logic low, the IC works in charging mode, and the power direction is from VBUS to VBAT. When DIR is logic high, the IC works in discharging mode with power direction from VBAT to VBUS. This pin is internally pulled low.
23	IPWM	I	To apply a PWM signal on IPWM pin can adjust the IBUS current limit dynamically. See the requirements for duty cycle of IPWM signal in Application sections.
24-26	PGND	I/O	Power ground. Connect PGND and AGND together at the thermal pad under IC.
27	ILIM2	I	Connect a resistor RILIM2 from this pin to AGND to set the battery side current limit for both charging mode and discharging mode. See the requirements for RILIM2 in Application sections.
28	PG	O	Open drain output to indicate the charging/discharging status. Needs connect to a pull up resistor. When in charging mode (DIR = low), PG pin indicates EOC (end of charging) status: It outputs logic low when the IC is charging the battery; and outputs high impedance when the battery is fully charged. When in discharging mode (DIR = high), PG pin indicates load condition. It outputs logic low when the load is higher than 50mA typically, and outputs high impedance when the load is lower than the threshold.
29	MODE	I	In discharging mode (DIR = high), MODE pin controls the PFM/PWM operation mode under light load condition. In charging mode (DIR = low), MODE pin controls the termination way when EOC condition is detected.
30	VCC	O	Output of an internal regulator. Connect a 1 μF ceramic capacitor from VCC to PGND pin close to the IC. The regulator provides supply for internal gate drivers.
31	NC		NC pin. Leave it floating.
32	BT2	I	Connect a 100nF ceramic capacitor between BT2 pin and SW2 pin to provide the boosted bias voltage for high side gate driver.
33 – 35	SW2	I/O	Switching Node 2. Connect to inductor.
36	BT1	I	Connect a 100nF capacitor between BT1 pin and SW1 pin to provide the boosted bias voltage for high side gate driver.

37	LG	I	Gate input of the integrated low side MOSFET. Connect to LD1 pin with or without a driving resistor in between.
38	LD1		Gate driver output to the integrated low side MOSFET. User can short LD1 pin and LG pin directly, or connect a driving resistor between LD1 and LG pins to limit the driver current.
39	VPWM	I	When in discharging mode (DIR = high), VPWM pin is to adjust the VBUS output voltage in real time. When in charging mode (DIR = low), VPWM signal controls the VINREG voltage threshold. This pin is internally pulled **HIGH.**
40	SW1	I/O	Switching Node 1. Connect to inductor.
41	SW1	I/O	Switching pad 1. Connect to SW1 pins.
42	SW2	I/O	Switching pad 2. Connect to SW2 pins.
43	PGND	I/O	Power ground pad. For thermal dissipation. Connect to AGND and PGND pins together.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	Unit
Voltage range at terminals(2)	VPWM, DP, DM, CSEL, ILIM1, COMP, IPWM, ILIM2, MODE, VCC	-0.3	5.5	V
	FB, VBUS, VBUS_SP, VBUS_SN, VBUSP, VBATP, VBAT_SP, VBAT_SN, /CE, DIR, PG	-0.3	24	V
	SW1, SW2	-0.3	30	V
	BT1, BT2	-0.3	40	V
T_J	Operating junction temperature range	-40	150	°C
T_{stg}	Storage temperature range	-65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

7.2 Thermal Information

THERMAL RESISTANCE(1)		QFN-40 (6mm x 6mm)	UNIT
Θ_{JA}	Junction to ambient thermal resistance	58	°C/W
Θ_{JC}	Junction to case resistance	5	°C/W

(1) Measured on JESD51-7, 4-layer PCB.

7.3 Handling Ratings

PARAMETER	DEFINITION		MIN	MAX	UNIT
ESD(1)	Human body model (HBM) ESD stress voltage(2)	All pins except DP, DM	-2	2	kV
		DP, DM	-8	8	kV
	Charged device model (CDM) ESD stress voltage(3)		-750	750	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.4 Recommended Operating Conditions(1)

		MIN	MAX	UNIT
V_{BUS}	VBUS voltage range	2.7	22	V
V_{BAT}	VBAT voltage range	2.7	22	V
C_{BUS}, C_{BAT}	VBUS Capacitance, VBAT capacitance	30		µF
L	Inductance	2.2	10	µH
$R_{SNS1/2}$	Current Sensing Resistor	0	20	mΩ
f_{PWM}	PWM singal frequency range	20	100	kHz

D_{PWM}	PWM signal duty cycle range	0	100	%
T_A	Operating ambient temperature	-40	85	°C
T_J	Operating junction temperature	-40	125	°C

(1) See the requirements for RILIM1 / RILIM2 and the duty cycle of IPWM signal in Application sections.

7.5 Electrical Characteristics

T_J= 25°C and V_{IN}= 5V unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
V_{UVLO_VBAT}	VBAT under-voltage lockout threshold	Rising edge		2.5	2.6	V
		Hysteresis		160		mV
V_{UVLO_VBUS}	VBAT under-voltage lockout threshold	Rising edge		2.5	2.6	V
		Hysteresis		160		mV
I_Q	Quiescent current into VBAT	VBAT = 8V, VBUS = 5V /CE = L, non-switching		4		mA
		VBAT = 8V, VBUS = 12V /CE = L, non-switching		1		mA
I_{SD}	Shutdown current into VBAT	VBAT = 8V, /CE = H		5.5	15	μA
I_{LKG}	Leakage current into VBATP pins	/CE = H, VBATP = 8V			100	nA
VCC, DIRVER AND POWER SWITCH						
V_{CC}	VCC regulation voltage	VBAT = 9V		5.35	5.45	V
		VBAT = 5V, ICC = 30mA		4.1	4.2	V
I_{VCC_LIM}	VCC current limit	VBAT = 9V, VCC = 4V		170	270	mA
R_{HS/LS_PU}	High/low side MOS driver pull up resistor			4.6		Ω
R_{HS/LS_PD}	High/low side MOS driver pull down resistor			0.7		Ω
R_{DSon_HS}	High side MOS on resistance			22		mΩ
R_{DSon_LS}	Low side MOS on resistance			8.5		mΩ
REFERENCE VOLTAGE FOR VBUS						
V_{FB1}	FB reference voltage		1.176	1.2	1.224	V
V_{FB1_OVP}	FB OVP threshold, over FB target	Rising edge	107%	109.5%	112%	
		Hysteresis		2%		
V_{BUS_OVP}	Absolute OVP threshold for VBUS		21.5	22	22.5	V
V_{SHORT}	Short circuit detection threshold			0.7		V
V_{BAT_TRGT}	Battery target voltage	CSEL = 9.1kΩ	4.179	4.2	4.221	V
		CSEL = floating	8.35	8.4	8.45	V
		CSEL = 300kΩ	8.65	8.7	8.75	V
		CSEL = 150kΩ	8.75	8.8	8.85	V
		CSEL = 80kΩ	12.53	12.6	12.67	V
		CSEL = 40kΩ	12.98	13.05	13.12	V
		CSEL = 20kΩ	13.13	13.2	13.27	V
V_{BAT_TERM}	Termination threshold over V_{BAT_TRGT}		97%	97.7%	98.5%	
V_{BAT_RECH}	Recharge threshold over V_{BAT_TRGT}			96%		
V_{TRK_CH}	Trickle charge threshold over V_{BAT_TRGT}		55%	60%	65%	
I_{BUS_TRK}	IBUS trickle charge current, over ILIM1 set current			10%		
I_{BUS_TERM}	IBUS current termination threshold, over ILIM1 set current			8%		

V_{BAT_OVP}	OVP threshold, over VBAT target			110%		
V_{BAT_OVP}	Absolute OVP threshold for VBAT		21.5	22	22.5	V
CURRENT LIMIT						
V_{LIM_REF}	ILIM1 / ILIM2 reference voltage		1.176	1.2	1.224	V
I_{BUS_LIM}	IBUS current limit accuracy	DIR = 0 $I_{OUT} R_{SNS1} \geq 20mV$	-10%		10%	
		DIR = 1 $I_{OUT} R_{SNS1} \geq 20mV$	-10%		10%	
I_{BAT_LIM}	IBAT current limit accuracy	DIR = 0 $I_{BAT\_LIM} R_{SNS1} \geq 20mV$	-10%		10%	
		DIR = 1 $I_{BAT\_LIM} R_{SNS1} \geq 20mV$	-25%		25%	
ERROR AMPLIFIER						
Gm_{EA}	Error amplifier gm			0.16		mS
R_{OUT}	Error amplifier output resistance			20		MΩ
I_{SINK_COMP}	COMP sink current			27		μA
I_{SRC_COMP}	COMP source current			16		μA
I_{BIAS_FB}	FB pin input bias current	FB in regulation			50	nA
SWITCHING						
f_{SW}	Switching frequency			460		kHz
INDICATION						
I_{SINK_PG}	PG pin sink current	V_{PG} = 0.4V		4		mA
I_{COM}	Small load threshold			60		mA
LOGIC CONTROL						
R_{PD}	/CE/DIR pin internal pull down resistor			1.2		MΩ
	VPWM pin internal pull up resistor			0.9		MΩ
V_{IL}	/CE, DIR, VPWM and MODE pins input low voltage				0.4	V
V_{IH}	/CE, DIR, VPWM pins input high voltage		1.2			V
	MODE pin input high voltage		2			V
SOFTSTART						
t_{SS}	Internal soft-start time	From 10% to 90% VOUT		5		ms
DPDM						
V_{DP_SRC}	D+ source voltage		0.5	0.6	0.7	V
V_{DM_SRC}	D- source voltage		0.5	0.6	0.7	V
I_{DP_sink}	D+ sink current		25	100	175	μA
I_{DM_sink}	D- sink current		25	100	175	μA
V_{DAT_REF}	Data detect voltage		0.25	0.325	0.4	V
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown temperature (1)			165		°C
	Thermal shutdown hysteresis (1)			15		°C

8 Detailed Description

8.1 Chip Enable

The IC is enabled or disabled by /CE signal. When /CE input is logic low, the IC is enabled; when /CE input is logic high, the IC is disabled. The /CE pin is pulled low by 1 MΩ resistor internally.

8.2 Charging Mode

Charging mode and discharging mode is controlled by DIR pin, which is internally pulled low by 1 MΩ resistor.

When DIR signal is logic low, the IC works in charging mode. The current flows from VBUS to VBAT to charge the battery cells.

When in charging mode, the IC charges the battery cells according to below typical charging profile. When battery voltage is lower than trickle charge threshold, the IC charges the cells with small charging current; when cell voltage is higher than the threshold, the IC enters into Constant Current charging phase, and charges the cells with constant current set by IBUS limit or IBAT limit. When the cell voltage reaches the termination voltage target, the IC enters into Constant Voltage charge phase, and charges the cells with gradually decreased current until the current is lower than termination current threshold. Once termination voltage and termination current conditions are satisfied, the IC enters into End of Charge phase. In this phase the IC can either terminate the charging or keep charging the cells.

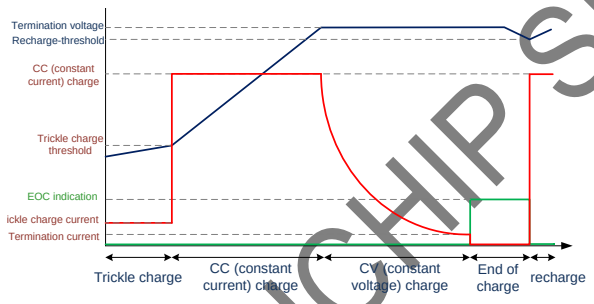


Figure 1 Typical Charging Profile

8.2.1 Trickle Charge

The trickle charge voltage threshold is 60% of battery target voltage. When in trickle charge phase, the IBUS charging current is reduced to 1/10 of current limit set value for the good of battery cells.

8.2.2 CC Charge (Constant Current Charge)

When cell voltage is higher than the trickle threshold, the IC charges the battery cells with constant current set by IBUS limit or IBAT limit. The user can set the IBUS limit and IBAT limit through ILIM1 and ILIM2 pins respectively as below:

$$IBUS\_LIM = \frac{VLIM\_REF}{RILIM1} \times \frac{1000\ \Omega}{RSNS1}$$

$$IBAT\_LIM = \frac{VLIM\_REF}{RILIM2} \times \frac{1000\ \Omega}{RSNS2}$$

where

V_{LIM_REF} = Internal reference voltage 1.21V;

R_{ILIMx} = Resistors at ILIMx pin;

R_{SNS1} = Current sense resistor to sense IBUS current;

R_{SNS2} = Current sense resistor to sense IBAT current

In charging mode, the IC regulates the current which reaches its current limit value first. For example, if IBUS current limit is set to 3A, IBAT limit is set to 10A, and when IBUS reaches 3A, IBAT is only 6A, which is much lower than IBAT limit 10A, then the IC limits the IBUS at 3A.

For correct CC charge operation, the IBUS current limit must be set, but IBAT current limit is not necessary. So if battery current limit is not needed for applications, user can short ILIM2 pin to ground to disable IBAT current limit function.

It is not allowed to set any of the current limits to 0A. Keep the minimum current limit above 0.3A.

8.2.3 CV Charge (Constant Voltage Charge)

The battery target voltage is set by CSEL pin.

When the IC is enabled, the IC checks the resistor value at CSEL pin and set the charge termination voltage internally.

Below table shows the resistor value to set different charge termination voltages.

Table 1 CSEL pin resistor to set battery voltage

CSEL resistor value	Charge termination voltage
9.1 kΩ	4.2V
open	8.4V
300 kΩ	8.7V
150 kΩ	8.8V
80 kΩ	12.6V
40 kΩ	13.05V
20 kΩ	13.2V

When the battery cell voltage reaches 98% of the cell target voltage, the IC enters into CV charge phase. In this phase, the VBAT voltage is regulated at target value, and the charging current reduces gradually.

8.2.4 EOC (End of Charge) and PG Indication

When both of below voltage condition and current condition for EOC detection are satisfied, the IC enters into EOC phase, and indicates the EOC status to MCU through PG

pin.

1. the cell voltage is higher than 98% of set value
2. the IBUS current is lower than 8% of the IBUS current limit set value

In EOC phase, the IC can terminate the charging process or keep charging the battery cells, which can be set by MODE pin as below table shows.

Table 2 Termination Selection

MODE Input	Operation Mode
Logic low	Auto-terminate charging at EOC phase
Logic high	Auto-terminate charging at EOC phase
Float	Keep charging and regulates the battery voltage at the termination target voltage.

No matter what termination way is set, the PG pin outputs high impedance once the IC detects the EOC condition.

PG is open drain output and it requires an external pullup resistor as below.

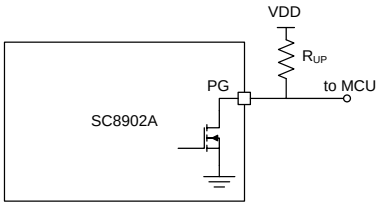


Figure 2 PG pin structure

8.2.5 Recharge

If the IC terminates the charging process after EOC is detected, the battery voltage may drop slowly due to leakage or operation current from battery cells. Once the VBAT voltage drops below 96% of the set voltage, the PG outputs low, and the IC enters into CC charge phase and recharges the battery.

8.2.6 Self-adaptive Charging Current

The IC features dynamic power management. The allowed minimum VBUS operation voltage is VINREG threshold, which can be set by VPWM signal. During charging, if the IBUS charging current is higher than adapter's current capability, the adapter will be overloaded and the VBUS voltage is pulled low. Once the VBUS voltage drops at VINREG threshold, the IC reduces the charging current automatically and regulates the VBUS voltage at VINREG threshold.

When in charging mode VPWM signal controls the VINREG threshold. If VPWM signal is logic high, the VINREG threshold is set to 4.5V; if VPWM signal is logic low, the VINREG threshold is set to 10.8V. If applying a PWM signal in the range of 20kHz~100kHz to VPWM pin, the VINREG threshold can be adjusted by the PWM duty cycle D as below equation shows.

$$VINREG = 4.5\ V + (1 - D) \times 6.3\ V$$

VPWM pin is internally pulled **HIGH.**

8.2.7 Real-Time Charge Current Control

The IBUS charging current can be controlled in real time through IPWM signal.

If a logic high signal is applied to IPWM pin, the IBUS limit is the default set value. If a logic low signal is applied, the IBUS limit is reduced to 10% of the set value. With a PWM signal in the range of 20kHz~100kHz at IPWM pin, the IBUS current limit is proportional to the duty cycle as below equation shows.

$$IBUS\_LIM = 0.1 \times IBUS\_LIM\_SET + 0.9 \times IBUS\_LIM\_SET \times D$$

where, IBUS_LIM_SET is the default IBUS current limit set by ILIM1 resistor.

8.3 Discharging Mode

When DIR signal is logic high, the IC enters into discharging mode. In discharging mode, the battery (VBAT) is discharged and the current flows from VBAT to VBUS.

The VBUS output voltage is set by the resistor divider connected at FB pin, and can be calculated as below.

$$VBUS = VFB\_REF \times \left(1 + \frac{RUP}{RDOWM}\right)$$

Where:

V_{FB_REF} is the internal reference voltage 1.2V, R_{UP} and R_{DWON} are the resistors connected from VBUS to FB and to AGND.

8.3.1 Soft Start

The IC implements soft start feature to prevent inrush current during startup in discharging mode. After the discharging mode is enabled, the IC ramps up the internal reference voltage in around 6ms. The output voltage follows the reference so it starts up slowly. Meantime, the IC ramps up the current limits during the startup. If a heavy load is applied before the output voltage is established, the IC may fail to start up due to the current limit.

For the applications which require startup with heavy load, below circuit is suggested. During startup, M2 is turned on by DIR signal, and VCC voltage ramps up quickly so V_B voltage is pulled up through C1 to turn on M1. So the ILIM1 pin is short to ground to disable the current limit for a moment. After V_B voltage drops due to the discharging path through 100k resistor, M1 is turned off. So the current limit recovers. The R1 resistor is optional. User can either NC it or use it to adjust the IBUS current limit in discharging mode.

The user can also adjust the startup current capability by adding a resistor in series with M1 and also adjust the recovery time by changing the C1 value.

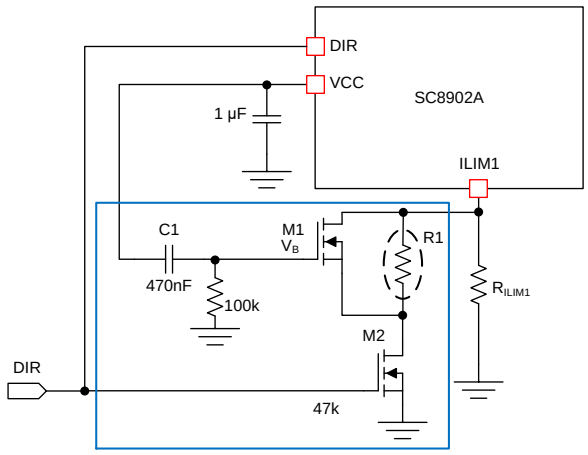


Figure 3 Circuit to support startup with heavey load

8.3.2 Dynamic Output Control

In charging mode, VPWM pin is used to set the VINREG threshold; in discharging mode, the VPWM pin can be used to control the output voltage dynamically.

The VPWM pin accepts a PWM signal in the range of 20kHz to 100kHz, and its duty cycle controls the output voltage as below:

$$VBUS = V_{BUS\_SET} \times D$$

Where;

V_{BUS_SET} = VBUS voltage set by FB resistor divider,

D = Duty cycle of VPWM signal.

If VPWM input signal is logic high, which means 100% of duty cycle, the output voltage becomes the set value V_{BUS_SET}.

If VPWM input signal is logic low, which means 0% of duty cycle, the output voltage becomes off.

The VPWM signal is internally pulled high, so if this dynamic output control function is not required, user can leave VPWM pin floating, then the IC outputs the set voltage V_{BUS_SET}.

When the dynamic output control function is used, the default V_{BUS_SET} voltage is normally a high voltage like 12V or 20V. In order to prevent the IC outputs the V_{BUS_SET} voltage when the VPWM signal is fault or open, it is suggested to add a 100 kΩ pull down resistor at this pin as below.

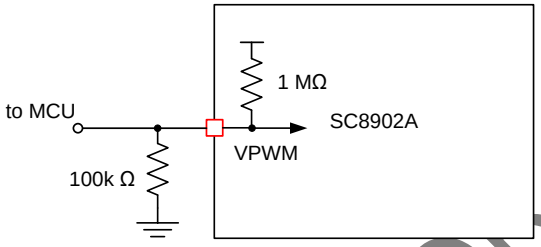


Figure 4 VPWM pin circuit

8.3.3 Small Load Current Indication

PG pin indicates the charging / EOC status in charging mode; but in discharging mode, it is used to indicate the output load status. When the IC detects output current is lower than a threshold I_{COM} (typical 50mA), it outputs high impedance at PG pin. When output current is detected higher than I_{COM}, the IC pulls PG pin to logic low internally.

This indication function can report load status to a system controller, like an MCU. For example, it can be used to detect the load device removal for adapter applications.

8.3.4 PWM/PFM Operation

The IC supports two operation modes in discharging mode: PWM mode and PFM mode. User can select the operation mode through MODE pin in discharging mode as below.

Table 3 Mode Selection (only in discharging mode)

MODE Input	Operation Mode
Logic low	PWM mode
Logic high	PFM mode
Float	PFM mode

In PWM mode, the IC always works with constant switching frequency for the whole load range. This helps achieve the best output voltage performance, but the efficiency is low at light load condition because of the high switching loss.

In PFM mode, the IC still works with constant switching frequency under heavy load condition, but under light load condition, it changes to pulse frequency modulation operation to reduce the switching loss. The efficiency can be improved under light load condition while output voltage ripple will be a little larger compared with PWM operation. Below figure shows the output voltage behavior of PFM mode.

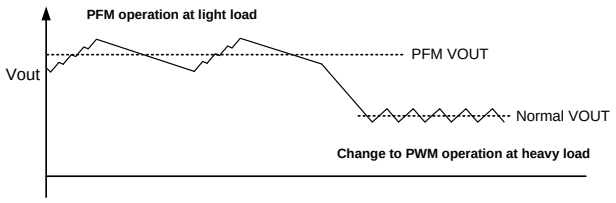


Figure 5 PFM operation

One way to balance the output ripple and efficiency is to tie MODE pin and PG pin together. In this way, the PFM mode is only enabled after the small load current condition is detected.

8.4 Current Limit

The IC integrates two current sense amplifiers to sense IBUS and IBAT respectively. With external current sense resistor(s), it can provide IBUS / IBAT current limit functions for both charging and discharging modes.

The IC monitors the voltage drop across the current sense resistor through the amplifier, and once the detected current exceeds the set limit value, the IC reduces the switching duty cycle to regulate the current at the set limit. The IPWM signal can also adjust the IBUS current limit in discharging mode dynamically. Please refer to 8.2.2 CC Charge (Constant Current Charge) and 8.2.7 Real-Time Charge Current Control for current limit setting details.

IBUS current limit must be set for charging mode operation. IBAT current limit is provided just for applications where battery current limit is required. If IBAT limit is not required, user can remove the IBAT current sense resistor and short ILIM2 pin to ground to disable the IBAT limit function.

See the requirements for RILIMx and duty cycle of IPWM signal in Application section.

8.5 Current Monitor

With the external current sense resistor at VBUS / VBAT, the ILIM1/ILIM2 pin's voltage is proportional to IBUS / IBAT current, so the user can monitor the current through ILIM1 / ILIM2 pin as below:

$$IBUS = \frac{VLIM1}{RILIM1} \times \frac{1000\ \Omega}{RSNS1}$$

$$IBAT = \frac{VLIM2}{RILIM2} \times \frac{1000\ \Omega}{RSNS2}$$

Where:

V_{LIM1} is the voltage on ILIM1 pin; V_{LIM2} is the voltage at ILIM2 pin

R_{SNS1} is the current sense resistor to sense IBUS current;

R_{SNS2} is the current sense resistor to sense IBAT current.

To get a better voltage sense, a RC circuit as below is recommended to filter the voltage ripple on ILIM1/2 pins. If the RC filter is not added, the MCU itself should implement digital filter.

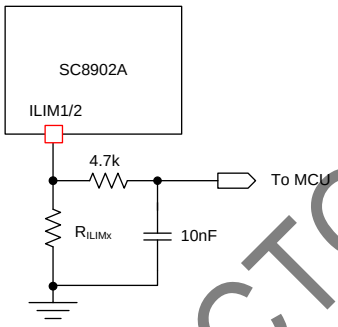


Figure 6 ILIMx pin voltage monitor circuit

8.6 Switching Frequency

The switching frequency is fixed at 460kHz for both charging mode and discharging.

8.7 VCC Driver Voltage

The IC integrates a VCC regulator so to generate the driver voltage for internal driver circuit. The VCC is supplied by the higher voltage of VBUS and VBAT, and is clamped to 5V. Connect a 1 μF ceramic capacitor from VCC to PGND pin close to the IC.

8.8 Loop Compensation

The internal control loop should be compensated by the resistor and capacitor connected at COMP pin. 15 kΩ resistor and 15 nF capacitor are suggested for most applications. If faster response is required, the user can increase the resistor value but should keep R*C value unchanged. After changing the compensation, check and make sure the loop is stable under target conditions.

8.9 DP/DM Handshaking

The IC supports automatic DP/DM handshaking. Once VBUS is detected in charging mode, the IC initiates the handshaking process at DP / DM lines and requests 9V charging voltage from the adapter.

8.10 Protections

8.10.1 Over Voltage Protection

The IC supports three mechanisms for over voltage protection.

The first is once the IC detects the VBUS or VBAT voltage is higher than typical 22V, the IC stops switching until the voltage drops below the threshold.

The second is once the IC detects the VBUS voltage is higher than the setting target by typical 10% in discharging mode, the IC stops switching until the voltage drops below

the threshold. This over voltage is still valid with dynamic voltage change function. For example, if the user sets the output voltage to 5V through VPMW signal, the IC can still stop switching once the VOUT is higher than 5.5V.

The third is once the IC detects the VBAT voltage is higher than the battery target voltage by 10%, the IC stops switching no matter in charging mode or discharging mode. The IC resumes switching when VBAT voltage recovers.

8.10.2 Over Current Protection

The IC implements internal current limit at 10A. Once the IC detects the inductor current is higher than 10A, it reduces the switching duty cycle, and keeps the inductor current from increasing.

8.10.3 Short Circuit Protection

The IC supports FB pin short circuit protection in discharging mode. During power on, the IC monitors the FB pin status. Once it detects the FB pin is short to ground, it still starts up and limits the VBUS voltage at 5V fixed voltage. This helps protect the circuits connected at VBUS pin from over voltage stress.

Besides FB short circuit protection, the IC also monitors the VBUS voltage all the time. Once it detects the VBUS voltage drops below short circuit protection threshold, typical 0.7V, the IC reduces the IBUS and IBAT current limits to 1/10 of the original setting.

8.10.4 Over Temperature Protection

Once the IC detects the chip junction temperature exceeds the threshold (160°C typical), the IC goes into thermal shutdown and stops switching. When the junction temperature falls below typical 145°C, the IC resumes operation.

9 Application Information

9.1 Input and Output Capacitor Selection

Since MLCC ceramic capacitor has good high frequency filtering and low ESR, X5R or X7R capacitors are recommended for input and output capacitors. Typically, three 22 μF ceramic input capacitors and three 22 μF ceramic output capacitors work for most applications. The input / output capacitors should be places as close to VBUSP / VBATP pins as possible, and they should be also near the PGND pins or thermal pad.

Capacitors' derating effect under DC bias should be taken into account when selecting the capacitors. Ceramic capacitor normally loses its most capacitance at the rated voltage, so leave margin on voltage rating to ensure adequate effective capacitance. For example, if the highest operating voltage is 12V, select 16V or 25V capacitor.

Besides this, high value electrolytic capacitor or tantalum capacitor is recommended to place in parallel with the ceramic capacitors at output to improve the load transient response.

9.2 Inductor Selection

Because the selection of inductor affects the loop stability and the power efficiency, inductor is one of the most important components for the DCDC design.

The IC can work with inductors between 2.2 μH to 10 μH range for most applications. A higher value is suggested to keep the inductor current ripple ≤ 30% of the DC current.

Compared with high value inductor in the same package size, a lower value inductor normally has smaller DC resistance (DCR), so can reduce the conduction power loss, which can be calculated roughly as

$$PL\_DC = IL^2 \cdot DCR$$

IL is the average value of inductor current, and it equals to IBUS or IBAT.

However, besides DCR, the core loss or AC loss of an inductor also affects the power efficiency a lot. The low value inductor causes large inductor current ripple, thus high core loss or AC loss, so it is not always the low value inductor supports the higher efficiency.

Since the core loss is related to the inductor material type, and normally the inductor vendors don't provide the core loss data, it is very difficult to suggest what inductor value can result in higher efficiency. As a rule of thumb, high value inductor like 4.7 μH to 10 μH is recommended for applications where the difference between input voltage and output voltage is big, such as 5V to 20V; while for those applications where input voltage is close to output voltage but large current is on power path, low value inductor like 2.2 μH is suggested.

For applications where efficiency or thermal dissipation is very important, it is highly suggested that the user chooses the inductor in larger package size for lower DCR, and also tests the efficiency with different inductor values, so to find the best combination to achieve the highest efficiency.

The saturation current is another important parameter when selecting the inductor. The inductance can decrease 20% to 35% when the current approaches saturation level, so the user should make sure the saturation current is higher than the inductor peak current during the operation.

The inductor peak current can be calculated by below formula.

$$IL\_peak = IBAT + \frac{VBAT \cdot (VBUS - VBAT \cdot \eta)}{2 \cdot fsw \cdot L \cdot VBUS} \quad (VBUS \geq VBAT)$$

$$IL\_peak = IBUS + \frac{VBUS \cdot (VBAT - VBUS)}{2 \cdot fsw \cdot L \cdot VBAT \cdot \eta} \quad (VBUS < VBAT)$$

where IBAT is the battery current at VBAT side, and can be calculated as

$$IBAT = \frac{VBUS \cdot IBUS}{\eta \cdot VBAT}$$

η is the power conversion efficiency. User can use 90% for calculation.

fsw is the switching frequency

L is the inductor value

The peak inductor current in charging mode can be calculated as

$$IL\_peak = IBAT + \frac{VBAT \cdot (VBUS - VBAT)}{2 \cdot fsw \cdot L \cdot VBUS \cdot \eta} \quad (VBUS > VBAT)$$

$$IL\_peak = IBUS + \frac{VBUS \cdot (VBAT - VBUS \cdot \eta)}{2 \cdot fsw \cdot L \cdot VBAT} \quad (VBUS \leq VBAT)$$

where IBAT is the battery charging current at VBAT side, and can be calculated as

$$IBAT = \frac{VBUS \cdot IBUS \cdot \eta}{VBAT}$$

η is the power conversion efficiency. User can use 90% for calculation.

fsw is the switching frequency

L is the inductor value

When selecting inductor, the inductor saturation current must be higher than the peak inductor current with enough margin (20% margin is recommended). The rating current of the inductor must be higher than the battery current.

9.3 Current Sense Resistor

The RSNS1 and RSNS2 in the typical application circuit are current sense resistors for current limit / monitor functions. The IC can work well without the RSNS2 resistor, so the user can remove it if the IBAT limit and monitor functions are not needed.

If the RSNS2 current sense resistor is not used, the user should tie the sense input pins VBAT_SP and VBAT_SN

together and connect them to VBATP pins.

A high resistor value can result in high current limit / monitor accuracy but causes high conductor loss. Typically 10 mΩ is recommended. But for applications where efficiency is more important than accuracy, lower value is suggested.

When selecting the current sense resistor, its power rating and temperature coefficient should also be considered.

The power dissipation can be roughly calculated as $P=I^2R$, where I is the highest current flowing through it. The power rating should be higher than the calculated value.

The resistor value varies with temperature and the variation is decided by its temperature coefficient. If high accuracy of limit or monitor is required, select as lower temperature coefficient as possible.

9.4 RILIMx and IPWM Duty Requirement

It is not allowed to set any of the current limits to 0A. Keep the minimum current limit above 0.3A.

In order to keep a normal operation, the value of RILIMx/D_{IPWM} shall also satisfy below requirements at different operation modes.

	RILIM1/IPWM Duty	RILIM2
Charging mode	≤63kΩ	≤48kΩ
During startup of discharging mode	≤48kΩ	≤25kΩ

9.5 Snubber Circuit and Driver Resistor

The RC snubber circuits at SWx nodes as shown below can be used to suppress the switching spike so to improve the EMC performance. A typical snubber circuit is composed by a 2.2Ω resistor and 1nF capacitor. The user can reduce the resistance and increase the capacitance further to improve the EMC. However, because it often causes higher switching loss and results in lower efficiency, it is suggested not to add snubber circuits unless necessary.

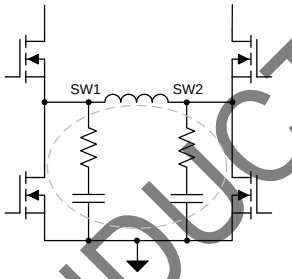


Figure 7 Snubber circuit at SWx nodes

The IC also allows user adding a driver resistor for the low side MOSFET at VBUS side to slow down the switching, thus to reduce the switching spike improve the EMC performance. However, because the driver resistor also causes higher switching loss and thus lower efficiency, it is suggested not to add the driver resistor unless necessary.

If the driver resistor is needed, a 0603 resistor should be used, and it should be placed near the IC.

10 Layout Guide

For switching power supplies, the layout is an important step. If the layout is not carefully designed, the converter may suffer instability and noise issues.

1. The VBUS bulk capacitors should be placed close to VBUSP and PGND pins, and the connection traces should be as short as possible. Put a 100nF capacitor parallel with the bulk capacitors to absorb high frequency noise. Since the trace will carry high current, wide copper are suggested. Similarly, the VBAT bulk capacitors should be placed close to VBATP and PGND pins, and keep the trace as wide and short as possible. It is suggested to put the input and output capacitors on the contrary layer to the IC, so the trace to PGND pad can be in the shortest way. Place sufficient vias to connect VBUSP or VBATP pins to the capacitors. User can refer to below layout as an example.

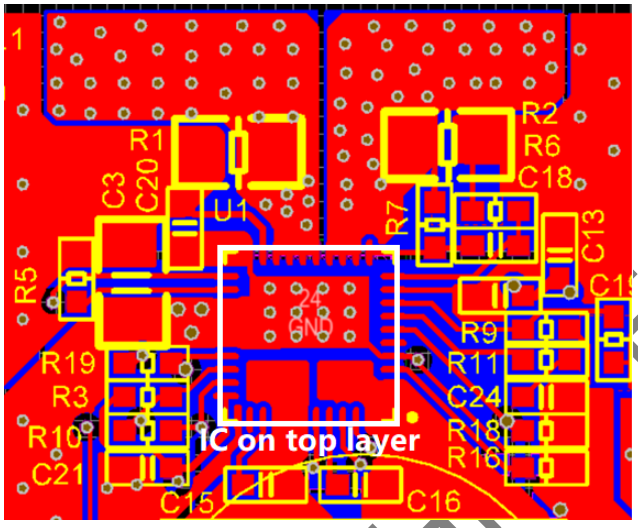


Figure 8 IC on top layer

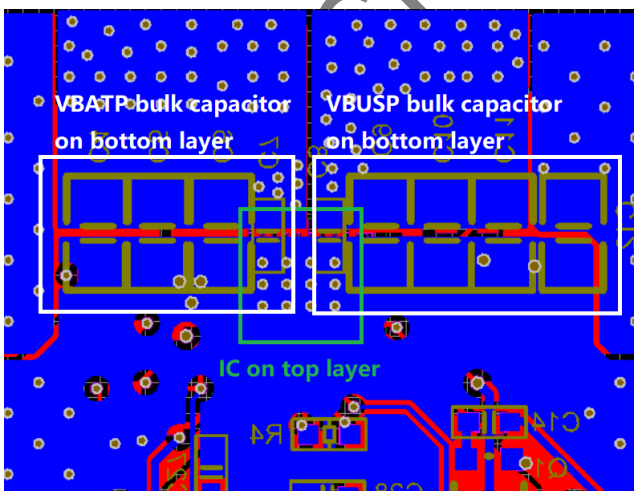


Figure 9 Bulk capacitors on bottom layer

2. Put the 1 μF bypass capacitor at VCC / VBAT_SN / VBUS pins as close to the IC as possible. The ground trace of the capacitor to PGND pins should be as short as possible.

3. Put the inductor close to the SW1 and SW2 pins. Keep the SW1 and SW2 traces wide because they carry high current during operation. Connect SW1 pins to the SW1 thermal pad under IC, and connect SW2 pins to the SW2 thermal pad.

4. Put the boot strap capacitors between BTx and SWx pins and the driving resistor between LG and LD1 pins close to the IC.

5. If current sense resistor is used for current sense or limit function, how to connect the sensing trace to the sense resistor is very important for the accuracy. It is required to route as below: the sensing trace should be routed to the pads of the sense resistor instead of the copper trace. Bad connection way will introduce sense error.

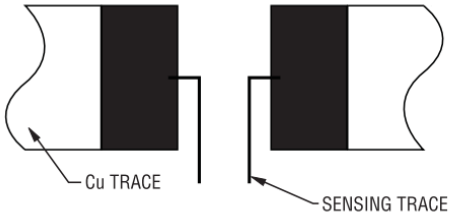


Figure 10 Sensing trace connection for current sense resistor

6. If it is for VBUS current sense, differential resistors and capacitor close to the sense pins as below is needed to suppress the switching noise. The sense traces should be routed in differential way.

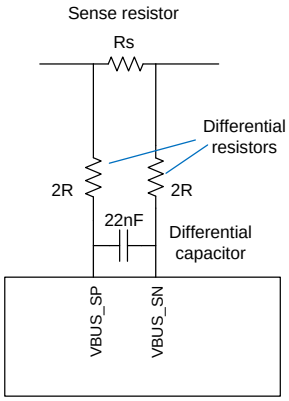


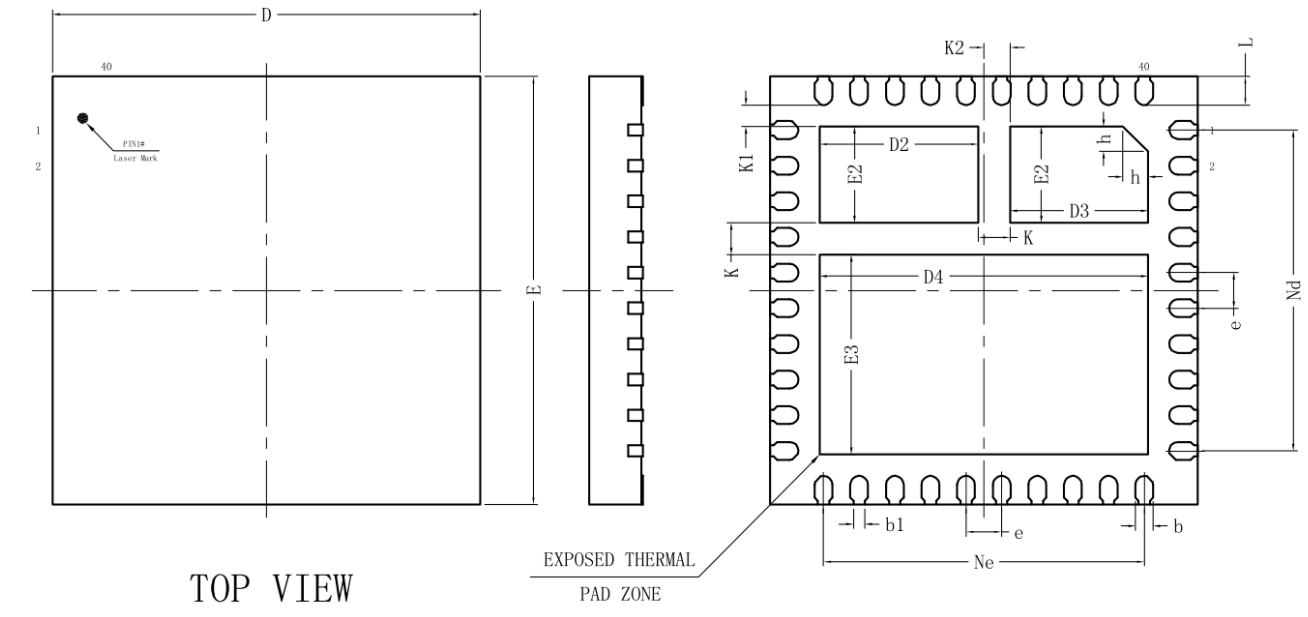
Figure 11 Differential sense

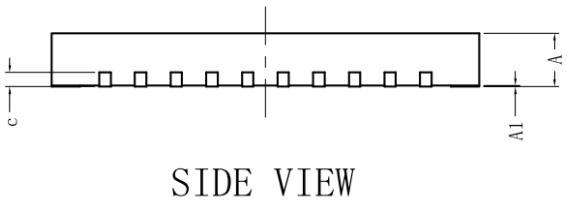
However, the differential resistors are not allowed for battery current sense because there is operation current into VBAT_SN pin and the differential resistor will lead to wrong sense.

7. The FB resistor divider, ILIMx resistor and COMP components should be put close to the IC.
8. Separate the analog ground from power ground to avoid switching noise. The ground of the analog components like FB resistor, ILIMx resistor, COMP components should be connect together, and the ground of the power components like the input/output bulk capacitor should be connect together. Then tie the analog ground and power ground at a single point, like at the ground thermal pad.
9. It is suggested to have a ground layer in the middle of PCB so the power ground can be complete. If only two layers are used, other signal traces should not block the ground return, and the power ground should be kept as wide and complete as possible

MECHANICAL DATA

QFN40L(6x6x0.75)





SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.20	0.25	0.30
b1	0.16REF		
c	0.18	0.20	0.25
D	5.90	6.00	6.10
D2	2.12	2.22	2.32
D3	1.83	1.93	2.03
D4	4.50	4.60	4.70
e	0.50BSC		
Ne	4.50BSC		
Nd	4.50BSC		
E	5.90	6.00	6.10
E2	1.25	1.35	1.45
E3	2.70	2.80	2.90
L	0.35	0.40	0.45
h	0.30	0.35	0.40
K	0.40	0.45	0.50
K1	0.25	0.30	0.35
K2	0.32	0.37	0.42