# High Efficiency, Synchronous 100V/1.2A Buck Converter with Low Quiescent Current

## 1 Descriptions

SC8171 is a synchronous buck converter with a wide input voltage range from 5V to 100V. With integrated both high-side and low-side power MOSFETs, the converter can achieve high efficiency without an external rectifier diode and can support up to 1.2A continuous load current. With sleep mode, pulse skips mode, and low quiescent current during standby or light load, the device can further prolong battery life and is suitable for battery-powered applications.

The device adopts a constant on-time control mode that provides fast transient response and eases loop stabilization. It supports low equivalent series resistance output capacitors such as ceramic (MLCC) and specialty polymer capacitors without an external compensation circuit. The switching frequency can be programmed easily by an external resistor.

SC8171 integrates internal VCC bias supply to save external VCC capacitor. An open-drain PG indicator provides sequencing, fault indication, and output voltage monitoring.

SC8171 supports protections including input under-voltage protection, cycle-by-cycle peak/ valley current limitation, short circuit protection with hiccup mode, and thermal shutdown protection with auto-recovery

SC8171 is available in SOIC8EP Package.

## 2 Features

- Wide VIN Range: 5 V to 100V
- Up to 1.2A Continuous Output Current Capability
- 115uA Low Quiescent Current
- Adaptive Sleep Mode
- Integrate 500mΩ/240mΩ MOSFET
- High-Efficiency Buck Conversion
- On-time Extention During Dropout Mode
- COT Mode for Fast Load Transient
- Few External Components
- Up to 1MHz Adjustable Switching Frequency
- EN control and Programmable UVLO
- ±1% Feedback Voltage Accuracy
- Power Good Indicator
- Internal Soft Start
- Cycle-by-cycle Over Current Protection
- Output Short Circuit Protection with Hiccup
- Input Under Voltage Protection
- Thermal Shutdown Protection
- Compact SOIC8E package

## 3 Applications

- High Voltage Post Regulator
- E-Bikes, Power and Garden Tools
- Motor Drivers, Drones, Telecom
- Industry Power Supplies

## 4 Device Information

| Part Number | Package | Dimension |
|---|---|---|
| SC8171SDER | ESOP8L | 4.90mm x 3.90mm |

## 5 Typical Application Circuit

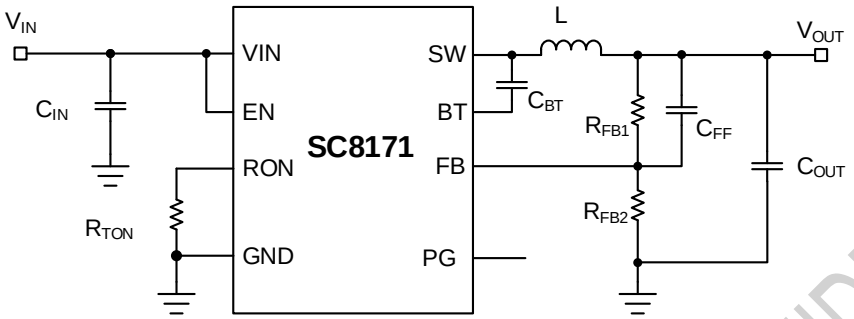
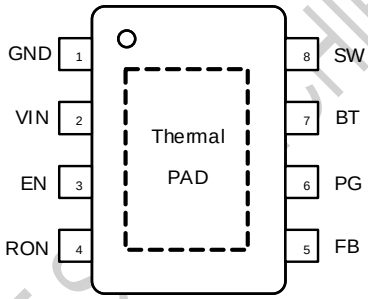



Figure. 1 Typical application circuit

## 6 Terminal Configuration and Functions

**Top View**




| TERMINAL | | I/O | DESCRIPTION |
|---|---|---|---|
| NUMBER | NAME | | |
| 1 | GND | PWR | Ground. Solder to thermal pad and connect to a large copper plane to reduce thermal resistance. |
| 2 | VIN | PWR | The power input node of the converter. |
| 3 | EN | I | Enable logic input. Logic high level enables the device and logic low level disables the device. |
| 4 | RON | I | Connect a resistor from this pin to GND to set the ON-time of high-side MOS |
| 5 | FB | I | Feedback node of VOUT output voltage. Set the VOUT output voltage by the external resistor divider connected at this pin |
| 6 | PG | O | An open-drain power-good indicator. Connect to a voltage source with an external pull-up resistor. |
| 7 | BT | PWR | Connect a 100nF X7R ceramic capacitor between BT pin and SW pin to provide the boosted bias voltage for high side gate driver. |
| 8 | SW | PWR | Switching Node. Connect to the switch node of the power inductor. |

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

| | | MIN | MAX | Unit |
|---|---|---|---|---|
| Voltage range at terminals(2) | VIN,SW | -0.3 | 100 | V |
| | EN | -0.3V | VIN+0.3 | V |
| | SW for less than 10ns | -3 | 120 | V |
| | FB, RON | -0.3 | 6 | V |
| | BT to SW | -0.3 | 6 | V |
| | PG | -0.3 | 14 | V |
| $T_J$ | Operating junction temperature range | -40 | 150 | °C |
| $T_{stg}$ | Storage temperature range | -65 | 150 | °C |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

## 6.2 Thermal Information(TBD)

| THERMAL RESISTANCE(1) | | SOIC8EP | UNIT |
|---|---|---|---|
| $\theta_{JA}$ | Junction to ambient thermal resistance | TBD | °C/W |
| $\theta_{JC}$ | Junction to case resistance | TBD | °C/W |

(1) Measured on JESD51-7, 4-layer PCB.

## 6.3 Handling Ratings

| PARAMETER | DEFINITION | MIN | MAX | UNIT |
|---|---|---|---|---|
| ESD(1) | Human body model (HBM) ESD stress voltage(2) | TBD | TBD | kV |
| | Charged device model (CDM) ESD stress voltage(3) | TBD | TBD | V |

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.4 Recommended Operating Conditions

| | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{IN}$ | VIN voltage range | 5 | | 100 | V |
| $I_{OUT}$ | Output Current range | | | 1.2 | A |
| $F_{SW}$ | Switching frequcency | 100 | | 1000 | KHz |
| $C_{BT}$ | Bootstrap capacitor for high-side MOS driver | | 100 | | nF |

# 7 Electrical Characteristics

$T_J$= 25°C and VIN =24V, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SUPPLY VOLTAGE** | | | | | | |
| $V_{IN}$ | Operating voltage | | 5 | | 100 | V |
| $V_{UVLO}$ | VIN under-voltage lockout threshold | Rising edge | | 4.2 | | V |
| | | Hysteresis | | 300 | | mV |
| $I_Q$ | Quiescent current in sleep mode | EN = H, VFB=2V | | 47 | | μA |
| | Quiescent current in active mode | EN = H, no switching | | 115 | | μA |
| $I_{SHUTDOWN}$ | Shutdown current VIN | EN = L | | 2 | | μA |
| **EN LOGIC AND SOFT START** | | | | | | |
| $V_{EN\_R}$ | EN threshold | EN rising | | 1.2 | | V |
| $V_{EN\_F}$ | EN threshold | EN falling | | 1.1 | | V |
| $t_{SS}$ | Internal soft-start time | | | 3 | | ms |
| **FEEDBACK** | | | | | | |
| $V_{FB}$ | Feedback reference voltage | VFB falling | | 1.2 | | V |
| **DIRVER AND POWER SWITCH** | | | | | | |
| $V_{BT\_UVLO}$ | High-side MOS driver UVLO | $V_{BT\_SW}$ rising | | 2.3 | | V |
| $R_{DSON}$ | High side MOS Q1 on resistance | | | 500 | | mΩ |
| | Low side MOS Q2 on resistance | | | 240 | | mΩ |
| **SWITCHING TIMER** | | | | | | |
| $F_{SW\_RANGE}$ | Switching frequency range | | 100 | | 1000 | KHz |
| $T_{ON0}$ | Typical on time | $V_{IN}$=6V, $R_{RT}$=75K | | 5000 | | ns |
| | | $V_{IN}$ =12V, $R_{RT}$=75K | | 2550 | | ns |
| $T_{ON\_MIN}$ | | | | 80 | | ns |
| **PG INDICATOR** | | | | | | |
| $V_{PG\_R}$ | FB rising for PG high to low | FB rising | | 1.14 | | V |
| $V_{PG\_F}$ | FB falling for PG low to high | FB falling | | 1.08 | | V |
| $R_{PG10}$ | PG pull down resistance | | | 30 | | Ω |
| **INTERNAL CURRENT LIMIT** | | | | | | |
| $I_{PEAK\text{-}1A}$ | Peak current limit threshold | | | TBD | | A |
| $I_{VALLEY\text{-}1A}$ | Valley current limit threshold | | | TBD | | A |
| **THERMAL SHUTDOWN** | | | | | | |
| $T_{SD}$ | Thermal shutdown temperature (1) | | | 150 | | °C |
| | Thermal shutdown hysteresis (1) | | | 15 | | °C |

# 8 Functional Block Diagram

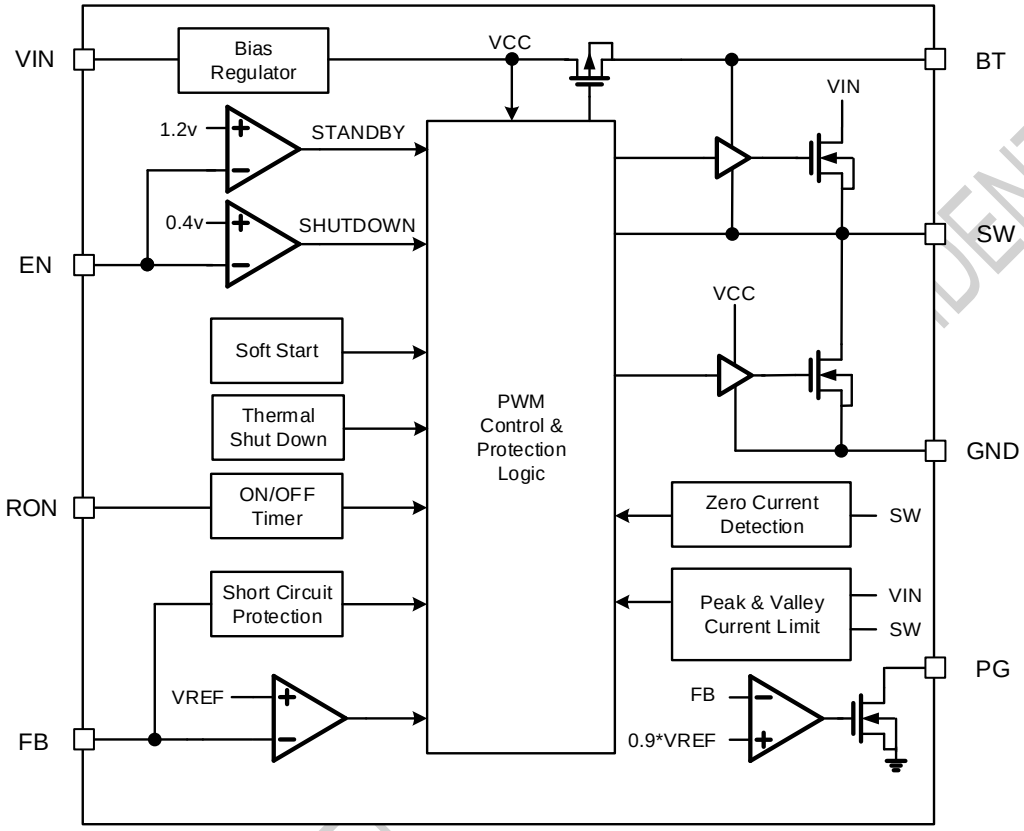



Figure.1 Functional Block Diagram

# 9 Feature Description

## 9.1 Enable and Programmable UVLO

The SC8171 has an enable control pin EN: pulling it high enables the IC and pulling it low disables the IC. Connect EN to VIN for automatic startup.

EN pin can also be reused for VIN under-voltage protection. Connecting the center tap of the divider resistors between VIN and GND programs the VIN under-voltage threshold and restart voltage, as shown in Figure. 2

The VIN under-voltage threshold can be calculated as the following equation.

$$V_{IN\_LOW} = 1.1\text{V} \times \left(1 + \frac{R_{IN1}}{R_{IN2}}\right)$$

When the input voltage is higher than the startup threshold, the device goes back to normal operation.

$$V_{IN\_HIGH} = 1.2\text{V} \times \left(1 + \frac{R_{IN1}}{R_{IN2}}\right)$$

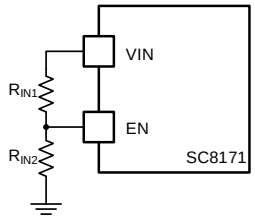



Figure.2 UVLO Threshold Programming

Connect EN pin to VIN or resistor network without floating. The EN pin voltage should never be higher than VIN + 0.3 V. It is not recommended to apply EN voltage when VIN is 0 V.

## 9.2 Internal VCC Regulator

The IC implements an internal VCC regulator which is powered from VIN without requiring an external capacitor to stabilize the linear regulator. The internal regulator powers the internal blocks including the MOSFET driver and logic circuits. The bootstrap capacitor which is connected between the BT pin and SW pin is also charged through the internal VCC regulator during the SW voltage is low enough. A typical capacitance of 100nF X7R ceramic bootstrap capacitor with a higher than 6.3V voltage rating is recommended.

## 9.3 Soft Start

The IC implements a soft start feature to prevent inrush current during startup. After the IC is enabled, it ramps up the internal reference voltage is around 3ms. The output voltage follows the reference, so it starts up slowly.

## 9.4 Sleep Mode

To improve standby and light load efficiency, the device adopts a sleep mode to reduce power consumption.

As the frequency of operation decreases and VFB remains above 1.2 V (VREF) with the output capacitor sourcing the load current for greater than 15μs, the converter enters a low IQ sleep mode to prevent draining the input power supply. The FB comparator and internal bias rail are active to detect when the FB voltage drops below the internal reference VREF and the converter transitions out of sleep mode into active mode. There is a 9μs wake-up delay from sleep to active states.

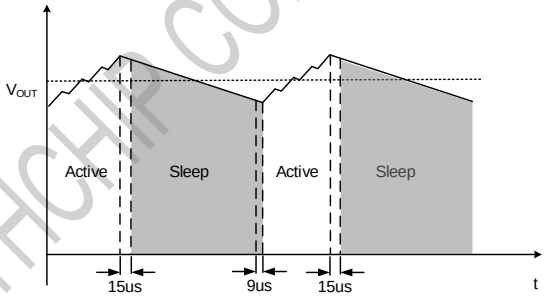



Figure.4 Sleep mode operation

## 9.5 Switching Frequency

The SC8171 adopts constant on-time mode control providing fast transient response and nearly constant frequency. The switching frequency of the device can be set from 100kHz to 1MHz through an external resistor at the $R_{ON}$ pin to GND.

The constant on-time can be calculated as:

$$t_{ON}(\mu s) = \frac{R_{ON}\ (k\Omega)}{2.5 \times V_{IN}(V)}$$

The switching frequency is estimated as the following equations by using a proper $R_{ON}$.

$$R_{ON}(k\Omega) = \frac{2500 \times V_{OUT}\ (V)}{f_{SW}(kHz)}$$

The minimum on-time of SC8171 is limited at 80ns and using the right $R_{ON}$ to set the on-time for proper operation.

## 9.6 Output Voltage Setting

The output voltage can be configured for customized values by using external feedback resistors and can be calculated as below.

$$V_{OUT} = V_{FB\_REF} \times (1.2 + \frac{R_{UP}}{R_{DOWN}})$$

Where:

$V_{FB\_REF}$ is the internal reference voltage 1.2V, $R_{UP}$ and $R_{DOWN}$ are the resistors connected from VOUT to FB and AGND. Use 1% tolerance or better resistors and keep the feedback resistors close to the FB pin.

## 9.7 Power Good

The device has an open-drain power good output to indicate whether the output voltage operates within appropriate levels. The PG is set to high impedance when the output voltage reaches 95% of its nominal value and stays there until the FB voltage falls below 90% of the nominal value. An external pull-up resistor of typical resistance from 10kΩ to 100kΩ is required to connect the PG pin to an external voltage under 12V. The output delay of the PG comparator is about 10μs to prevent false triggers.

The PG pin can be left floating if unused.

## 9.8 Protections

### 9.8.1 Input Under Voltage Lock Out

SC8171 features an input under-voltage lockout (UVLO) function to stops the operation of the converter when the input voltage drops below the typical UVLO threshold of 3.9V. The IC resumes normal operation when the rising voltage at the VIN pin is 300mV above the UVLO threshold.

### 9.8.2 Peak Current Limitation

SC8171 supports cycle by cycle current limit on both high side and low side MOSFET and prevents the device from high currents such as overload, output short circuit, or inductor saturation. If the high side current limit occurs, the high side MOSFET turns off and the low side MOSFET turns on to prevent the inductor current from running away. When the inductor current drops down to the low side current limit, the low side MOSFET turns off and the high side MOSFET turns on again.

To prevent this function false triggers by switching noise, a minimum on-time of 80ns is adopted, the actual inductor current may exceed the high side current limit threshold because of this feature.

### 9.8.3 Output Short Circuit Protection

The device integrates a hiccup mode which is triggered once the voltage of the FB pin is lower than 0.5V. In hiccup mode, SC8171 periodically stops switching for 40ms and then tries to restart with a soft start. If the short condition still exists in 5ms during the hiccup-on cycle, the device will stop switching again. This protection mode is especially useful when the output is dead-shorted to the ground. The average short-circuit current is greatly reduced to alleviate the thermal issue and to protect the converter. Once the short-circuit condition is removed, SC8171 exits hiccup mode and goes back to normal operation.

### 9.8.4 Over Temperature Protection

Once the IC detects the chip junction temperature exceeds the threshold of 150 °C, the IC goes into thermal shutdown and stops switching. When the junction temperature falls below the typical 135°C, the IC resumes operation.

# 10 Application Information

## 10.1 Input and Output Capacitor Selection

The input current of the Buck converter is discontinuous and the input capacitor should be carefully selected. At least 2.2μF with sufficient voltage rating capacitor is required for small input voltage ripple and stability. The input capacitor close to IC's VIN pin and GND must be a high-quality X7S or X7R ceramic capacitor.

To avoid an input hot-swapping spike, another low ESR aluminum electrolytic or polymer capacitor is recommended to suppress the input voltage spike.

The input voltage ripple caused by the capacitance can be calculated by:

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})$$

Since ceramic capacitors have low ESR and good high-frequency filtering, the X7S or X7R ceramic capacitor is recommended for best ripple performance across temperature and input voltage variations. The output voltage ripple is estimated as the following equation:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \times (1 - \frac{V_{OUT}}{V_{IN}})$$

Based on the voltage coefficient of ceramic, it normally loses its most capacitance at the rated voltage, so leave margin on voltage rating to ensure adequate effective capacitance. For example, if the highest operating voltage is 12V, select a 25V capacitor. Larger capacitors cause lower output voltage ripple and higher load transient performance.

## 10.2 Inductor Selection

The inductor selection is a tradeoff between size, cost, efficiency, and transient response performance. The key parameters of an inductor are inductance, DC resistance, and saturation current.

Generally, the inductor current ripple estimated at 30% of the maximum output current is a related good choice to compromise size and loss. The switching frequency, input voltage, output voltage, and output ripple determine the inductor value:

$$\mathrm{L} = \frac{V_{OUT}}{\Delta I_L \times f_{SW}} \times (1 - \frac{V_{OUT}}{V_{IN}})$$

The inductor DC resistance value (DCR) affects the conduction loss of the switching regulator, so a smaller DCR is recommended for the first selection. If the current is relatively small, a higher DCR inductor with larger inductance can be selected. The inductor saturation current $I_{SAT}$ should be higher than the input/output current with sufficient margin.

$$I_{SAT} \geq 0.5\Delta I_L + I_{OUT\_MAX}$$

## 10.3 PCB Layout Guide

For best performance, the PCB layout should be carefully designed to avoid instability, switching noise interference, and EMI issues. Minimizing the area of alternating current and voltage loops in the layout helps reduce EMI. For a BUCK converter, the critical loop area is showed in figure 5:

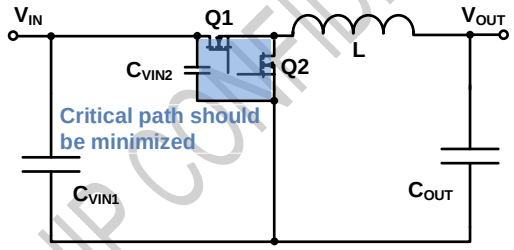



Figure.5 Minimizing the critical path helps mitigate EMI

Here show some guidelines for reference:

1) The input capacitor ($C_{VIN2}$, MLCC) should be close to IC to minimize the critical path area and make sure the current flows through the $C_{VIN}$ first, then the VIN pin. The PCB trace should be wide and short.

2) The Bootstrap capacitor (100nF) should be close to the BT pin and SW pin to avoid noise and instability.

4) The FB feedback resistor should be close to the FB pin and be away from the switching node. A reserved feed-forward capacitor in parallel with the upper resistor of the FB node is recommended to improve stability and transient performance if needed.

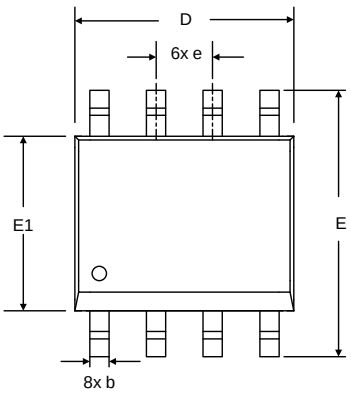
5) The RON pin is also sensitive to noise. The RON resistor should be close to the RON pin and be away from the switching node. The parasitic capacitance from RON to GND must not exceed 20pF.

6) The RC snubber is connected between SW and PGND to absorb switching noise. The snubber should be close to SW and GND pin and minimize the loop area to optimize EMI.

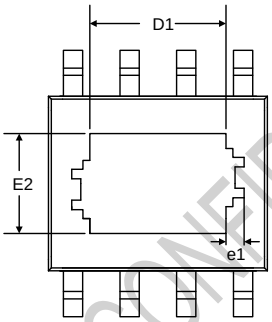
7) The GND pin must be connected to the exposed pad of SC8171. Use a ground plane in one of the middle layers as a noise shielding and to a heat-sinking PCB ground plane. Connect the exposed pad to the PCB ground plane with an array of heat-sink vias.

# MECHANICAL DATA

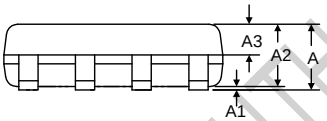
ESOP8L (4.9mm x 3.90mm)



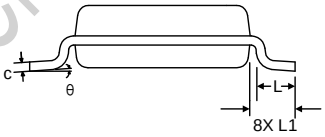

TOP VIEW




BOTTOM VIEW




SIDE VIEW




SIDE VIEW

| Symbol | Millimeter | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | - | - | 1.65 |
| A1 | 0.05 | - | 0.15 |
| A2 | 1.30 | 1.40 | 1.50 |
| A3 | 0.60 | 0.65 | 0.70 |
| b | 0.39 | - | 0.47 |
| c | 0.20 | - | 0.24 |
| D | 4.80 | 4.90 | 5.00 |
| E | 5.80 | 6.00 | 6.20 |
| E1 | 3.80 | 3.90 | 4.00 |
| e | 1.27BSC | | |
| L | 0.50 | 0.60 | 0.80 |
| L1 | 1.05REF | | |
| θ | 0 | - | 8° |

| L/F size (mil) | Size (mm) | | |
|---|---|---|---|
| | D1 | E2 | e1 |
| 95*130 | 3.10REF | 2.21REF | 0.10REF |