

SC8949 High Efficiency, Synchronous, Bi-directional Buck Charger Converter with Integrated MOSFETs and I2C Interface

1 Description

SC8949 is a synchronous buck charger with reverse boost discharging function. It integrates two N-channel MOSFETs with ultra-low $R_{ds(on)}$ and can support 5V high efficiency charging and discharging operation.

In charging mode, it steps down the input voltage to effectively charge the single cell battery. SC8949 supports trickle charging, constant current (CC) charging and constant voltage (CV) charging management functions automatically. When working in discharging mode (reverse boost mode), it can support 5V output and achieve up to 93% efficiency with 3V battery voltage for 5V4A output load.

The SC8949 features I2C interface, so the user can easily control the charging/discharging mode, and program the charging current, charging voltage, output voltage, and output current limits through I2C. It also monitors the VBUS status of up to three USB ports and provides three NMOS gate drivers to control the power path independently.

The IC also provides IMON pin, through which the MCU can monitor the VBUS / VBAT voltage, IBUS / IBAT current and the current of each port in real time. The NTC function guarantees the battery operation safety. All these features help simplify the system design and reduce the BOM.

The SC8949 supports under voltage protection, over voltage protection, over current protection, short circuit protection and over temperature protections to ensure safety under different abnormal conditions.

SC8949 adopts 32 pin 4mm x 4mm QFN package.

3 Applications

- Power Bank
- Li-Ion Battery Charger
- Fast Charge
- Smart USB Sockets

2 Features

- Charging management, including trickle charging, CC charging, CV charging and charging termination function
- 5V VBUS voltage operation
- Programmable battery voltage from 4.1V to 4.5V
- Integrated MOSFET with ultra-low $R_{ds(on)}$
- Support 3V VBAT to 5V4A output with 93% efficiency
- Programmable VINREG voltage
- Programmable current limit with 25mA/step
- Programmable output voltage with 10mV/step
- Programmable cable drop compensation
- Insert detection for up to three USB ports
- Integrate N-Gate drivers for up to three USB ports
- Voltage and current monitor through IMON pin
- Supports pass-through operation
- Charging status indication
- Support NTC function
- Under voltage protection and over voltage protection
- Over current protection, short circuit indication and thermal shutdown protection
- QFN-32 4x4 package

4 Device Information

ORDER NUMBER	PACKAGE	BODY SIZE
SC8949QFER	32 pin QFN	4.0mm x 4.0mm x 0.75mm

5 Typical Application Circuit

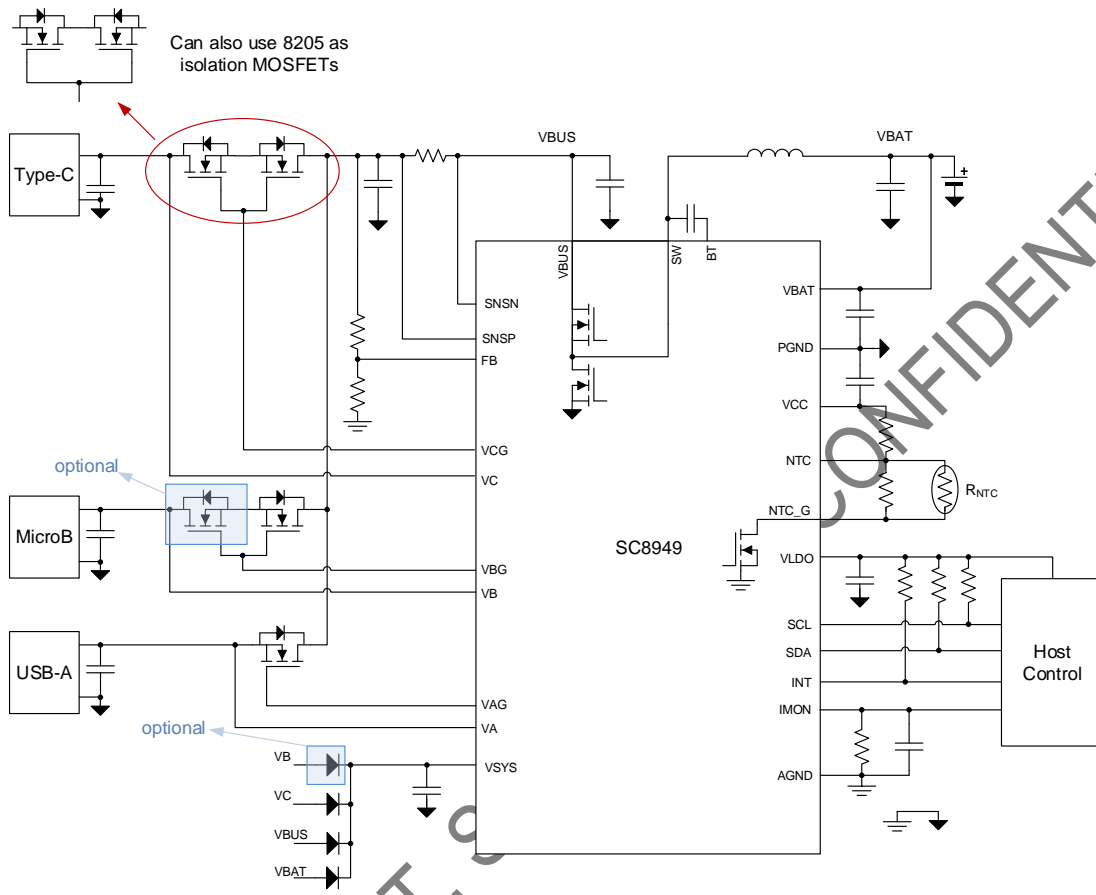
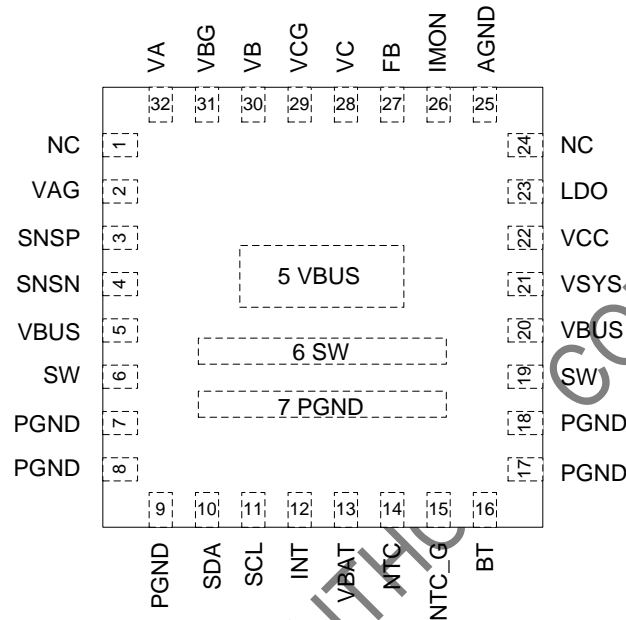


Figure 1 Typical Application Circuit

6 Terminal Configuration and Functions

TOP VIEW



TERMINAL		I/O	DESCRIPTION
NUMBER	NAME		
1, 24	NC		NC pin. Leave it floating
2	VAG	O	NMOS gate driver to control the external NMOS of VA port. Controlled by VAG_ON bit
3	SNSP	I	Positive input of a current sense amplifier. Connect to one pad of the 10 mΩ current sense resistor to sense the current into or out from VBUS.
4	SNSN	I	Negative input of a current sense amplifier. Connect to one pad of the 10 mΩ current sense resistor to sense the current into or out from VBUS.
5, 20	VBUS	IO	Power node of the buck charger.
6, 19	SW	IO	Switching Node. Connect to the inductor.
7-9, 17-18	PGND	IO	Power ground. Connect PGND and AGND together at a single point close to the IC.
10	SDA	IO	I2C data line. Connect with a pull up resistor (typical 4.7 kΩ).
11	SCL	I	I2C clock line. Connect with a pull up resistor (typical 4.7 kΩ).

12	INT	O	Open drain output for interrupt signal.
13	VBAT	I	Supply current to the IC and also sense the battery voltage. Connect to the battery positive node. Place a 1 μ F capacitor from this pin to AGND as close to the IC as possible.
14	NTC	I	Connect to the Negative Temperature Coefficient (NTC) thermistor to sense the battery cell temperature for protection.
15	NTC_G	O	Open drain output. It disconnects the NTC resistor from ground in idle mode automatically to save power.
16	BT	I	Bootstrap a bias voltage for high side MOSFET driver. Connect a 100nF capacitor between BT pin and SW pin.
21	VSYS	I	Power supply to the IC. Connect to power rails with diodes. Place a 1 μ F capacitor from this pin to PGND as close to the IC as possible.
22	VCC	O	Output of internal 5V linear regulator. Connect a 1 μ F capacitor from VCC pin to PGND as close to the IC as possible.
23	LDO	O	Output of internal linear regulator. The output voltage can be set to 3.3V or 2.8V through register.
25	AGND	IO	Analog ground. Connect PGND and AGND together at a single point close to the IC.
26	IMON	O	Used to monitor VBUS / VBAT voltage, IBUS / IBAT current, and the voltage drop of isolation MOS for VA / VB / VC ports
27	FB	I	Feedback node of VBUS voltage for external VBUS setting.
28	VC	I	Used to sense the VBUS status of the VC port. Connect a 1 μ F capacitor between VC and GND close to the USB port
29	VCG	O	NMOS gate driver to control the external NMOS of VC port. Controlled by VCG_ON bit.
30	VB	I	Used to sense the VBUS status of the VB port. Connect a 1 μ F capacitor between VB and GND close to the USB port
31	VBG	O	NMOS gate driver to control the external NMOS of VB port. Controlled by VBG_ON bit.
32	VA	I	Used to sense the VBUS status of the VA port. Connect a 1 μ F capacitor between VA and GND close to the USB port

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
Voltage range at terminals ⁽²⁾	VA, VB, VC, VBUS, VSYS, SNSP, SNSN	-0.3	9	V
	SW	-3	9	V
	BT to SW	-0.3	6.5	V
	VAG, VBG, VCG	-0.3	14	V
	FB, IMON, VCC, LDO, NTC, NTC_G, VBAT, INT, SCL, SDA	-0.3	6.5	V
T _J	Operating junction temperature range	-40	150	°C
T _{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.

7.2 Thermal Information

THERMAL RESISTANCE ⁽¹⁾		QFN-32 (4mmX4mm)	UNIT
θ _{JA}	Junction to ambient thermal resistance	45	°C/W
θ _{JC}	Junction to case resistance	9	°C/W

- (1) Measured on JESD51-7, 4-layer PCB.

7.3 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
ESD ⁽¹⁾	Human body model (HBM) ESD stress voltage ⁽²⁾	-2	2	kV
	Charged device model (CDM) ESD stress voltage ⁽³⁾	-750	750	V

- (1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.
- (2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.4 Recommended Operating Conditions

		MIN	TYP	MAX	UNIT
V _{BUS}	VBUS voltage range –internal setting for discharging mode	5		6	V
	VBUS voltage range – external setting for discharging mode	4.5		6	V
	VBUS voltage range – for charging mode	4.4		6	V
V _{BAT}	VBAT voltage range	2.6		4.5	V

C _{BUS}	Bulk capacitor for VBUS (effective value)	30			μF
C _{BAT}	Bulk capacitor for VBAT (effective value)	30			μF
L	Inductance	1.5	2.2	3.3	μH
R _{SNS}	Current sense resistor	10		10	mΩ
T _A	Operating ambient temperature	-40		85	°C
T _J	Operating junction temperature	-40		125	°C

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7.5 Electrical Characteristics

T_J = 25°C and V_{BUS} = 5V, V_{BAT} = 3.6V unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
V _{UVLO_VBUS}	VBUS under-voltage lockout threshold	Rising edge	2.4	2.5	2.7	V
		Hysteresis		180		mV
V _{UVLO_VBAT}	VBAT under-voltage lockout threshold	Discharging mode, Rising edge		2.47	2.6	V
		Hysteresis		220		mV
I _{Q_VSYS}	Quiescent current into VSYS	VSYS > VBAT; IDLE = 0, non-switching, NTC and FB resistor dividers' bias current not included		0.12	0.2	mA
I _{Q_VBAT}	Quiescent current into VBAT			5	10	μA
I _{SB_VBAT}	Standby current into VBAT	VSYS open, IDLE = 1		40	70	μA
		VSYS > VBAT, IDLE = 1		3	20	μA
I _{SB_VSYS}	Standby current into VSYS	VSYS = 5V, IDLE = 1		70	120	μA
VCC AND LDO						
V _{CC}	VCC regulation voltage	ICC = 1~70mA IDLE = 0/1	4.9	5.1	5.35	V
I _{VCC_LIM}	VCC regulator current limit	VSYS = VCC + 1V, IDLE = 0/1	70	100	130	mA
		VCC = 0V		30		mA
V _{CC_DROP}	VCC dropout voltage	VSYS = 5V, ICC = 70mA		360	440	mV
V _{LDO}	LDO regulation voltage	LDO set to 3.3V, ILDO = 1~50mA	3.23	3.30	3.37	V
		LDO set to 2.8V, ILDO = 1~50mA	2.73	2.80	2.87	V
V _{LDO_DROP}	LDO dropout voltage	ILDO = 50mA, VBAT = 2.7V	440	500	640	mV
SWITCHING AND POWER SWITCH						
F _{SW}	Switching frequency	FSW_SET = 00	220	300	380	kHz
		FSW_SET = 01	340	450	560	kHz
		FSW_SET = 10	450	600	750	kHz
		FSW_SET = 11	550	735	930	kHz
R _{dson_HS}	On resistance of high side MOS		11		mΩ	
R _{dson_LS}	On resistance of low side MOS		8.5		mΩ	
VOLTAGE AND CURRENT IN CHARGING MODE						
V _{BAT_ACC}	Battery voltage regulation accuracy	VBAT_SET = 000, 4.1V target	4.059	4.08	4.1	V
		VBAT_SET = 001, 4.2V target	4.158	4.18	4.2	V
		VBAT_SET = 010, 4.25V target	4.208	4.23	4.25	V
		VBAT_SET = 011, 4.3V target	4.257	4.28	4.3	V
		VBAT_SET = 100, 4.35V target	4.307	4.33	4.35	V
		VBAT_SET = 101, 4.4V target	4.356	4.38	4.4	V
		VBAT_SET = 110, 4.45V target	4.406	4.43	4.45	V

		VBAT_SET = 111, 4.5V target	4.455	4.48	4.5	V
V _{INREG_ACC}	VINREG voltage regulation accuracy	VINREG_SET = 000, 4.4V target	4.268	4.42	4.54	V
		VINREG_SET = 001, 4.5V target	4.365	4.52	4.64	V
		VINREG_SET = 010, 4.6V target	4.462	4.63	4.74	V
		VINREG_SET = 011, 4.7V target	4.559	4.73	4.85	V
		VINREG_SET = 100, 4.8V target	4.656	4.83	4.95	V
		VINREG_SET = 101, 4.9V target	4.753	4.93	5.05	V
V _{TRKL}	Trickle charge voltage threshold, over VBAT target	Rising edge	64%	66%	68%	
		Hysteresis		4%		
I _{BAT_TRKL}	Trickle charge current, measured at IBAT	ITRKL_SET = 0	130	260	390	mA
		ITRKL_SET = 1	400	540	680	mA
V _{EOC}	End of charge voltage threshold, over VBAT target		98%	99%	100%	
I _{TERM}	End of charger current threshold, measured at IBAT	ITERM_SET = 00	20	135	240	mA
		ITERM_SET = 01	90	200	300	mA
		ITERM_SET = 10	190	300	400	mA
		ITERM_SET = 11	290	400	500	mA
t _{EOC_deg}	EOC detection deglitch time		4			s
V _{RECH}	Recharge threshold	RECH_SET = 0	96.0%	97.6%	98.8%	
		RECH_SET = 1	95.0%	96.4%	97.8%	
CURRENT LIMIT						
I _{BUS_LIM}	IBUS current limit accuracy	IBUS_LIM set to 3A, DIR = 0/1	-5%		5%	
		IBUS_LIM set to 2A, DIR = 0/1	-5%		5%	
		IBUS_LIM set to 0.5A, DIR = 0/1	-20%		20%	
I _{BUS_MIN}	Minimum IBUS current limit clamping value accuracy	Min_IBUS_clamp_setting = 00	50	125	200	mA
		Min_IBUS_clamp_setting = 01	120	200	280	mA
		Min_IBUS_clamp_setting = 10	170	250	330	mA
		Min_IBUS_clamp_setting = 11	220	300	380	mA
I _{BAT_LIM}	IBAT current limit accuracy ⁽¹⁾	IBAT_LIM = 00, DIR = 0	3.6	3.9	4.3	A
		IBAT_LIM = 01, DIR = 0	5.5	5.7	6.0	A
		IBAT_LIM = 10, DIR = 0	7	7.6	8.3	A
		IBAT_LIM = 11, DIR = 0	8.8	9.5	10.5	A
		IBAT_LIM = 00, DIR = 1	5.2	5.7	6.3	A
		IBAT_LIM = 01, DIR = 1	7	7.6	8.3	A
		IBAT_LIM = 10, DIR = 1	8.8	9.5	10.5	A
		IBAT_LIM = 11, DIR = 1	10.2	11.4	12.6	A

VOLTAGE IN DISCHARGING MODE						
V _{FB_REF}	Reference voltage at FB pin	FB_SEL = 1	1.176	1.2	1.224	V
I _{FB_BIAS}	Bias current into FB pin	FB_SEL = 1, FB in regulation			50	nA
V _{BUS}	VBUS output voltage accuracy	FB_SEL = 0, VBUS set to 5V	4.9	5	5.1	V
R _{COMP_SET}	Cable compensation ratio	CBLCOMP_CTRL = 01, 100kΩ pull up resistor of FB pin if FB_SET=1, R _{SNS} = 10mΩ	37	50	63	mV/A
		CBLCOMP_CTRL = 10, 100kΩ pull up resistor of FB pin if FB_SET=1, R _{SNS} = 10mΩ	75	100	125	mV/A
		CBLCOMP_CTRL = 11, 100kΩ pull up resistor of FB pin if FB_SET=1, R _{SNS} = 10mΩ	112	150	188	mV/A
V _{COMP_clamp}	Cable compensation clamping voltage	CBLCOMP_CTRL = 01, 100kΩ pull up resistor of FB pin if FB_SET=1, R _{SNS} = 10mΩ	140	170	200	mV
		CBLCOMP_CTRL = 10, 100kΩ pull up resistor of FB pin if FB_SET=1, R _{SNS} = 10mΩ	283	340	397	mV
		CBLCOMP_CTRL = 11, 100kΩ pull up resistor of FB pin if FB_SET=1, R _{SNS} = 10mΩ	425	510	595	mV
POWER PATH MANAGEMENT						
R _{PU}	Pull up resistance for VAG/VBG/VC GATE driver			60		kΩ
R _{PD}	Pull down resistance for VAG/VBG/VC GATE driver			2.5		kΩ
R _{DIS_VBUS}	Discharging path from VBUS to PGND	VBUS_DISPATH = 1		1		kΩ
R _{DIS_VC}	Discharging path from VC to PGND	VC_DISPATH = 1		1		kΩ
DETECTION AND IMON MONITOR						
V _{IN_ACOK}	Input power good threshold	Rising, for VB or VC as charging port	4.3	4.4	4.5	V
		Hysteresis		250		mV
V _{INDET}	Phone detection threshold	For VA or VB as discharging port	1.9	2	2.1	V
I _{COM}	Small current detection threshold for IBUS	Falling edge	10	50	80	mA
		Hysteresis		50		mA
V _{IMON}	Suggested IMON output voltage range		0		2.8	V
K _{IMON_IBUS}	IBUS current sensing ratio	I _{IMON} / I _{IBUS} , R _{SNS} = 10 mΩ		5.47		μA/A
V _{IMON_IBUS_ACC U}	IBUS current monitor accuracy ⁽¹⁾	IBUS = 5A, R _{SNS} = 10 mΩ	-3.7%		3.7%	
		IBUS = 2A, R _{SNS} = 10 mΩ	-8%		8%	
K _{IMON_IBAT}	IBAT current sensing ratio	I _{IMON} / I _{IBAT} , R _{SNS} = 10 mΩ		4.31		μA/A

V _{IMON_IBAT_ACCU}	IBAT current monitor accuracy ⁽¹⁾	IBAT = 5A, R _{SNS} = 10 mΩ	-5%	5%		
		IBAT = 2A, R _{SNS} = 10 mΩ	-10%	10%		
K _{IMON_IPORT}	Port current sensing ratio	I _{IMON} / V _{DROP_X}	416.7		μA/V	
V _{IMON_IPORT_ACQU}	IPORT(Port A/B/C) current monitor accuracy ⁽¹⁾	I _{IPORT} * Ron _{Nx} = 100mV	-10%	10%		
		I _{IPORT} * Ron _{Nx} = 30mV	-25%	25%		
K _{IMON_VBAT}	VBAT voltage sensing ratio	I _{IMON} / V _{BAT}	10.06		μA/V	
V _{IMON_VBAT_ACCU}	VBAT voltage monitor accuracy	VBAT = 4V	-2%	2%		
K _{IMON_VBUS}	VBUS voltage sensing ratio	I _{IMON} / V _{BUS}	3.06		μA/V	
V _{IMON_VBUS_ACQU}	VBUS voltage monitor accuracy	VBUS = 5V ~12V	-4%	4%		
t _{IMON_POR}	Delay time for IMON pin to function after IC POR		200	250	ms	
t _{IMON_swth}	Establish time for IMON signal	10pF at IMON pin		50	μs	
PROTECTIONS						
V _{BAT_OVP}	Battery over voltage threshold, over VBAT target	Rising edge	103%			
		Hysteresis	2%			
R _{BAT_DISCH}	Discharging path resistance at VBAT		1		kΩ	
V _{BAT_DPL}	Battery depleted voltage	Rising edge	2.10	2.26	2.40	V
		Hysteresis	200			mV
I _{BAT_DPL}	Charging current to depleted battery		300		mA	
V _{FB_OVP}	FB over voltage threshold for external VBUS setting, measured over V _{FB_REF}	FB_SEL = 1, Rising edge	108%	110%	112%	
		FB_SEL = 1, Hysteresis	6%			
V _{BUS_OVP}	VBUS over voltage threshold for internal VBUS setting	FB_SEL = 0, Measured as V _{BUS_OVP} - V _{BUS_SET} Rising edge	0.4	0.5	0.6	V
		Hysteresis	0.3			V
V _{FB_SC}	FB short circuit protection threshold for external VBUS setting	Rising edge	90	110	130	mV
		Hysteresis	20			mV
V _{BUS_SC}	VBUS short circuit protection threshold, measured as VBAT - VBUS	Falling edge	10	160	300	mV
		Hysteresis	90			mV
V _{BUS_UVP}	VBUS under voltage threshold	VBUS_UVP_SET = 0 Falling edge	3.6	3.8	4.0	V
		Hysteresis	110			mV
		VBUS_UVP_SET = 1 Falling edge	4.3	4.4	4.6	V
		Hysteresis	170			mV

t_{HICCUP}	Hiccup time for short circuit protection		500		ms
NTC THRESHOLD					
$V_{\text{COLD_CH}}$	NTC cold threshold for charging mode, as percentage of VCC	Rising edge	75.6%	76.1%	76.6%
		Hysteresis	0.7%		
$V_{\text{COOL_CH}}$	NTC cool threshold for charging mode, as percentage of VCC	Rising edge	69.5%	70%	70.5%
		Hysteresis	1.3%		
$V_{\text{HOT_CH}}$	NTC hot threshold for charging mode, as percentage of VCC	Falling edge	41.2%	41.7%	42.2%
		Hysteresis	2.6%		
$V_{\text{COLD_DM}}$	NTC cold threshold for discharging mode, as percentage of VCC	Rising edge	86.1%	86.4%	87.1%
		Hysteresis	0.7%		
$V_{\text{HOT_DM}}$	NTC hot threshold for discharging mode, as percentage of VCC	Falling edge	30.7%	31.4%	31.7%
		Hysteresis	2.6%		
V_{DISNTC}	NTC disable threshold, as percentage of VCC	Falling edge	14.5%	15.0%	15.5%
		Hysteresis	10%		
$R_{\text{NTC_SW}}$	RON of NTC switch		25		Ω
I2C AND LOGIC CONTROL					
V_{IL}	SCL, SDA input low voltage			0.4	V
V_{IH}	SCL, SDA input high voltage		1.2		V
$I_{\text{SINK_SCL/SDA}}$	SCL/SDA pin sink current	$V_{\text{SCL/SDA}} = 0.4\text{V}$	40		mA
$I_{\text{SINK_INT}}$	INT pin sink current	$V_{\text{INT}} = 0.4\text{V}$	10	25	35
t_{PULINT}	Interrupt pulse width (logic low)		0.7	1	1.3
SOFTSTART					
$t_{\text{delay_CH}}$	Delay time for charging	VBUS = 5V, from PSTOP low to IC starting charging	8		ms
t_{SS}	Soft-start time for discharging	VBUS from VBAT to 5V in discharging mode, VBAT = 3.7V, CVBUS=100 μ F	250		μ s
THERMAL SHUTDOWN					
T_{SD}	Thermal shutdown temperature	Rising	165		$^{\circ}\text{C}$
		Hysteresis	15		$^{\circ}\text{C}$

Note: (1) layout sensitive. Refer to Layout Guide or demo board PCB layout for good layout practice.

7.6 Typical Characteristics

The following diagrams show typical performance of SC8949.

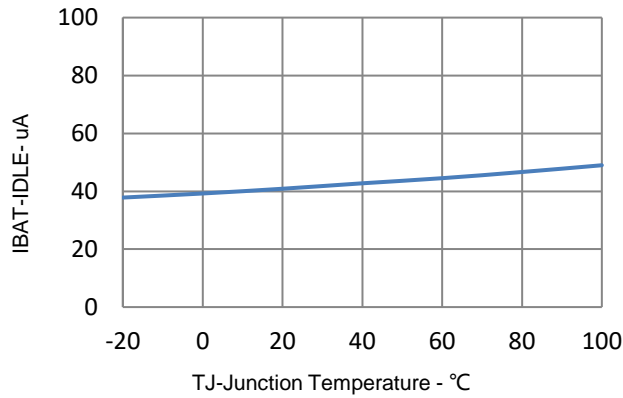


Figure 2 Sleep Mode Current VS Junction Temperature (VBAT=3.7V, Idle=1)

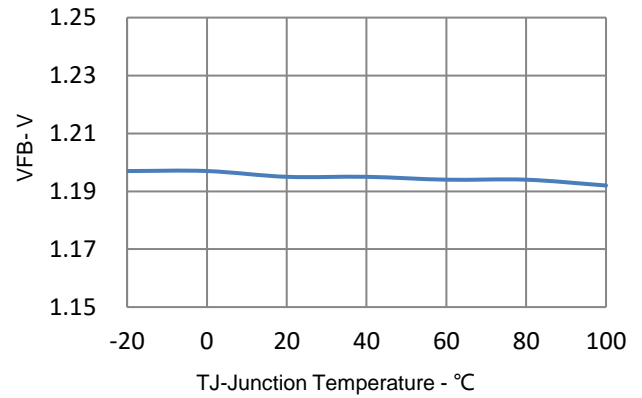


Figure 3 FB Reference voltage VS Junction Temperature in Discharging Mode (FB_SET=0)

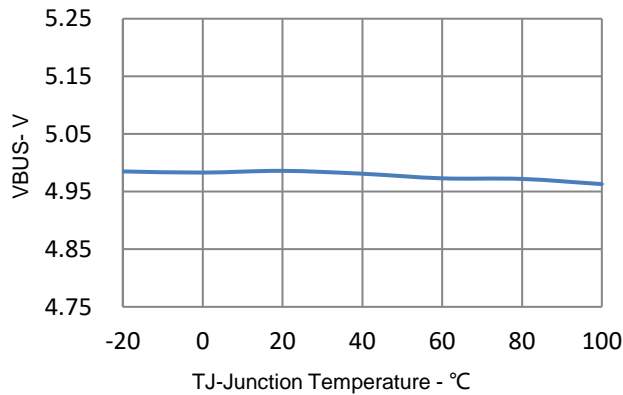


Figure 4 VBUS VS Junction Temperature in Discharging Mode (FB_SET=0, VBUS_SET=5V)

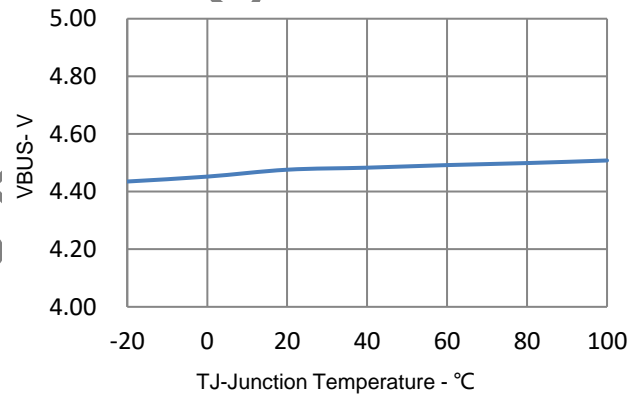


Figure 5 VinReg VS Junction Temperature in Charging Mode (VinReg_SET=4.5V)

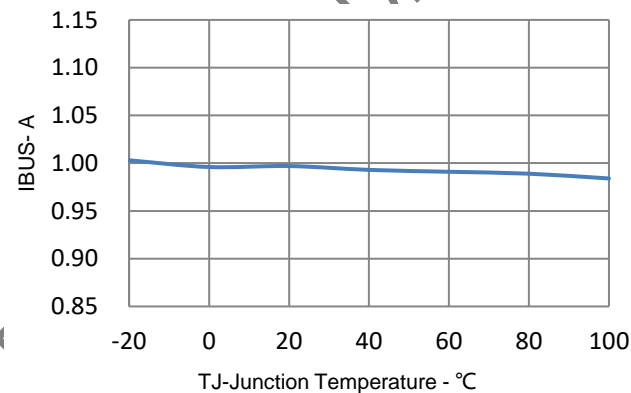


Figure 6 IBUS VS Junction Temperature in Discharging Mode (IBUS_SET=1A)

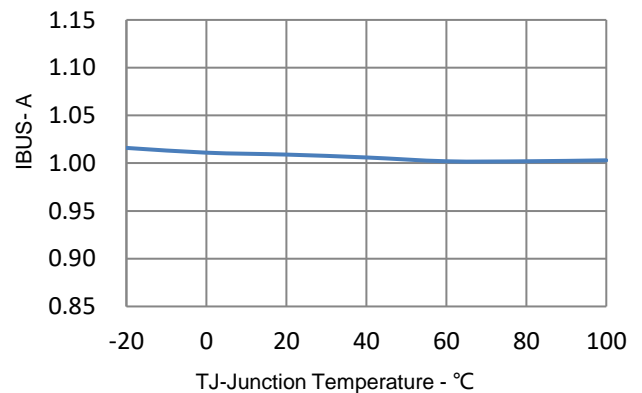


Figure 7 IBUS VS Junction Temperature in Charging Mode (IBUS_SET=1A)

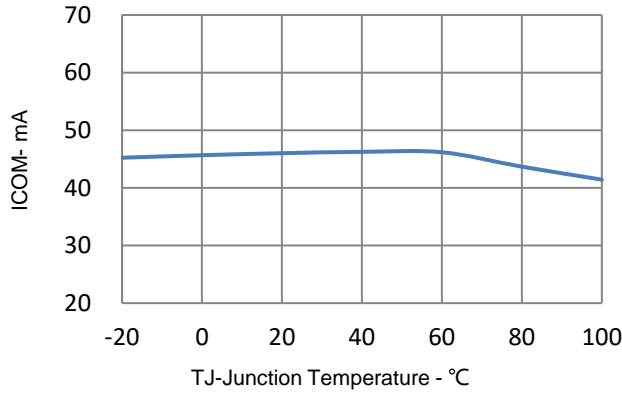


Figure 8 ICOM VS Junction Temperature

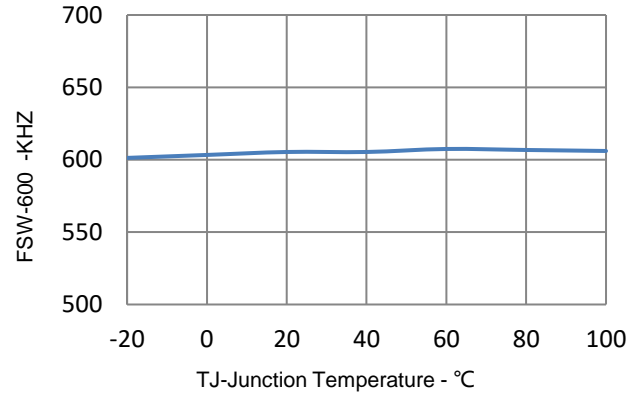


Figure 9 Switching Frequency VS Junction Temperature in Charging Mode

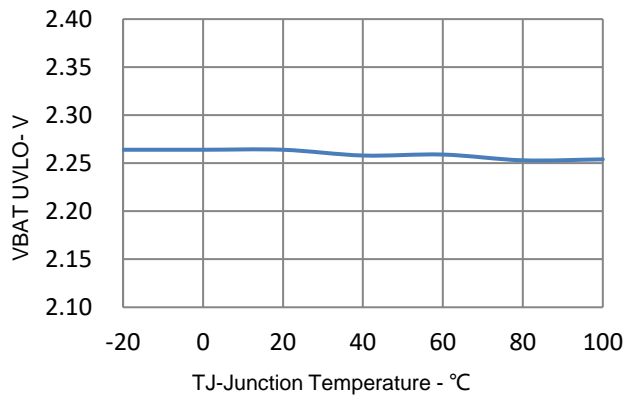


Figure 10 VBAT Under Voltage Lock Output VS Junction Temperature

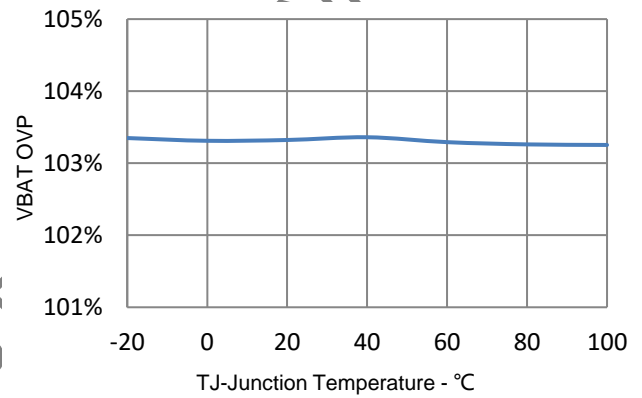


Figure 11 VBAT Over Voltage Protection VS Junction Temperature

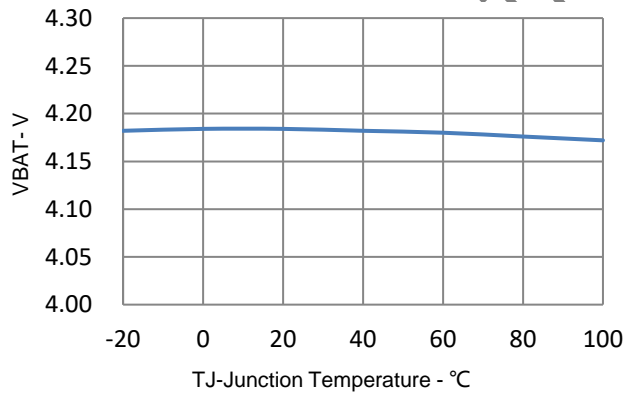
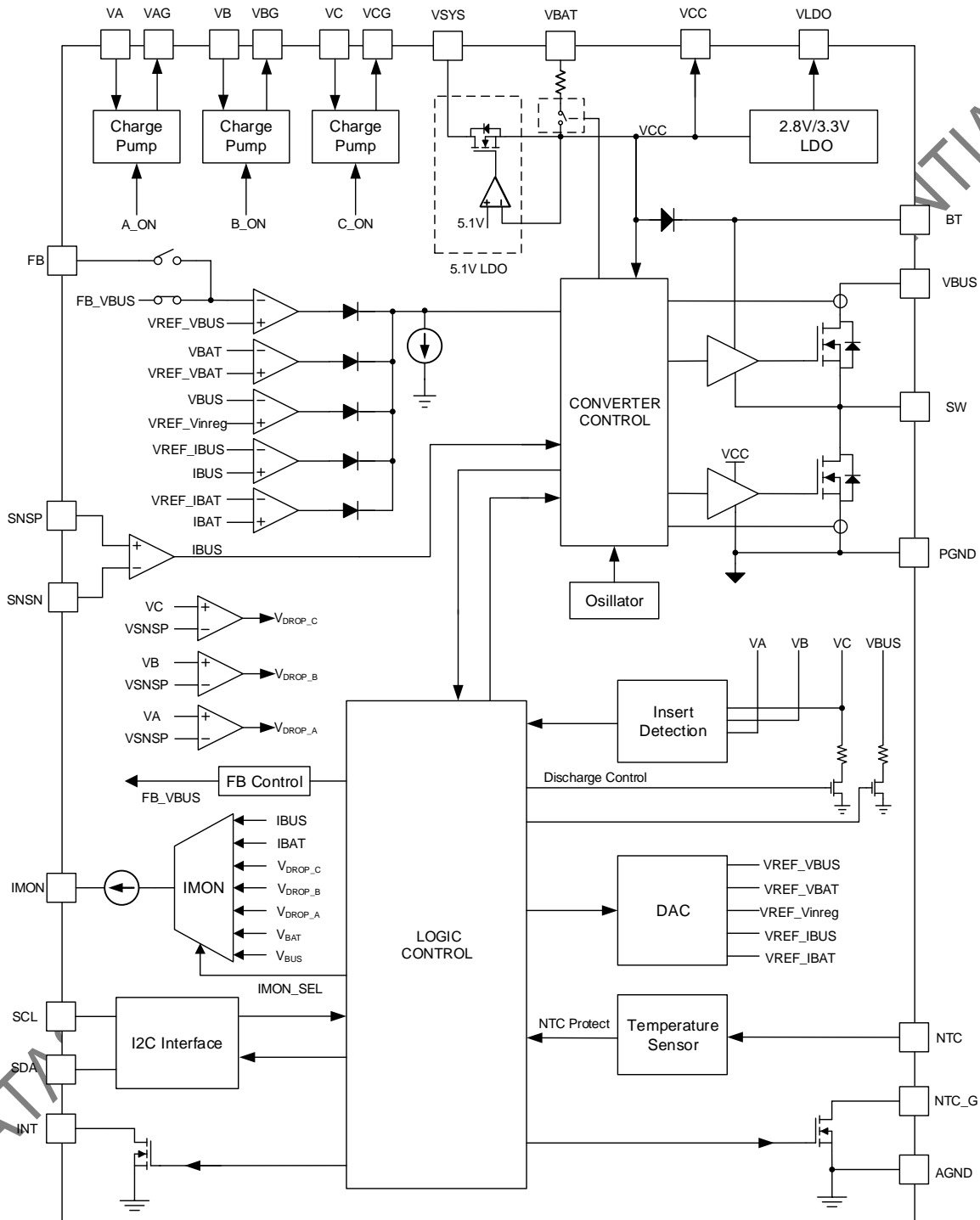


Figure 12 VBAT Termination Voltage VS Junction Temperature in Charging Mode, VBAT_SET=4.2V

8 Functional Block Diagram



Function Block Diagram

9 Detailed Description

The SC8949 is a high efficiency buck charger with integrated power switches of ultra-low $R_{ds(on)}$. It can charge a single cell battery with 5V input voltage in charging mode, and also support boost mode/discharging mode with 5V output voltage. The ultra-low $R_{ds(on)}$ allows SC8949 to achieve 93% efficiency from 3V battery to 5V 4A output.

9.1 Charging Mode

User can set the charging mode and discharging mode by DIR bit.

When DIR bit is set to 0, the IC is set in charging mode to charge the battery cells. The IC initiates charging operation when below conditions are satisfied:

If FORCE_CH = 0

1. DIR = 0
2. IDLE = 0
3. PSTOP = 0
4. At least one of the VB / VC port is configured as charging port, and the corresponding NGATE driver is turned on

If FORCE_CH = 1

1. DIR = 0
2. IDLE = 0
3. PSTOP = 0

When above conditions are satisfied, the IC initiates charging operation.

Note: during charging operation, if $V_{BUS} < V_{INREG_SET}[2:0]$, IC works in VINREG loop, and the charging current is 0. See details in 9.1.6 Self-adaptive Charging Current section.

In charging mode, the IC monitors the battery voltage through VBAT pin, and monitors the charging current through external current sense resistor (typ. 10 mΩ). The IC charges the battery cells according to below typical charging profile.

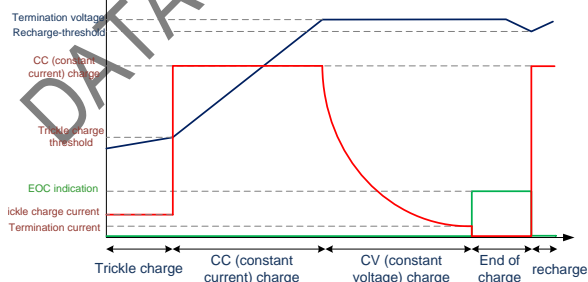


Figure 13 Typical Charging Profile

When battery voltage is below trickle charge threshold, the IC charges the cells with IBAT current set by ITRKL_SET bit; when VBAT is above the threshold, the IC enters into Constant Current charging phase with constant current set by IBUS_LIM[7:0] or IBAT_LIM[1:0]. When the cell voltage reaches the VBAT target, it enters into Constant Voltage charge phase, and charges the cells with gradually decreased current. Once termination voltage and termination current conditions are satisfied, the IC enters into End of Charge phase. In this phase the IC can either terminate the charging or keep charging the cells, depending on how user configures the IC.

9.1.1 Trickle Charge

The trickle charge voltage threshold is 65% (typ.) of the battery voltage target. When in trickle charge phase, the battery charging current IBAT is regulated to the value set by ITRKL_SET bit.

When in trickle charging phase, IBAT_Loop bit is set to 1 to indicate the battery current is under regulation.

If the battery voltage is depleted and lower than 2V (typ.), the IC charges the battery with 300mA (typ.) current.

9.1.2 CC Charge (Constant Current Charge)

When VBAT is higher than the trickle threshold, the IC charges the battery cells with constant current set by IBUS limit or IBAT limit. The current limit value can be changed dynamically. For any change of IBUS_LIM[7:0] to take effect, user shall write IBUS_LIM_Load bit to 1 to load the new setting.

The IC regulates the current which reaches the limit value first. For example, if IBUS current limit is set to 3A, IBAT limit is set to 10A, and when IBUS reaches 3A, IBAT is only 6A, the IC will regulate the IBUS at 3A.

In CC charging phase, IBAT_Loop bit or CC_Loop bit is set to 1 to indicate either IBAT or IBUS current is under regulation.

9.1.3 CV Charge (Constant Voltage Charge)

The VBAT target voltage is set by VBAT_SET[2:0]. When the battery voltage reaches 98% of the target voltage, the IC enters into CV charge phase. In this phase, the IC regulates the VBAT voltage, and charging current reduces gradually.

When in CV charging phase, CV_Loop bit is set to 1 to indicate the VBAT voltage is under regulation.

9.1.4 EOC (End of Charge)

When below conditions are satisfied, the IC enters into EOC phase, and set EOC bit to 1 to report the status.

1. the VBAT voltage is above 99% of VBAT target
2. the IBAT current is below ITERM_SET[1:0]
3. the IC is working in CV charge phase
4. above conditions are satisfied for more than 4sec

If DIS_TERM = 0, the IC stops switching to terminate the charging after EOC bit is set to 1; if DIS_TERM = 1, the IC keeps switching and regulating the battery cell voltage at the target value after EOC.

9.1.5 Recharge

If the IC terminates charging after EOC, the battery voltage may drop due to leakage or operation current from battery cells. Once the VBAT voltage drops below VRECH threshold, the EOC bit is cleared, and the IC enters into CC charge phase to recharge the battery. The SC8949 supports two VRECH thresholds, and can be set through RECH_SET bit.

9.1.6 Self-adaptive Charging Current

During charging, if the IBUS charging current is higher than adapter's current capability, the adapter will be overloaded and the VBUS voltage pulled low.

The IC supports dynamic power management. The allowed minimum VBUS operation voltage for charging is set by VINREG_SET [2:0]. Once VBUS voltage drops to VINREG threshold, the IC reduces the charging current automatically and regulates the VBUS at VINREG threshold. If the VBUS voltage drops below VINREG threshold, the IC reduces the charging current to 0.

VINREG_Loop bit is set to 1 to indicate the charger is under VINREG regulation.

Note: To avoid abnormal switching during battery charging, VINREG threshold which is set by VINREG_SET [2:0] should keep higher than battery voltage. User can set the a fixed VINREG threshold by VBAT_SET[2:0] or a dynamic VINREG threshold with the battery voltage change.

For example, when a 4.4V battery is used:

1. Set the VINREG threshold at 4.6V as a fixed value
2. Set the VINREG threshold at 4.5V if the battery voltage is lower than 4.2V; when the battery is fully charged and the battery voltage is higher than 4.25V, then set the VINREG threshold at 4.6V. The battery voltage can be monitored by the IMON function. See VBAT and VBUS Voltage Monitor for more details.

The following table shows recommend VINREG setting with the consideration of the VINREG and the IMON accuracy.

Table 1 Recommed VINREG configuration

VBAT	4.1V/4.2V	4.25V/4.3V	4.35V/4.4V	4.45V/4.5V
VINREG	≥4.4V	≥4.5V	≥4.6V	≥4.7V

9.2 Discharging Mode

When DIR bit is set to 1, the IC is set to discharging mode. The IC initiates the boost operation, and boosts the VBAT voltage to VBUS target when below conditions are satisfied:

1. DIR = 1
2. IDLE = 0
3. PSTOP = 0
4. VBAT > VBAT_UVLO

The IC supports two ways of regulating VBUS output:

- If FB_SEL is set to 0, internal feedback resistors are used, and the VBUS output is set by VBUS_SET[9:0]. The default output is 5V, and can be adjusted from 5V to 6V with 10mV per step as below:

$$VBUS (V) = 5V + 10mV \times (VBUS_SET[9:2] \times 4 + VBUS_SET[1:0])$$

User shall write VBUS_SET_Load bit to 1 to load the VBUS setting otherwise the change will not take effect.

- If FB_SEL is set to 1, the IC detects VBUS by external feedback resistors connected at FB pin, and regulates FB voltage at 1.2V. The output voltage can be set as below.

$$VBUS = VREF \times \left(1 + \frac{RUP}{RDOWN}\right)$$

Where, VREF is the reference voltage, which is fixed at 1.2V. RUP and RDOWN are the external resistors connected at FB pin.

User can leave FB pin floating if internal setting is configured. If external setting is set, keep VBUS_SET[9:0] at default values.

User shall make sure the VBUS output voltage is set below 6V. If a higher voltage is set, the IC may be damaged.

User shall keep the FB_SEL unchanged while the IC operates. Change is only allowed when PSTOP = 1 or IDLE = 1.

9.2.1 PFM Operation

To reduce the switching loss, the IC features Pulse-Frequency Modulation (PFM) operation under light load condition for discharging mode. The IC decreases the frequency automatically to reduce the switching loss so the efficiency can be improved under light load condition. Below figure shows the output voltage behavior of PFM mode.

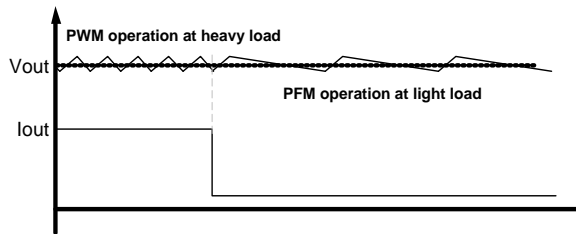


Figure 14 PFM mode illustration

9.2.2 Cable Drop Compensation

Due to the cable resistance, there is normally obvious voltage drop on the USB cable under heavy load condition, causing the voltage at the other end of the cable low. To compensate the voltage drop, the SC8949 features cable drop compensation function in discharging mode. The output voltage can increase along with the output current according to the relationship as below:

$$V_{BUS_COMP} = V_{BUS} + I_{BUS} * R_{COMP_SET}$$

where

V_{BUS_COMP} is the compensated output at V_{BUS} pin,

V_{BUS} is the original output setting,

I_{BUS} is the output current sensed by $SNSP$ and $SNSN$ pins,

R_{COMP_SET} is the compensation ratio set by $CBLCOMP_CTRL[1:0]$.

The compensation voltage ($I_{BUS} * R_{COMP_SET}$) is clamped at 140/320/500mV for 50/100/150mV/A setting respectively.

The cable drop compensation function is default disabled, and can be turned on and configured by $CBLCOM_CTRL[1:0]$. It is effective for both external and internal V_{BUS} setting ways. If external setting is used, R_{up} of the resistor divider shall be fixed to 100kΩ.

9.2.3 Current Limit in Discharging Mode

When DIR is set to 1, the IC monitors the discharging current

through the voltage drop from $SNSN$ pin to $SNSP$ pin (opposite direction of charging mode). $IBUS_LIM[7:0]$ and $IBAT_LIM[1:0]$ are still functional in discharging mode for over current protection. Once the current reaches the limit setting, the duty cycles is reduced so to regulate the current at the setting.

9.3 Port Configuration

The SC8949 integrates the port detection and control circuit for up to three USB ports: V_A , V_B and V_C .

For V_A port, it can only work as discharging port, and just the current from V_{BUS} to V_A is allowed. It supports phone insert detection function.

For V_B port, it can be configured as either charging port or discharging port.

- If $V_B_SET = 0$, it works as charging port: adapter insert and removal detection are supported, and the current shall flow from V_B to V_{BUS}
- if $V_B_SET = 1$, it works as discharging port: phone insert detection function is supported, and the current shall flow from V_{BUS} to V_B

For V_C port, it is normally used for DRP TYPE-C port.

- when $C_DIR = 0$, it works as charging port: adapter insert and removal detection are supported, and the current shall flow from V_C to V_{BUS}
- when $C_DIR = 1$, it works as discharging port: the current shall flow from V_{BUS} to V_C . However,
- V_C port is designed for TYPE-C port configuration, but it can also be configured as a Micro-B charging port with $C_DIR = 0$. V_C doesn't support phone insert detection function even with $C_DIR = 1$, so it cannot be configured as a USB-A discharging port.

Note: If V_C port works as charging port, the V_C discharging patch (V_C_DIS) should be always enabled to establish correct adapter insert and removal detection

To avoid false detection and reduce system level ESD stress, a 1 μF (typ.) MLCC is recommended between $V_A/V_B/V_C$ and GND close to the USB port respectively. If the port is configured as Micro-B port or Type-C port, it is highly recommended to put a 1 μF capacitor at USB port and another 1 μF capacitor close to the chip.

The supported configurations are summarized as below.

Table 2 Port Configuration

Pin	Direction Control Bit	Port Function	Current direction	Function		Can be configured as		
				Phone insert detection (INDET)	Adapter insert and removal detection (ACOK)	USB-A	Micro-B	TYPE-C
VA	NA	discharging	VBUS to VA	yes		yes		DFP
VB	VB_SET = 0	charging	VB to VBUS		yes		yes	UFP or DRP
	VB_SET = 1	discharging	VBUS to VB	yes		yes		DFP or DRP
VC	C_DIR = 0	charging	VC to VBUS		yes		yes	UFP or DRP
	C_DIR = 1	discharging	VBUS to VC					DFP or DRP

9.4 Power Path Management

The IC provides three NMOS gate drivers for VA / VB / VC ports respectively.

The NGATE driver must be combined with corresponding port, that is, VAG can only be used for VA, VBG only for VB, and VCG only for VC.

When the driver is turned on, its VGS (from gate to VBUS) is equal to VCC. When it is turned off, the gate is pulled to ground. +7V clamping circuit for VGS of each NGATE driver is implemented to protect the NMOS. However, when the NGATE is off, no negative clamping is implemented.

Either a single NMOS or back-to-back NMOS can be used for each port as shown in typical application circuit. The VGS rating of the NMOS must be considered for the safe operation.

The NGATE driver is controlled by VAG_ON / VBG_ON / VCG_ON bits respectively. However, they will be forced off no matter how the bits are set in some scenarios as below:

1. in standby mode (IDLE = 1), for all NGATE drivers
2. during boost soft-start in discharging mode if BlockSS = 0, for all NGATE drivers. The NGATE drivers return to normal operation after soft-start ends.
 - a) If BlockSS = 1, the boost soft-start will not impact the NGATE drivers.
3. Under protections as
 - a) input over voltage protection or under voltage protection (ACOK = 0), for corresponding NGATE driver
 - b) short circuit protection, for all NGATE drivers.

Refer to Adapter Detection section and Protections sections for details.

The NGATE driver status may affect the charging operation, depending on FORCE_CH bit as below:

- if FORCE_CH = 0, charging operation is only allowed when one of the VB / VC port is configured as charging

port, and its NGATE driver is turned on.

- If FORCE_CH = 1, the gate driver status will not affect the charging operation.

If other charging port is designed in the system, which is not controlled by the IC, the MCU shall set the FORCE_CH bit to 1 so to allow charging operation.

9.5 Phone Insert Detection

For the discharging port (VA or VB with VB_SET = 1), phone insert detection function is supported.

While the isolation MOS is off, the port (VA or VB) is only biased by an internal weak pull up. After a phone is inserted, the port voltage is pulled low by the operating current of the phone, so the IC can detect the phone attachment. When phone insert is detected, the corresponding interrupt bit (INDET_A or INDET_B) is set to inform MCU.

9.6 Adapter Detection

For the charging port (VB with VB_SET = 0, or VC with C_DIR = 0), the IC can detect the attachment / detachment of the adapter, and indicate the status through IN_UVP (B_IN_UVP or C_IN_UVP) and ACOK (VB_ACOK or VC_ACOK) bits.

9.6.1 IN_UVP Bit

IN_UVP is a status bit which reflects the under voltage condition. When the port voltage is lower than V_{IN_ACOK} , the bit is set to 1, indicating the adapter is bad or removed; when the port voltage is higher than V_{IN_ACOK} threshold, the bit is cleared to 0.

9.6.2 ACOK Bit

ACOK is an interrupt bit to report whether the adapter is good or bad.

The ACOK bit can reflect the under voltage status, depending on EN_INUVP bit as below:

- When EN_INUVP = 1, ACOK bit can also reflect the under voltage status, that is, the port voltage is lower than V_{IN_ACOK}
- When EN_INUVP = 0, it only reflect over voltage status.

When ACOK bit toggles (changes from 0 to 1 or from 1 to 0), the SC8949 generates an interrupt pulse at INT pin, to report the status change.

The reset of ACOK also initiates the protection mechanism, that is, the IC forces the corresponding NGATE driver off. For example, if VB_SET = 0, the VBG driver is forced off when VB_ACOK = 0.

Note: the port voltage may drop below V_{IN_ACOK} for a short period during charging startup due to inrush current. In order to avoid false trigger of the ACOK protection, it is suggested to set EN_INUVP to 0 during the charging startup and set it to 1 after startup.

9.7 Small Current Indication

The IC monitors its output current IBUS in discharging mode.

Once the IBUS is lower than 50mA typical, it reports the status to MCU through ICOM bit.

9.8 Pass-Through Mode

If DIR = 0 and Pass-Through = 1, the IC is set to Pass-Through mode, or called discharging-while-charging mode.

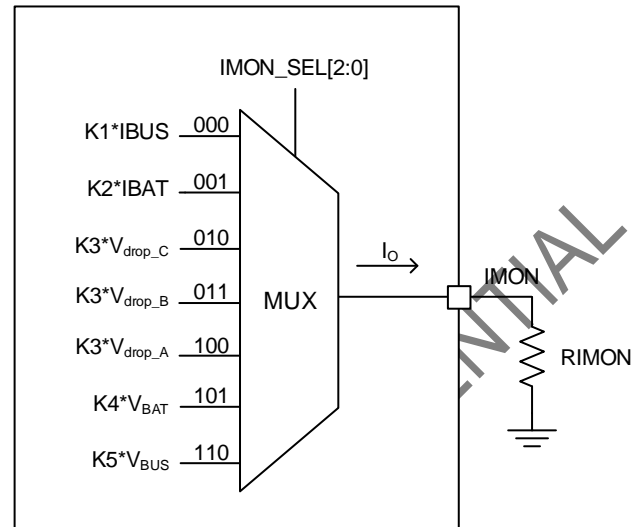
As same as in the charging mode, the IC works in buck mode and charges the battery. The only difference is that in pass-through mode, VBUS short circuit protection and VBUS under voltage protection are activated after charging starts. See 9.16 Protections section for protection details.

The IC doesn't determine it is in pass-through mode according to port status. It only enters into pass-through mode under the DIR and Pass-Through bits control.

9.9 Current and Voltage Monitor Function

The IC monitors the VBUS, VBAT, IBUS, IBAT, and voltage drop across each isolation NMOS in real time. It can output a proportional current I_O at IMON pin to the selected object as shown below, providing a way for MCU to monitor the IC input/output status.

User can use 27kΩ for R_{IMON} as a starting point, and can adjust the resistance if necessary.



$$K1 = 5.556 \times 10^{-6}$$

$$K2 = 4.386 \times 10^{-6}$$

$$K3 = 4.167 \times 10^{-4}$$

$$K4 = 10.06 \times 10^{-6}$$

$$K5 = 3.06 \times 10^{-6}$$

Figure 15 IMON monitor illustration

Leave 250ms delay time for the IMON function to work when the IC is just powered up from VBAT or VSYS.

After power up, when the IMON is switched between different objects, leave at least 50 μs time for the new IMON signal to establish. >10pF capacitor in parallel with R_{IMON} will cause longer establish time. 10 times of the RC constant time shall be considered for establishment for better signal sampling.

The IMON function keeps working when PSTOP = 1 but is disabled to save power when IDLE = 1.

9.9.1 IBUS and IBAT Current Monitor

When IMON_SEL[2:0] = 000B, IBUS current is monitored at IMON pin. When IMON_SEL[2:0] = 001B, IBAT current is monitored.

The DIR bit sets the IBUS / IBAT current monitor direction.

When DIR = 0, the charging current is monitored. If the current is out from battery, the IMON pin will indicate as 0A.

Similarly, when DIR = 1, the discharging current is monitored. If the current direction is into battery, the IMON pin indicates as 0A.

The relationships between IMON pin voltage and IBUS/IBAT current is shown as below:

$$I_{BUS} = \frac{V_{IMON}}{K1 \times R_{IMON}}$$

$$I_{BAT} = \frac{V_{IMON}}{K2 \times R_{IMON}}$$

Where $K1 = 5.47 \times 10^{-6}$, $K2 = 4.31 \times 10^{-6}$, R_{IMON} is the resistor connected at IMON pin.

For above calculation, 10mΩ current sense resistor must be used.

9.9.2 Port Current Monitor

When $IMON_SEL[2:0] = 010B / 011B / 100B$, the voltage drop across the NMOS of VC / VB / VA port is monitored at IMON pin respectively. The relationship is shown as below:

$$V_{IMON} = K3 \times V_{drop_X} \times R_{IMON}$$

$$I_X = \frac{V_{drop_X}}{R_{dson_X}} = \frac{V_{IMON}}{K3 \times R_{IMON} \times R_{dson_X}}$$

Where V_{drop_X} is the voltage drop between the isolation MOS for VX port, that is, the voltage drop between SNSP pin and VX pin; R_{dson_X} is the R_{dson} of the isolation MOS including the path resistance between SNSP pin and VX pin.

$X = A / B / C$; $K3 = 4.167 \times 10^{-4}$.

The voltage drop compliant with discharging direction is monitored for VA port;

VB_SET and C_DIR set the monitor direction for VB and VC ports.

If the real current direction is opposite to the setting, the IMON pin will indicate as 0A.

9.9.3 VBUS and VBAT Voltage Monitor

Besides the current information, the IMON pin can also be used to monitor the VBUS and VBAT voltage when $IMON_SEL[2:0] = 101B / 110B$.

The VBUS and VBAT can be calculated as:

$$V_{BAT} = \frac{V_{IMON}}{K4 \times R_{IMON}}$$

$$V_{BUS} = \frac{V_{IMON}}{K5 \times R_{IMON}}$$

Where $K4 = 10.06 \times 10^{-6}$ and $K5 = 3.06 \times 10^{-6}$

9.10 Discharging Path

The IC provides a discharging path of 1kΩ impedance from VBUS to ground. The MCU can turn on or off the discharging path by VBUS_DISPATH bit.

Similarly, the IC also provides a discharging path of 1kΩ impedance from VC to ground, and the MCU can turn on or off the discharging path by VC_DISPATH bit.

The discharging paths are designed to pull down the residue voltage on VBUS capacitor or on VC port when necessary. It is important to properly configurate VC or VBUS discharging patch during charging mode:

1. Keep VC_DISPATH is enabled when VC port is configurated as a charging port.
2. Keep VBUS_DISPATH is enabled when FORCE_CH mode is used.

9.11 NTC Function

The SC8949 can monitor the battery cell temperature through Negative Temperature Coefficient thermistor (NTC thermistor). The NTC thermistor shall be connected at NTC pin with external divider as shown in below figure.

The IC compares the NTC voltage with internal thresholds, so to decide whether the battery temperature is within a good range. If the temperature is outside the range, the IC stops the charging or discharging operation automatically for battery safety.

MCU can check the NTC status through STA1 register.

There is an internal switch between NTC_G and AGND pin. When IDLE = 1, the switch is auto-off, so to reduce the leakage. When IDLE = 0, the switch is auto-on, and the NTC function resumes after a 50ms delay.

User can short NTC pin to ground to disable the NTC function.

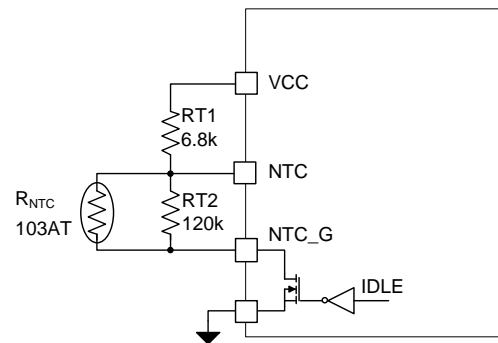


Figure 16 NTC Circuit

9.11.1 NTC for charging mode

There are four temperature zones for charging mode: cold, cool, normal and hot.

To initiate a charging cycle, the NTC voltage must be within

the cool or the normal range. When it is in the normal range, the SC8949 charges the battery normally. If in the cool range, the IBUS current is reduced to 1/2 of the setting value automatically. When beyond the normal or cool range, the IC suspends charging until the NTC voltage is within the range again.

The IC reports the abnormal temperature status by NTC_HOT, NTC_COOL and NTC_COLD bits.

Use below equation to calculate the RT1/RT2 resistance when a 103AT NTC thermistor is used as shown in the application circuit.

$$R_{T2} = \frac{R_{COLD} \times R_{HOT} \times \left(\frac{VCC}{V_{COLD_CH_R}} - \frac{VCC}{V_{HOT_CH_F}} \right)}{R_{HOT} \times \left(\frac{VCC}{V_{HOT_CH_F}} - 1 \right) - R_{COLD} \times \left(\frac{VCC}{V_{COLD_CH_R}} - 1 \right)}$$

$$R_{T1} = \frac{\frac{VCC}{V_{COLD_CH_R}} - 1}{\frac{1}{R_{T2}} + \frac{1}{R_{COLD}}}$$

Where, R_{HOT} is the NTC resistance at the hot temperature threshold; R_{COLD} is the resistance at the cold threshold.

For example, select 0°C (cold) to 45°C (hot) as the range for the charging. So R_{COLD} = 27.28 kΩ, R_{HOT} = 4.91 kΩ (resistance of 103AT thermistor at 0°C and 45°C).

So the calculation results are:

RT1 = 6.8 kΩ

RT2 = 120 kΩ

With above setting, the cool temperature threshold is around 10°C.

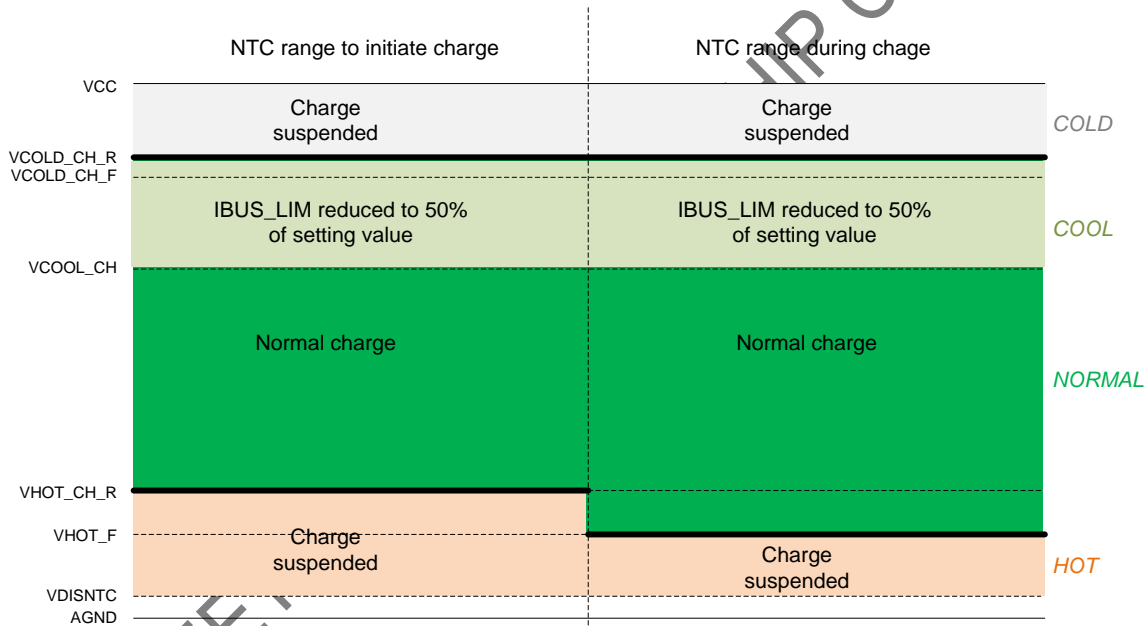


Figure 17 NTC zone for charging mode

9.11.2 NTC for discharging mode

There are three zones for discharging mode: cold, normal and hot. The NTC voltage must be within the normal range for normal operation.

The hot and cold thresholds are adjusted under discharging

mode. When RT1 = 6.8 kΩ and RT2 = 120 kΩ, the hot threshold is around 60°C, and the cold threshold is around -20°C.

The IC reports the abnormal temperature status by NTC_HOT and NTC_COLD bits for discharging mode.

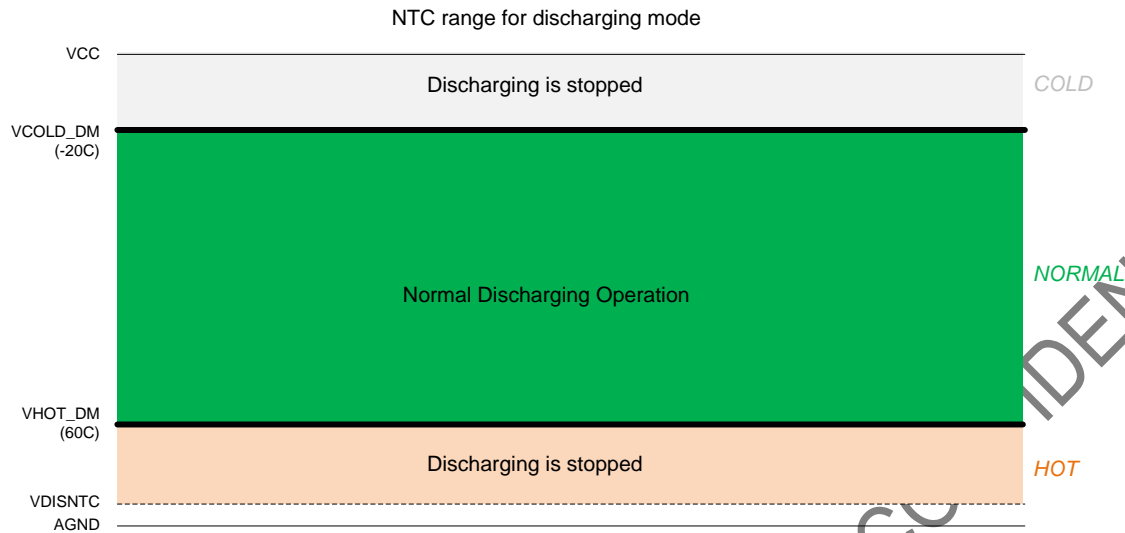


Figure 18 NTC zone for discharging mode

9.12 Switching Frequency

In charging mode (buck mode), the IC works in constant off time control; in discharging mode (boost mode), it works in constant on time control. The switching frequency can be configured through FSW_SET[1:0] bits for both charging mode and discharging mode.

9.13 Operation Modes

User can use PSTOP bit and IDLE bit to disable parts of the IC circuits.

9.13.1 Power Stop Mode

When PSTOP = 1, the IC stops the DCDC switching operation no matter in charging or discharging mode. The other circuits (including the NGATE drivers, IMON function) still work normally. It is called power stop mode.

The loop status indication bits are cleared when PSTOP is set to 1.

9.13.2 Standby Mode

When IDLE = 1, the IC enters into Standby mode with most functions disabled to save power.

The IC stops switching and forces all NGATE drivers off; the IMON and NTC function are also disabled; the internal switch at NTC_G pin disconnects NTC resistor divider.

The VCC regulator and LDO, I2C interface, phone insert detection and adapter detection circuit still work in standby mode. MCU can still configure the IC through I2C. The typical standby current drawn from VBAT pin is around 40 μ A.

The different operation modes are summarized below.

Table 2 Operation Mode Summary

IDLE bit	PTOP bit	Mode	VCC and LDO	DCDC switching	NGATE drivers	IMON function	NTC function	I2C interface
0	0	Active	Enabled	Enabled	Controlled by register	Enabled	Enabled	Enabled
0	1	Power Stop	Enabled	Disabled	Controlled by register	Enabled	Enabled	Enabled
1	x	Standby	Enabled	Disabled	Forced off	Disabled	Disabled	Enabled

9.14 Power Supply and VCC Regulator

VBUS pin just functions as the power node of the DCDC converter, and doesn't provide operation current to internal circuits.

The IC gets operation current from VBAT and VSYS pins. VBAT pin is connected to the battery, and the VSYS pin is connected to external supply (normally connected to the VBUS node). Put 1 μ F bypass capacitor from VSYS and VBAT pins to PGND respectively. The capacitors should be close to the IC.

The IC integrates a 5.1V regulator (VCC regulator) to power the internal circuits including the power drivers and NGATE drivers. The regulator input is from the higher voltage of VSYS and VBAT. If the input voltage is lower than 5.1V, the VCC regulator operates in fully conduction mode.

The VCC regulator supports at least 70mA load capability. Current limit function is designed. The IC reduces the VCC voltage when the total load (including the internal operation current) exceeds I_{VCC_LIM} value. Connect at least 1 μ F capacitor from VCC to AGND close to the IC.

To get enough driver voltage, VSYS pin is normally connected to VBUS node with a diode. However, user must check whether VBUS node has voltage under dead battery condition. If VBUS is isolated from adapter input by back-to-back NMOS, the adapter input shall be connected to VSYS pin with a diode as well. Never connecting VSYS to VBUS or any other voltage source directly. Schottky diodes with low forward voltage drop and tiny package are suitable for this application.

Refer to Typical Application Circuit for connection illustration.

9.15 LDO Regulator

The IC integrates an LDO to power the MCU controller or other chips in the system. The output of LDO can be set to 3.3V or 2.8V by VLDO_SET bit. No current limit is implemented for this regulator. If its load is too high, the VCC current limit will be triggered.

Connect at least 1 μ F capacitor from LDO to AGND close to the IC.

9.16 Protections

9.16.1 Over Current Protection

The IC monitors the IBUS and IBAT current in charging and discharging mode. Once the current exceeds the current limit set by IBUS_LIM[7:0] or IBAT_LIM [1:0], the IC regulates the current at the limit value.

MCU can also monitor the port current through IMON pin, and decide whether the port is over current and what protection shall be taken.

9.16.2 Input Port Under Voltage Protection

For the charging port(s), if the port voltage (VB if VB_SET = 0; or VC if C_DIR = 0) is lower than V_{IN_ACOK} threshold, the IN_UVP status bit (B_IN_UVP or C_IN_UVP) is set to 1, indicating the adapter is bad or removed.

When EN_INUVP = 1, the ACOK bit also reflects the under voltage status. When under voltage fault happens, the corresponding ACOK bit is reset to 0 at once and the corresponding NGATE driver is forced off. The bit and NGATE driver return to normal status after the UVP fault is removed with 20ms delay time.

When EN_INUVP = 0, the ACOK bit doesn't reflect the under voltage status. So when fault happens, only IN_UVP bit reflects the status, and the IC keeps normal operation. However, if the VBUS voltage is below the VINREG threshold, the VINREG loop will stop the charging.

For the charging port, the inrush current during startup may pull the port voltage down, result in false trigger of the under voltage protection. In order to avoid false triggering, it is suggested to set IBUS below 500mA as the initiate charging current then adjust this current by the adapter information which detected by DP/DM or CC signals, or disable EN_UVP temporarily during charging start-up process.

9.16.3 Boost Output Over Voltage Protection

In discharging mode, the IC monitors the output voltage through internal or external feedback resistors (decided by FB_SEL bit). Once the IC detects the VBUS voltage is higher than OVP threshold, the IC stops switching until the FB recovers. The NGATE drivers keep normal operation during the OVP process.

For external setting way (FB_SEL = 1), the OVP is decided by FB voltage; for internal setting (FB_SEL = 0), the OVP is decided by VBUS voltage. Please find the summary below.

Table 3 Boost OVP Threshold Summary

FB_SEL	OVP threshold
1	$V_{FB_OVP} = 1.2V \times 110\% = 1.32V$
0	$V_{BUS_OVP} = V_{BUS\ target} + 500mV$

9.16.4 FB Pin Short Circuit Protection

With external voltage setting (FB_SEL = 1) in discharging mode, once FB pin is detected short to ground, the IC changes to internal setting way automatically, and the output



voltage is decided by `VBUS_SET[9:0]`. The IC reports the FB shortage fault through `FB_SC` bit. After FB pin shortage fault is removed, the IC changes back to external setting way automatically. It is suggested to keep `VBUS_SET[9:0] = 0` when `FB_SEL = 1`, so the IC can output a safe 5V when FB pin short circuit fault happens.

9.16.5 VBUS Short Circuit Protection

In discharging mode or pass-through mode, if the IC detects that VBUS voltage drops below VBAT for a period (1 μ s or 90 μ s, configured by `Short_CTRL` bit), the IC reports the short circuit fault through `VBUS_SHORT` bit. The IC still keeps switching but forced all the NGATE drivers off no matter for charging port or discharging port to protect the IC.

The IC supports hiccup mode when `Short_auto_rtr = 1`. It tries to recover the NGATE drivers to normal operation every 500ms. If the short circuit fault is still there, all the NGATE drivers will be forced off again. After the fault is removed, the `VBUS_SHORT` bit is cleared to 0, and the IC returns to normal operation. When in pass-through mode, `Short_auto_rtr = 0` is recommended, MCU should recover charging port first, then the discharging port.

If `Short_auto_rtr = 0`, all the NGATE drivers latch in off status until MCU sets `Short_RST` bit to 1 to reset. If the short circuit fault is still there after resetting, the IC enters to NGATE drivers latch off status again until next reset operation from MCU.

9.16.6 VBUS Under Voltage Protection/Soft Short Circuit Protection

When `EN_VBUSUVP = 1`, the VBUS under voltage protection is enabled for both discharging mode and pass-through mode. This protection is similar to VBUS short circuit protection, so is called soft short protection.

If the VBUS voltage is below 3.8V or 4.5V (set by `VBUS_UVP_SET`) for more than 8ms, under voltage fault is detected and the IC triggers the same protection as the VBUS short circuit protection, that is, the `VBUS_SHORT` bit is set to 1, and the IC turns off all NGATE drivers. If `Short_auto_rtr = 1`, the IC supports hiccup mode, trying to recover every 500ms; if `Short_auto_rtr = 0`, the IC latches in off status until MCU sets `Short_RST` bit to 1.

When `EN_VBUSUVP = 0`, the VBUS under voltage detection is disabled.

9.16.7 VBAT Over Voltage Protection

When VBAT is higher than `V_BAT_OVP` threshold (103% of VBAT target) no matter in charging mode or discharging

mode, the IC sets `VBAT_OVP` bit to 1 to report the battery over voltage status.

If `EN_VBATOVP = 1`, the IC takes further protections, that is, it stops switching and turns on a 1k Ω path from VBAT to GND to discharge the battery. It returns to normal operation after VBAT drops below 101% of the target. The NGATE drivers keep normal operation during protection.

If `EN_VBATOVP = 0`, the IC just sets `VBAT_OVP` to report the status and keeps switching. MCU can set `EN_VBATOVP` to 0 in discharging mode so to allow normal operation for over-voltage battery.

9.16.8 Thermal Shutdown

When the IC detects the chip junction temperature is higher than 165 $^{\circ}$ C, the IC stops switching to protect the chip, and sets the OTP interrupt bit to inform the MCU. It resumes switching and clear OTP bit once the temperature drops below 150 $^{\circ}$ C. The NGATE drivers keep normal operation during protection.

9.17 I2C and Interrupt

9.17.1 I2C Interface

The IC features I2C interface, so the MCU can program and control the IC flexibly.

The 7-bit I2C address of the chip is 0x76 (8-bit address is 0xEC for write command, 0xED for read command).

The SDA and SCL pins are open drain and must connect to the power rail through pull-up resistors. When the I2C bus is free, both SDA and SCL output high impedance. The I2C interface supports standard mode (up to 100kbits) and fast mode (up to 400k bits). To support fast mode, 4.7 kΩ pull up resistor is suggested for SCL and SDA respectively.

9.17.1.1 Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. One clock pulse is generated for each data bit transferred.

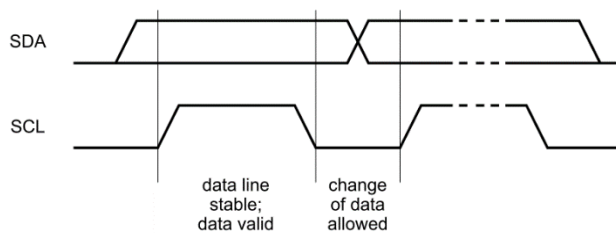


Figure 19 Bit transfer on the I2C bus

9.17.1.2 START and STOP Conditions

All transactions begin with a START (S) and are terminated by a STOP (P). A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition.

START and STOP conditions are always generated by the master. The bus is considered to be busy after the START condition. The bus is considered to be free again a certain time after the STOP condition.

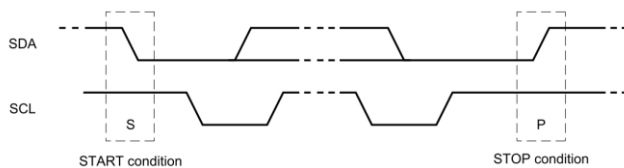


Figure 20 START and STOP conditions

9.17.1.3 Byte Format

Every byte put on the SDA line must be eight bits long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte must be followed by an Acknowledge bit. Data is transferred with the Most Significant Bit (MSB) first. If a slave cannot receive or transmit another complete byte of data until it has performed some other function, for example servicing an internal interrupt, it can hold the clock line SCL LOW to force the master into a wait state. Data transfer then continues when the slave is ready for another byte of data and releases clock line SCL.

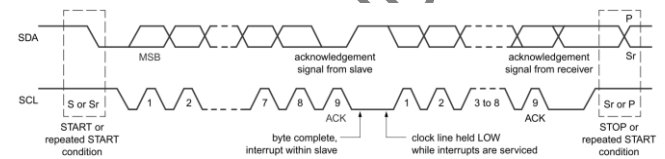


Figure 21 Data transfer on the I2C bus

9.17.1.4 Acknowledge (ACK) and Not Acknowledge (NACK)

The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. During data is transferred, the master can either be the transmitter or the receiver. No matter what it is, the master generates all clock pulses, including the acknowledge ninth clock pulse.

The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line LOW and it remains stable LOW during the HIGH period of this clock pulse.

When SDA remains HIGH during this ninth clock pulse, this is defined as the Not Acknowledge signal. The master can then generate either a STOP condition to abort the transfer, or a repeated START condition to start a new transfer.

9.17.1.5 The slave address and R/W bit

Data transfers follow the format shown in below. After the START condition (S), a slave address is sent. This address is seven bits long followed by an eighth bit which is a data direction bit (R/W) — a 'zero' indicates a transmission (WRITE), a 'one' indicates a request for data (READ). A data transfer is always terminated by a STOP condition (P) generated by the master. However, if a master still wishes to communicate on the bus, it can generate a repeated START condition (Sr) and address another slave without first generating a STOP condition.

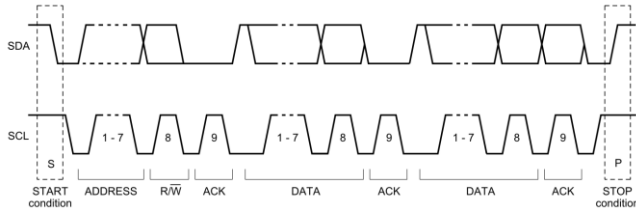


Figure 22 A complete data transfer

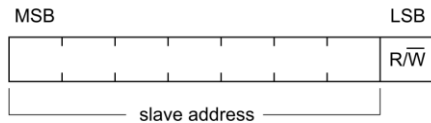


Figure 23 The first byte after the START procedure

9.17.1.6 Single Read and Write

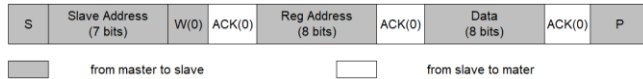


Figure 24 Single Write

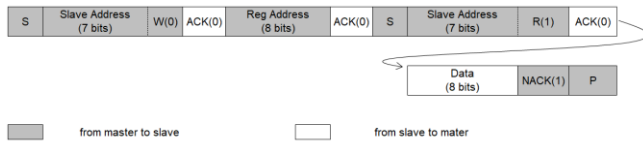


Figure 25 Single Read

If the register address is not defined, the charger IC send back NACK and go back to the idle state.

9.17.1.7 Multi-Read and Multi-Write

The IC supports multi-read and multi-write for continuous registers.

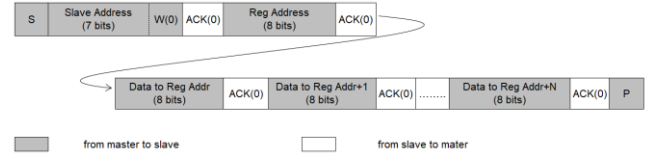


Figure 26 Multi-Write

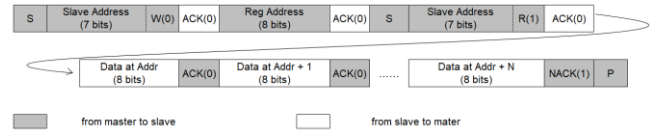


Figure 27 Multi-Read

9.17.2 Interrupt

When below events happen, the IC sends a 1ms active low interrupt pulse at INT pin to inform MCU.

- VBUS_SHORT changes from 0 to 1
- INDET_B changes from 0 to 1
- INDET_A changes from 0 to 1
- VC_ACOK changes from 0 to 1, or changes from 1 to 0
- VB_ACOK changes from 0 to 1, or changes from 1 to 0

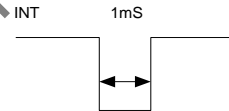


Figure 28 Interrupt pulse at INT pin

User can mask an interrupt by setting its corresponding bit in INT_Mask register. When the mask bit is set, the corresponding interrupt bit is still set, but the IC doesn't generate the interrupt pulse at INT pin.

9.17.3 Reset

If MCU sets the RESET bit to 1, all registers are reset to default values, and the RESET bit will be resets to 0 automatically after being written to 1.



10 Application Information

10.1 Capacitor Selection

As the output node of the boost converter, VBUS node needs enough capacitors to reduce the voltage ripple. The voltage ripple is determined as below

$$V_{\text{Ripple_DIS}} = \frac{(\text{VBUS}-\text{VBAT}) \cdot \text{IBUS}}{\text{VBUS} \cdot \text{fsw} \cdot \text{C}_{\text{BUS}}}$$

$$V_{\text{Ripple_ESR}} = I_{\text{Lpeak}} \cdot R_{\text{C_ESR}}$$

Where

$V_{\text{Ripple_DIS}}$ is the output ripple caused by the switching current charging and discharging the output capacitor at VBUS

$V_{\text{Ripple_ESR}}$ is the output ripple caused by the ESR of output capacitor

I_{Lpeak} is the peak current of the inductor

fsw is the switching frequency, in the range of 300kHz ~ 750kHz

C_{BUS} is the effective capacitance of the capacitors connected between VBUS and GND

$R_{\text{C_ESR}}$ is the Equivalent Series Resistor of the capacitors.

For small ripple, low ESR output capacitor like MLCC ceramic capacitor is recommended. Typically 66 μF (three 22 μF in parallel) X5R or X7R MLCC capacitors work for most applications. Higher capacitors can be used to improve the load transient response. When selecting capacitors, the degrading effect of MLCC effective capacitance under DC bias must be considered. Ceramic capacitors can lose most capacitance at rated voltage; for example, the effective C_{BUS} is normally much lower than 66 μF when three 22 μF ceramic capacitors are used. Enough voltage rating (higher voltage than operating voltage with margin) is recommended. Check the effective capacitance at the operating voltage to make sure the voltage ripple can be maintained.

MLCC capacitor of small package size normally has better high frequency filtering, so a 1 μF MLCC of 0402 package size is highly recommended to added in parallel and put as close to VBUS pin as possible.

The polymer capacitor normally has lower ESR than electrolytic capacitor and higher capacitance than MLCC, for the applications which require very small output ripple and better load transient performance, the high capacitance polymer capacitor is recommended. However, since its high frequency characteristic is not as good as MLCC, at least 1 μF + 10 μF MLCC capacitor must be used and placed in parallel to reduce high frequency ripple. The smaller the

capacitance, the closer it should be to the chip.

10.2 Inductor Selection

1.5 μH ~ 3.3 μH inductor is recommended for loop stability. The peak inductor current in discharging mode can be calculated as

$$I_{\text{L_peak}} = \text{IBAT} + \frac{\text{VBAT} \cdot (\text{VBUS} - \text{VBAT} \cdot \eta)}{2 \cdot \text{fsw} \cdot \text{L} \cdot \text{VBUS}}$$

where IBAT is the battery current at VBAT side, and can be calculated as

$$\text{IBAT} = \frac{\text{VBUS} \cdot \text{IBUS}}{\eta \cdot \text{VBAT}}$$

η is the power conversion efficiency. User can use 90% for calculation.

fsw is the switching frequency

L is the inductor value

The peak inductor current in charging mode can be calculated as

$$I_{\text{L_peak}} = \text{IBAT} + \frac{\text{VBAT} \cdot (\text{VBUS} - \text{VBAT})}{2 \cdot \text{fsw} \cdot \text{L} \cdot \text{VBUS} \cdot \eta}$$

where IBAT is the battery charging current at VBAT side, and can be calculated as

$$\text{IBAT} = \frac{\text{VBUS} \cdot \text{IBUS} \cdot \eta}{\text{VBAT}}$$

η is the power conversion efficiency. User can use 90% for calculation.

fsw is the switching frequency

L is the inductor value

When selecting inductor, the inductor saturation current must be higher than the peak inductor current with enough margin (20% margin is recommended). The rating current of the inductor must be higher than the battery current.

The inductor DC resistance value (DCR) affects the conduction loss of switching regulator, so low DCR inductor is recommended especially for high power application. The conductor loss of inductor can be calculated roughly as

$$P_{\text{L_DC}} = I_{\text{L}}^2 \cdot \text{DCR}$$

I_{L} is the average value of inductor current, and it equals to IBAT or IBUS.

Besides DC power loss, there are also inductor AC winding loss and inductor core loss, which are related to inductor peak current. Normally, higher peak current causes higher AC loss and core loss. The user shall consult with the inductor vendor to select the inductor which has small ESR at



high frequency and small core loss.

10.3 Current Sense Resistor

10 mΩ should be used to sense IBUS current. Resistor of 1% or higher accuracy and low temperature coefficient is recommended.

The resistor power rating and temperature coefficient should be considered. The power dissipation can be roughly calculated as $P=I^2R$, and I is the RMS current flowing through the resistor. The resistor power rating should be higher than the calculated value.

Normally the resistor value is varied if the temperature increased and the variation is decided by temperature coefficient. If high accuracy of current limit is required, select lower temperature coefficient resistor as much as possible.

10.4 SW Snubber Circuit

To adjust MOSFET switching time and switching overshoot for EMI debugging, it is recommended to add RC snubber (0603 size) circuit at SW, as shown in Figure .

The RC snubber is helpful in absorbing the high frequency spike at SW node, so to improve EMC performance. User can leave RC components as NC at the beginning, and adjust the value to improve the EMC performance if necessary. Normally user can try 2.2Ω and 1nF for the snubber. If EMC should be improved further, reduce the resistor value (like 1 Ω or even lower) and increase the capacitor value (like 2.2nF or even higher).

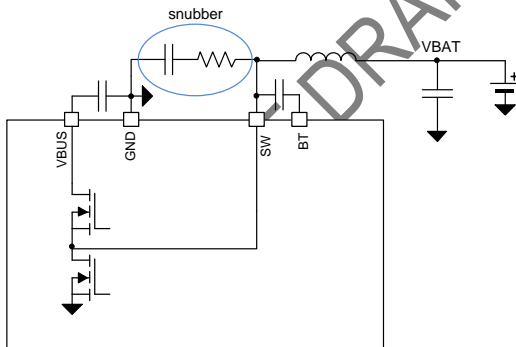


Figure 29 Snubber circuit

Besides snubber circuit, user can also use DRV_LS_SET and DRV_HS_SET bits to adjust the driver capability of the internal driver circuits. Strong capability helps reduce the switching loss so to achieve higher power conversion efficiency, while weak capability helps suppress the switching spike, improving the EMI performance.

10.5 Isolation MOSFET Selection

For the VA/VB/VC port, N-channel MOSFET can be used as isolation switch.

When selecting the MOSFET, user shall consider the VGS rating, VDS rating and the R_{ds(on)} parameters.

When the NGATE driver is turned on, the IC outputs VCC based on the lower voltage of VBUS and port voltage, that is, $V_{GX} = VCC + \min(VBUS, 5V\text{-Typical})$. There is also clamping circuit designed which guarantees the VGS voltage doesn't exceed 8V. However, when the NGATE driver is turned off, VGX pin is pulled to ground, so user shall consider the VGS voltage the MOS will see in the application and select the right rating.

The V_{DS} of MOSFET should be higher than the highest VBUS operating voltage with enough margin.

The MOSFET current I_b should be higher than the highest port current with enough margin.

To ensure the sufficient current capability in relatively high temperature circumstance, the current rate at T_A=70°C or T_C=100°C should be considered. In addition, the power dissipation value P_D should also be considered and higher P_b is better in applications. Make sure that MOSFET power consumption must not exceed P_D value.

10.6 Diode Selection

The IC can get power from VSYS pin to power the internal driver circuits and the LDO. To get enough capability, VBUS node shall be connected to VSYS; if there is charging port where back-to-back isolation is used, the port voltage shall also be connected to VSYS pin. Diodes shall be used when multiple rails are connected.

To improve the driver capability, Schottky diodes of small voltage drop are recommended for applications where high current capability of VCC or LDO is required.

10.7 Layout Guide

1. The capacitors connected at VBUS/VBAT/VCC/VDRV pins should be placed near the IC, and their ground connection to the ground pins should be as short as possible.
2. The current sense resistor and bulk capacitor at VBUS side should be placed very close to VBUS and PGND pins.
3. The isolation MOSFETs for each port shall be put as close to the 10mΩ current sense resistor as possible. Isolate the current path if possible (as illustrated below).



This is helpful to improve the accuracy of port current detection

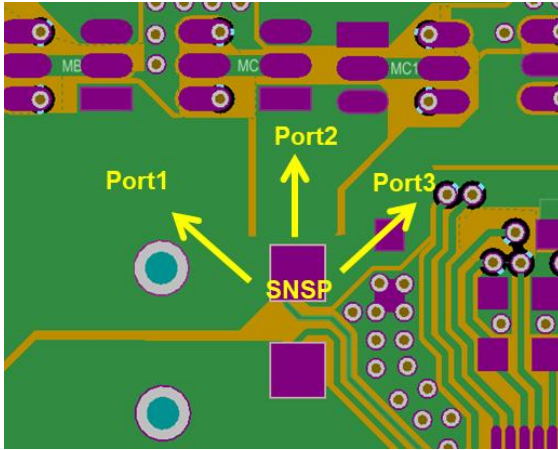


Figure 30 Isolation of current path for each port

- 4. The current sense traces should be connected to the current sense resistor's pads in Kelvin sense way as

below, and routed in parallel (differential routing), and the filter for current sense should be placed near the IC.

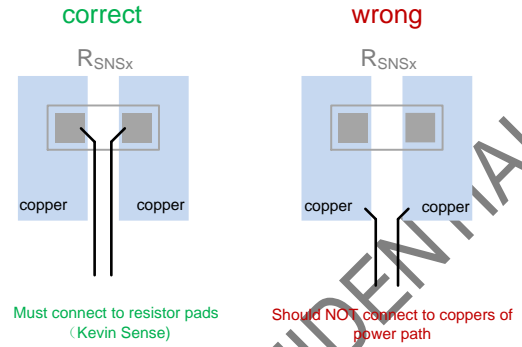


Figure 31 Current sense

- 5. The FB resistor divider and COMP pin components should be placed near IC, and connect to AGND (analog ground) pin. Then connect the AGND pin and PGNDs at the PGND pad under IC.

11 Register Map

The 7-bit I2C address of the chip is 0x76 (8-bit address is 0xEC for write command, 0xED for read command).

Addr	Register	Type	Default	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Go to
01H	MODE	R/W	0010 0000	Short_CTRL	FB_SEL	ITRKL_SET	VLDO_SET	VB_SET	C_DIR	Pass-Through	DIR	Table 4
02H	PWR_SET	R/W	0100 0110	FSW_SET[1:0]		Reserved	FORCE_CH	IDLE	DRV_LS_SET	DRV_HS_SET	PSTOP	Table 5
03H	PWR_PATH	R/W	0000 0000	Reserved	Reserved	BlockSS	VBUS_DISPATH	VC_DISPATH	VAG_ON	VBG_ON	VCG_ON	Table 6
04H	IMON	R/W	0010 0000	INDET_SET	RECH_SET	EN_OOA	CBLCOMP_CTRL[1:0]		IMON_SEL[2:0]			Table 7
05H	CHAR_SET	R/W	0010 0001	VINREG_SET [2:0]			ITERM_SET[1:0]		VBAT_SET[2:0]			Table 8
06H	IBUS_LIM	R/W	0001 0010	IBUS_LIM[7:0]								Table 9
07H	VBUS_SET_MSB	R/W	0000 0000	VBUS_SET[9:2]								Table 10
08H	VBUS_SET_LSB	R/W	0000 0000	Reserved						VBUS_SET[1:0]		Table 11
09H	Load	W1C	0000 0000	Reserved						IBUS_LIM_Load	VBUS_SET_Load	Table 12
0AH	IBAT_LIM	R/W	0000 0010	Reserved				Min_IBUS_clamp_setting[1:0]		IBAT_LIM [1:0]		Table 13
0BH	PRO_SET	R/W	0001 1101	DIS_TERM	VBUS_UVP_SET	EN_VBATOVP	EN_VBUSUVP	Short_auto_rtr	EN_INUVP	Reserved	Reserved	Table 14
0CH	CTRL	W1C	0000 0000	Reserved					RESET	Reserved	Short_RST	Table 15
0DH	Loop_STA	R	0000 0000	Reserved				IBAT_Loop	VINREG_Loop	CC_Loop	CV_Loop	Table 16
0EH	STA1	R	0000 0000	Reserved		OTP	NTC_hot	NTC_cool_ch	NTC_cold	EOC	ICOM	Table 17
0FH	STA2	R	0000 0000	Reserved	FB_SC	VBAT_OVP	Reserved	Reserved	Reserved	C_IN_UVP	B_IN_UVP	Table 2
10H	INT	R	0000 0000	Reserved			VBUS_SHORT	INDET_B	INDET_A	VC_ACOK	VB_ACOK	Table 19
11H	INT_Mask	R/W	0000 0000	Reserved			VBUS_SHORT_M	INDET_B_M	INDET_A_M	VC_ACOK_M	VB_ACOK_M	Table 20

Table 4 0x01 MODE Register ([go back to map](#))

Bit	Type	Bit Name	Default	Description	Notes
7	R/W	Short_CTRL	0	Set the short circuit detection time (VBUS<VBAT) for discharging mode and pass-through mode 0: 1 μs (default) 1: 90 μs	
6	R/W	FB_SEL	0	Configure the VBUS output voltage setting way for discharging mode 0: internal feedback resistors are used, and the VBUS voltage can be set through VBUS_SET[9:0] bits. (default) 1: the VBUS output is set by the external resistor divider connected at FB pin User shall keep the FB_SEL unchanged while the IC operates. Change is only allowed when PSTOP = 1 or IDLE = 1.	
5	R/W	ITRKL_SET	1	Set the battery current (IBAT) regulation target in trickle charge phase 0: 260mA 1: 540mA (default)	
4	R/W	VLDO_SET	0	Set the LDO output voltage 0: 2.8V (default) 1: 3.3V	
3	R/W	VB_SET	0	Set the function of the VB port 0: as charging port, supporting adapter plug and removal detection. Charging current can be monitored (default) 1: as discharging port, supporting load insert detection. Discharging current can be monitored	
2	R/W	C_DIR	0	Set the function of the VC port 0: as charging port, supporting adapter plug and removal detection. Charging current can be monitored. For TYPE-C application, set this bit to 0 after the port is determined as sink/UFP role. (default) 1: as discharging port, NOT supporting load insert detection. Discharging current can be monitored. For TYPE-C application, set this bit to 1 after the port is determined as source/DFP role.	
1	R/W	Pass-Through	0	Set the IC in pass-through mode so to enable VBUS short circuit protection during charging. 0: Not in pass-through mode. VBUS short circuit protection is disabled when DIR = 0 (default) 1: set in pass-through mode. VBUS short circuit protection is enabled when DIR = 0.	
0	R/W	DIR	0	Set the charging/discharging mode 0: charging mode (default) 1: discharging mode	

Table 5 0x02 PWR_SET Register ([go back to map](#))

Bit	Type	Bit Name	Default	Description	Notes
7-6	R/W	FSW_SET[1:0]	01	Set the switching frequency of the IC 00: 300kHz 01: 450kHz (default) 01: 600kHz 11: 750kHz	
5	R/W	Reserved	0	Reserved	
4	R/W	FORCE_CH	0	Configure the startup condition for charging operation 0: At least one of VA / VB / VC ports must be configured as charging port, and only after the NGATE driver of the charging port is fully turned on, the IC can start charging operation (default) 1: The charging operation doesn't rely on the port configuration and NGATE driver status. Set this bit to 1 to allow charging operation for the extra charging port instead of VB or VC.	
3	R/W	IDLE	0	Idle mode control 0: normal operation (default) 1: set IC into idle state	
2	R/W	DRV_LS_Set	1	Adjust the low side driver capability for EMI performance 0: weak 1: strong (default)	
1	R/W	DRV_HS_Set	1	Adjust the high side driver capability for EMI performance 0: weak 1: strong (default)	
0	R/W	PSTOP	0	Power stop control. 0: normal operation (default) 1: power stage (DCDC) stops switching	

Table 6 0x03 PWR_PATH Register ([go back to map](#))

Bit	Type	Bit Name	Default	Description	Notes
7	R/W	Reserved	0	Reserved	
6	R/W	Reserved	0	Reserved	
5	R/W	BlockSS	0	Set whether the NGATE driver will be forced off during boost start-up process in discharging mode 0: all of the NGATE drivers are forced off during boost start-start process (default) 1: the NGATE drivers keeps normal operation during boost start-up	

4	R/W	VBUS_DISPATH	0	Control the discharging path from VBUS to GND (typ. 1 kΩ) 0: disable the discharging path (default) 1: enable the discharging path
3	R/W	VC_DISPATH	0	Control the discharging path from VC to GND (typ. 1 kΩ) 0: disable the discharging path (default) 1: enable the discharging path
2	R/W	VAG_ON	0	NMOS gate driver control at VAG pin 0: turn off the gate driver (default) 1: turn on the gate driver
1	R/W	VBG_ON	0	NMOS gate driver control at VBG pin 0: turn off the gate driver (default) 1: turn on the gate driver
0	R/W	VCG_ON	0	NMOS gate driver control at VCG pin 0: turn off the gate driver (default) 1: turn on the gate driver

Table 7 0x04 IMON Register ([go back to map](#))

Bit	Type	Bit Name	Default	Description	Notes
7	R/W	INDET_SET	0	Set the pull up capability for phone insert detection 0: strong (default) 1: weak	
6	R/W	RECH_SET	0	Set the recharge threshold for charging mode 0: 97.4% of VBAT target(default) 1: 96.2% of VBAT target	
5	R/W	EN_OOA	1	PFM Out-of-Audio (OOA) Mode Control 0: Out-of-audio mode disabled while converter is in PFM 1: Out-of-audio mode enabled while converter is in PFM (default)	
4-3	R/W	CBLCOMP_CTRL[1:0]	00	Configure the cable drop compensation ratio R_{COMP_SET} for VBUS output voltage in discharging mode, effective for both internal and external VBUS setting 00: disabled (default) 01: 50 mV/A 10: 100 mV/A 11: 150 mV/A	
2-0	R/W	IMON_SEL[2:0]	000	Select the object to monitor at IMON pin 000: IBUS current, direction is decided by DIR bit (default) 001: IBAT current, direction is decided by DIR bit	

				010: voltage drop between VC and SNSP, direction is decided by C_DIR bit 011: voltage drop between VB and SNSP, direction is decided by VB_SET bit 100: voltage drop between VA and SNSP, direction is from SNSP to VA 101: VBAT 110: VBUS 111: reserved	
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Table 8 0x05 CHAR_SET Register ([go back to map](#))

Bit	Type	Bit Name	Default	Description	Notes
7-5	R/W	VINREG_SET [2:0]	001	Set the VINREG threshold for charging mode 000: 4.4V 001: 4.5V (default) 010: 4.6V 011: 4.7V 100: 4.8V 101: 4.9V 110: Reserved 111: Reserved	
4-3	R/W	ITERM_SET	00	Set the termination threshold for battery current IBAT in charging mode 00: 130mA (default) 01: 200mA 10: 300mA 11: 400mA	
2-0	R/W	VBAT_SET	001	Set the VBAT target for charging mode. 000: 4.1V 001: 4.2V (default) 010: 4.25V 011: 4.3V 100: 4.35V 101: 4.4V 110: 4.45V 111: 4.5V	

Table 9 0x06 IBUS_LIM Register ([go back to map](#))

Bit	Type	Bit Name	Default	Description	Notes
7-0	R/W	IBUS_LIM[7:0]	0001 0010	<p>Set the IBUS current limit, effective for both charging mode and discharging mode.</p> <p>$IBUS_LIM(A) = IBUS_LIM[7:0] \times 25mA$</p> <p>25mA/step, from a clamping current (decided by Min_IBUS_clamp_setting[1:0]) to 6.375A</p> <p>Default at 450mA (0x12)</p> <p>The change will not take effect until IBUS_LIM_Load is set to 1.</p>	

Table 10 0x07 VBUS_SET_MSB Register ([go back to map](#))

Bit	Type	Bit Name	Default	Description	Notes
7-0	R/W	VBUS_SET[9:2]	0000 0000	<p>Highest 8 bits of VBUS_SET registers. Set the VBUS output voltage in discharging mode when internal setting way is selected (FB_SEL = 0)</p> <p>$VBUS(V) = 5V + 10mV \times (VBUS_SET[9:2] \times 4 + VBUS_SET[1:0])$</p> <p>40mV/step for the high 8 bits</p> <p>VBUS Default at 5V + 0V (0x00)</p> <p>The change will not take effect until VBUS_SET_Load is set to 1.</p> <p>Keep the register at fault value if external setting way is used (FB_SEL = 1)</p>	VBUS<6V

Table 11 0x08 VBUS_SET_LSB Register ([go back to map](#))

Bit	Type	Bit Name	Default	Description	Notes
7-2	R/W	Reserved	0000 0000	Reserved	
1-0	R/W	VBUS_SET[1:0]	00	<p>Lowest 2 bits of VBUS_SET registers. Set the VBUS output voltage in discharging mode when internal setting way is selected (FB_SEL = 0)</p> <p>$VBUS(V) = 5V + 10mV \times (VBUS_SET[9:2] \times 4 + VBUS_SET[1:0])$</p> <p>10mV/step for the low 2 bits</p> <p>VBUS Default at 5V + 0V (00)</p> <p>The change will not take effect until VBUS_SET_Load is set to 1.</p> <p>Keep the register at fault value if external setting way is used (FB_SEL = 1)</p>	VBUS<6V

Table 12 0x09 Load Register ([go back to map](#))

Bit	Type	Bit Name	Default	Description	Notes
7-2	R/W	Reserved	0000 000	Reserved	
1	W1C	IBUS_LIM_Load	0	Set this bit to 1 to load the IBUS_LIM[7:0] setting into circuit. Any change of IBUS_LIM[7:0] can only take effect after this bit is set to 1. This bit resets to 0 automatically after being written to 1.	
0	W1C	VBUS_SET_Load	0	Set this bit to 1 to load the VBUS_SET[9:0] setting into circuit. Any change of VBUS_SET[9:0] can only take effect after this bit is set to 1. This bit resets to 0 automatically after being written to 1.	

Table 13 0x0A IBAT_LIM Register ([go back to map](#))

Bit	Type	Bit Name	Default	Description	Notes
7-4	R/W	Reserved	0000	Reserved	
3-2	R/W	Min_IBUS_clamp_setting[1:0]	00	Set the minimum clamping value for IBUS_LIM[7:0] 00: 150mA (default) 01: 200mA 10: 250mA 11: 300mA The change will not take effect until IBUS_LIM_Load is set to 1.	
1-0	R/W	IBAT_LIM[1:0]	10	Set the battery current limit value 00: 4A for charging mode, 6A for discharging mode 01: 6A for charging mode, 8A for discharging mode 10: 8A for charging mode, 10A for discharging mode (default) 11: 10A for charging mode, 12A for discharging mode	

Table 14 0x0B PRO_SET Register ([go back to map](#))

Bit	Type	Bit Name	Default	Description	Notes
7	R/W	DIS_TERM	0	Configure the charger behavior at end of charge phase 0: IC terminates the charging automatically after EOC (default) 1: IC keeps regulating VBAT voltage after EOC	
6	R/W	VBUS_UVP_SET	0	Set the VBUS under voltage threshold 0: 3.8V (default) 1: 4.5V	

5	R/W	EN_VBATOVP	0	Configure the protection mechanism when VBAT OVP status is detected, effective for both charging and discharging mode 0: IC keeps normal operation (default) 1: IC stops switching. It recovers to normal operation after the fault is removed
4	R/W	EN_VBUSVP	1	Enable VBUS under voltage detection 0: disable the under voltage detection 1: enable the VBUS under voltage detection, and once VBUS under voltage is detected, IC forces all NGATE drivers off. Whether the IC recovers normal operation depends on Short_auto_rtr bit (default)
3	R/W	Short_auto_rtr	1	Configure the protection mechanism when VBUS short circuit or VBUS under voltage fault is detected, effective for discharging mode and pass-through mode 0: All NGATE drivers are forced off until Short_RST bit is set to 1 1: All NGATE drivers are forced off, and IC tries to return normal operation every 500ms (default)
2	R/W	EN_INUVP	1	Configure the protection mechanism when input under voltage is detected for charging port(s). 0: ACOK bit will not reflect the status, and IC keeps normal operation, 1: ACOK bit is reset to 0, and the corresponding NGATE driver is forced off (default)
1	R/W	Reserved	0	Reserved
0	R/W	Reserved	1	Reserved

Table 15 0x0C CTRL Register ([go back to map](#))

Bit	Type	Bit Name	Default	Description	Notes
7-3	R/W	Reserved	0000	Reserved	
2	W1C	RESET	0	Set this bit to 1 to reset all registers to default values. This bit resets to 0 automatically after being written to 1.	
1	R/W	Reserved	0	Reserved	
0	W1C	Short_RST	0	Set this bit to 1 to recover the IC from latch off status after short circuit protection. This bit resets to 0 automatically after being written to 1.	

Table 16 0x0D Loop_STA Register ([go back to map](#))

Bit	Type	Bit Name	Default	Description	Notes
7-4	R	Reserved	0000	Reserved	
3	R	IBAT_Loop	0	0:normal 1: in IBAT_LIM regulation (no matter charging mode or discharging mode)	Just for rough indication

2	R	VINREG_Loop	0	0:normal 1: in VINREG regulation	Just for rough indication
1	R	CC_Loop	0	0:normal 1: in IBUS_LIM regulation (no matter charging mode or discharging mode)	Just for rough indication
0	R	CV_Loop	0	0:normal 1: in VBAT regulation for charging mode, in VBUS regulation for discharging mode	Just for rough indication

Table 17 0x0E STA1 Register ([go back to map](#))

Bit	Type	Bit Name	Default	Description	Notes
7-6	R	Reserved	00	Reserved	
5	R	OTP	0	0:normal 1: in OTP protection	
4	R	NTC_hot	0	0: normal 1: the temperature sensed by NTC pin is within hot zone (beyond 60°C for discharging mode or 45°C for charging mode under recommended NTC setup condition)	
3	R	NTC_cool_ch	0	0: normal 1: the temperature sensed by NTC pin is within cool zone for charging mode (0°C ~10°C under recommended NTC setup condition)	
2	R	NTC_cold	0	0: normal 1: the temperature sensed by NTC pin is within cold zone (below -20°C for discharging mode or 0°C for charging mode under recommended NTC setup condition)	
1	R	EOC	0	0: normal 1: the end of charge conditions are detected. Whether the IC terminates charging depends on DIS_TERM bit	
0	R	ICOM	0	0: normal 1: the IBUS output current is detected lower than 50mA (typ.) in discharging mode	

Table 2 0x0F STA2 Register ([go back to map](#))

Bit	Type	Bit Name	Default	Description	Notes
7	R	Reserved	0	Reserved	
6	R	FB_SC	0	0: normal 1: FB pin short circuit to ground is detected when FB_SEL is set to 1 (external setting way)	

5	R	VBAT_OVP	0	0: normal 1: VBAT OVP status is detected no matter how EN_VBATOVP is set, effective for both charging and discharging mode	
4	R	Reserved	0	Reserved	
3	R	Reserved	0	Reserved	
2	R	Reserved	0	Reserved	
1	R	C_IN_UVP	0	0: normal 1: input under voltage status is detected for VC when C_DIR = 0	
0	R	B_IN_UVP	0	0: normal 1: input under voltage status is detected for VB when VB_SET = 0	

Table 19 0x10 INT Register ([go back to map](#))

Bit	Type	Bit Name	Default	Description	Notes
7-5	R	Reserved	000	Reserved	
4	R/C	VBUS_SHORT	0	0: normal 1: VBUS short circuit or under voltage status is detected for discharging mode or pass-through mode After being set, this bit is latched to 1 until reset by hiccup mode or Short_RST signal	
3	R	INDET_B	0	0: normal 1: phone insertion is detected at VB when VB_SET = 1	
2	R	INDET_A	0	0: normal 1: phone insertion is detected at VA	
1	R	VC_ACOK	0	0: normal 1: input voltage is good for VC when C_DIR = 0 Input voltage good means the port voltage is higher than V _{IN_ACOK} when EN_INUVP = 1	
0	R	VB_ACOK	0	0: normal 1: input voltage is good for VB when VB_SET = 0 Input voltage good means the port voltage is higher than V _{IN_ACOK} when EN_INUVP = 1	

Table 20 0x11 INT_MASK Register ([go back to map](#))

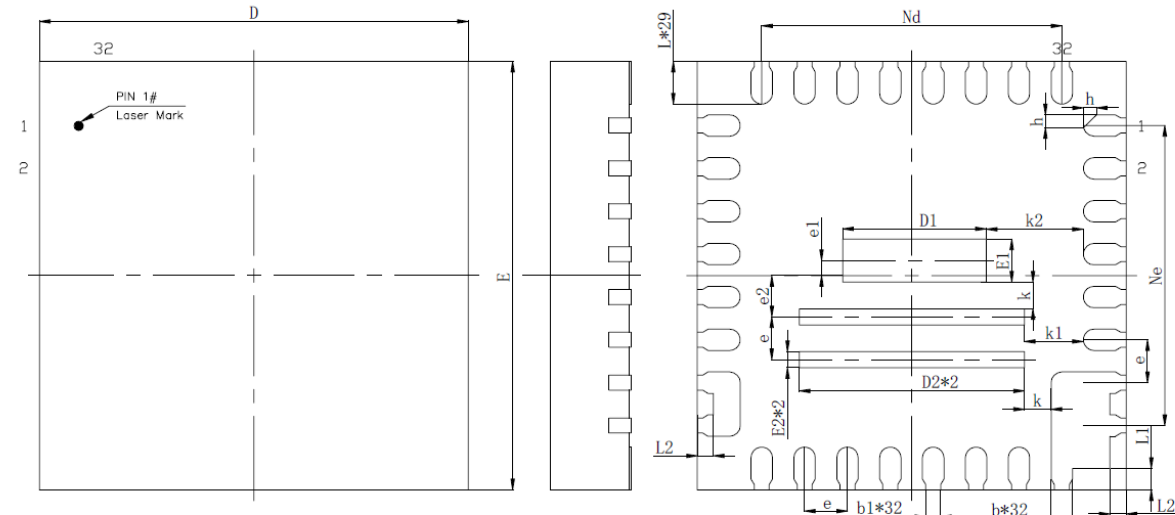
Bit	Type	Bit Name	Default	Description	Notes
7-5	R/W	Reserved	000	Reserved	
4	R/W	VBUS_SHORT_M	0	VBUS_SHORT INT mask 0: VBUS_SHORT bit rising edge generates an INT pulse (default) 1: VBUS_SHORT bit rising edge doesn't generate an INT pulse	

3	R/W	INDET_B_M	0	INDET_B INT mask 0: INDET_B bit rising edge generates an INT pulse (default) 1: INDET_B bit rising edge doesn't generate an INT pulse
2	R/W	INDET_A_M	0	INDET_A INT mask 0: INDET_A bit rising edge generates an INT pulse (default) 1: INDET_A bit rising edge doesn't generate an INT pulse
1	R/W	VC_ACOK_M	0	VC_ACOK INT mask 0: VC_ACOK bit toggle generates an INT pulse (default) 1: VC_ACOK bit toggle doesn't generate an INT pulse
0	R/W	VB_ACOK_M	0	VB_ACOK INT mask 0: VB_ACOK bit toggle generates an INT pulse (default) 1: VB_ACOK bit toggle doesn't generate an INT pulse

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MECHANICAL DATA

QFN-32L(4x4x0.75)



TOP VIEW

BOTTOM VIEW

SIDE VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.15	0.20	0.25
b1	0.14REF		
c	0.203REF		
D	3.90	4.00	4.10
D1	1.29	1.34	1.39
D2	2.05	2.10	2.15
Nd	2.80BSC		
e	0.40BSC		
e1	0.14BSC		
e2	0.385BSC		
E	3.90	4.00	4.10
E1	0.35	0.40	0.45
E2	0.10	0.15	0.20
Ne	2.80BSC		
L	0.35	0.40	0.45
L1	0.15	0.20	0.25
L2	0.10	0.15	0.20
h	0.12REF		
k	0.25REF		
k1	0.55REF		
k2	0.905REF		

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