High Efficiency, Synchronous Buck Charger for 1-4 cell Li-ion Battery with PowerPath management

1 DESCRIPTION

The SC89171 is a highly integrated switch-mode buck charger for 1-4 cells Li-ion battery applications. It supports 4-24V input, up to 5A charging current and provide battery charge management functions including trickle charge, constant current charge, constant voltage charge, charge termination, auto recharge and charging status indication.

SC89171 also integrates NMOS driver and PMOS driver for Powerpath management, it is easy to support dynamic power management for charging and system power.

The SC89171 supports flexible charge current and input current option, and the user can program the current freely through external resistor for different applications.

The SC89171 supports input current limit, input over voltage and under voltage protections, internal cycle by cycle current limit, battery short circuit protection, and battery over voltage protection. It also offers charging safety timer and battery temperature protection to ensure safety under different abnormal conditions.

Besides, SC89171 keeps monitoring IC temperature and automatically decreases charging current to ensure IC working in normal temperature range.

The SC89171 is available in QFN-3.5*5.5 package.

2 FEATURES

- Wide input voltage: 4V~24V, 30V sustainable
- Integrated low-Rdson synchronous buck charger, efficiency up to 97%
- Charging Management (Trickle Charge / Constant Current Charge / Constant Voltage Charge / Charge Termination/Auto-Recharge)
- Adjustable Input Current Limit and Charging Current
- Adjustable Constant Voltage by External Resistor setting
  - FB version: 2.1V for 1 to 4 cells battery
- Powerpath management for System Power Selector
- Battery Detection
- Adjustable Charge Safety Timer
- NTC supporting JEITA Standard for Battery temperature Protection
- Charging Status Indication
- Adjustable Input Over Voltage and Under Voltage Protection
- Battery Over Voltage Protection
- Battery Short Circuit Protection
- Charging Over Current and Under Current Protection
- Thermal Regulation and Shutdown
- QFN 3.5*5.5 footprint

3 APPLICATIONS

- Blue-tooth speaker charger
- Portable Media Players
- Notebook, Tablet
- POS machine

4 DEVICE INFORMATION

Part Number	Package	Dimension
SC89171QDNR	24 pin QFN	3.5mm x 5.5mm

5 Typical Application Circuit

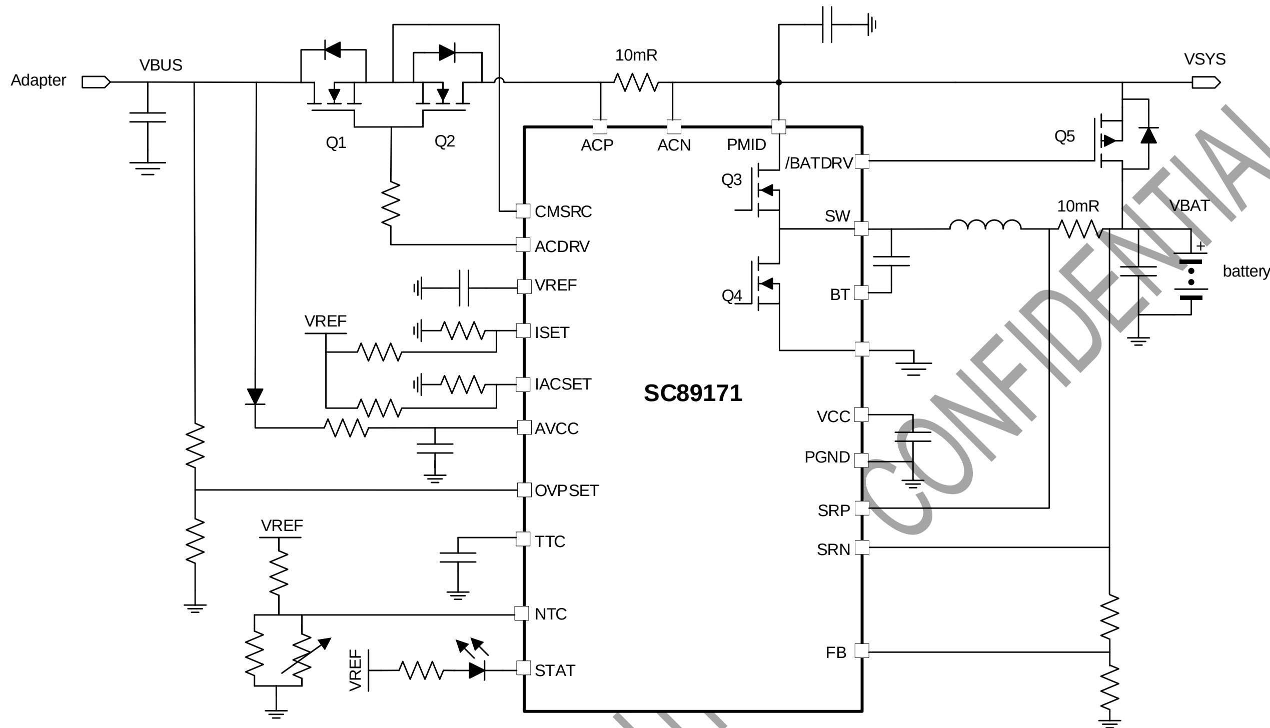


Figure 1. SC89171 with powerpath application

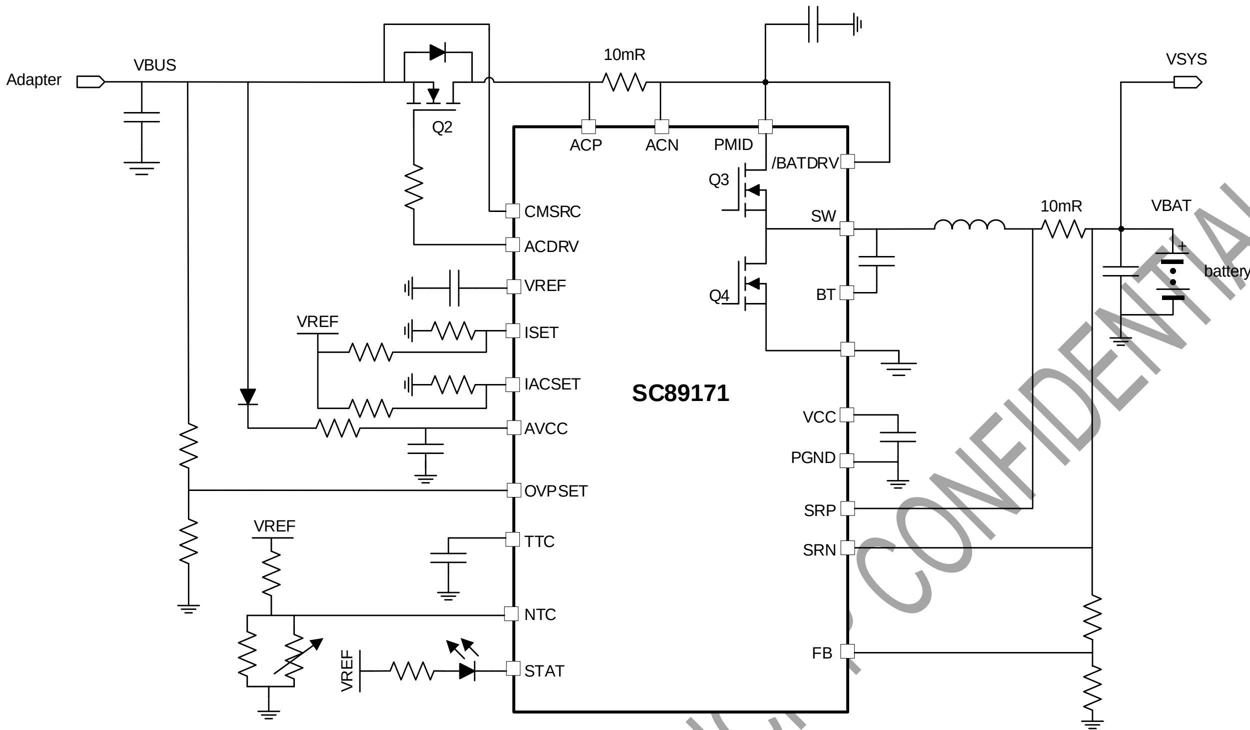
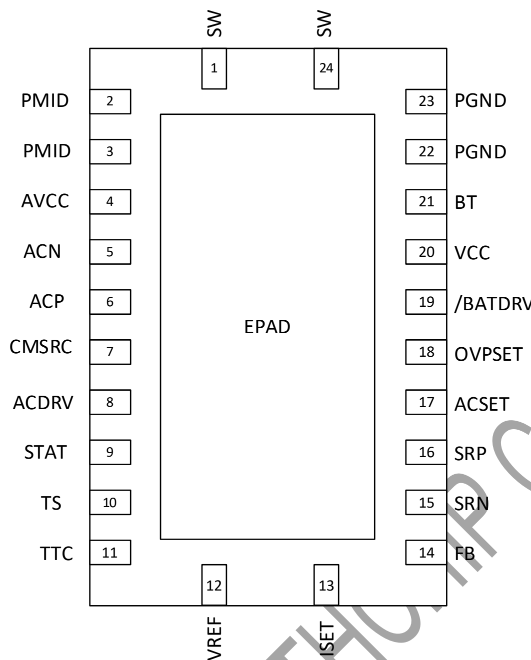


Figure 2. SC89171 without power path application

6 Terminal Configurations and Functions

QFN 3.5x 5.5



I/O			DESCRIPTION
SC89171	NAME		
1, 24	SW	I/O	Switching node of the boost converter. Connect to external inductor.
2, 3	PMID	I	Input of buck charger to charge the battery cells. Connected to the drain of the reverse blocking MOSFET.
4	AVCC	I	IC power positive supply. Place a 1-µF ceramic capacitor from AVCC to AGND and place it as close as possible to IC.
5	ACN	I	Adapter input current sense resistor negative input.
6	ACP	I	Adapter input current sense resistor positive input.
7	CMSRC	O	Connect to common source of ACFET and reverse blocking FET.
8	ACDRV	O	Blocking FET driver output. Connect to the gate of blocking FET.
9	STAT	O	Charge status indication. Open drain output. Connect it to pull-up,
10	TS	I	Temperature sense pin. Connect to the Negative Temperature Coefficient (NTC) thermistor inside the battery cells to sense the battery cells temperature for protection. Short this pin to ground to disable this function.
11	TTC	I	Safety Timer and termination control. Low: disable both safety timer and charge termination High: only disable safety timer
12	VREF	O	3.3-V reference voltage output. Place a 1-µF ceramic capacitor from VREF to AGND pin close to the IC.
13	ISET	I	Charging current setting pin.
14	FB	I	Battery charge voltage feedback pin, internal reference is 2.1V.
15	SRN	I	Charging current sense resistor negative input.
16	SRP	I	Charging current sense resistor positive input.
17	IACSET	I	Adapter input current limit setting pin.
18	OVPSET	I	Adapter input voltage setting pin. Connected with a resistor divider from VBUS to AGND

			to set charger working range.
19	/BATDRV	O	BATFET gate driver output.
20	VCC	O	Internal LDO output. Connect a 1uF capacitor with it.
21	BT	O	Bootstrap pin. Connect a 100nF ceramic capacitor between BT pin and SW pin to provide bias voltage for internal driver circuit.
22, 23	PGND	O	power ground.
25	AGND	I/O	Exposed thermal pad. Connected with power ground through vias.

7 Specification

7.1 Absolute Maximum Rating

Over operating free-air temperature range (unless otherwise noted)(1)

		Min.	Max.	Unit
Voltage(2)	AVCC, ACP, ACN, ACDRV, CMSRC, STAT	-0.3	30	V
	SRP, SRN, PMID, FB, /BATDRV	-0.3	25	V
	BT	-0.3	31	V
	SW	-2(10ns)	25	V
	VCC	-0.3	6.5	V
	OVPSET, NTC, TTC, VREF, ISET, IACSET	-0.3	6.5	V
T_J	Operating junction temperature	-40	155	°C
T_{stg}	Storage temperature	-65	155	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device.
(2) All voltages are with respect to network ground terminal.

7.2 Thermal Information(TBD)

THERMAL RESISTANCE(1)		QFN (3.5mmX5.5mm)	Unit
θ_{JA}	Junction to ambient thermal resistance	36	°C/W
θ_{JC}	Junction to case resistance	7	°C/W

(1) Measured on JESD51-7, 4-layer PCB.

7.3 ESD Ratings

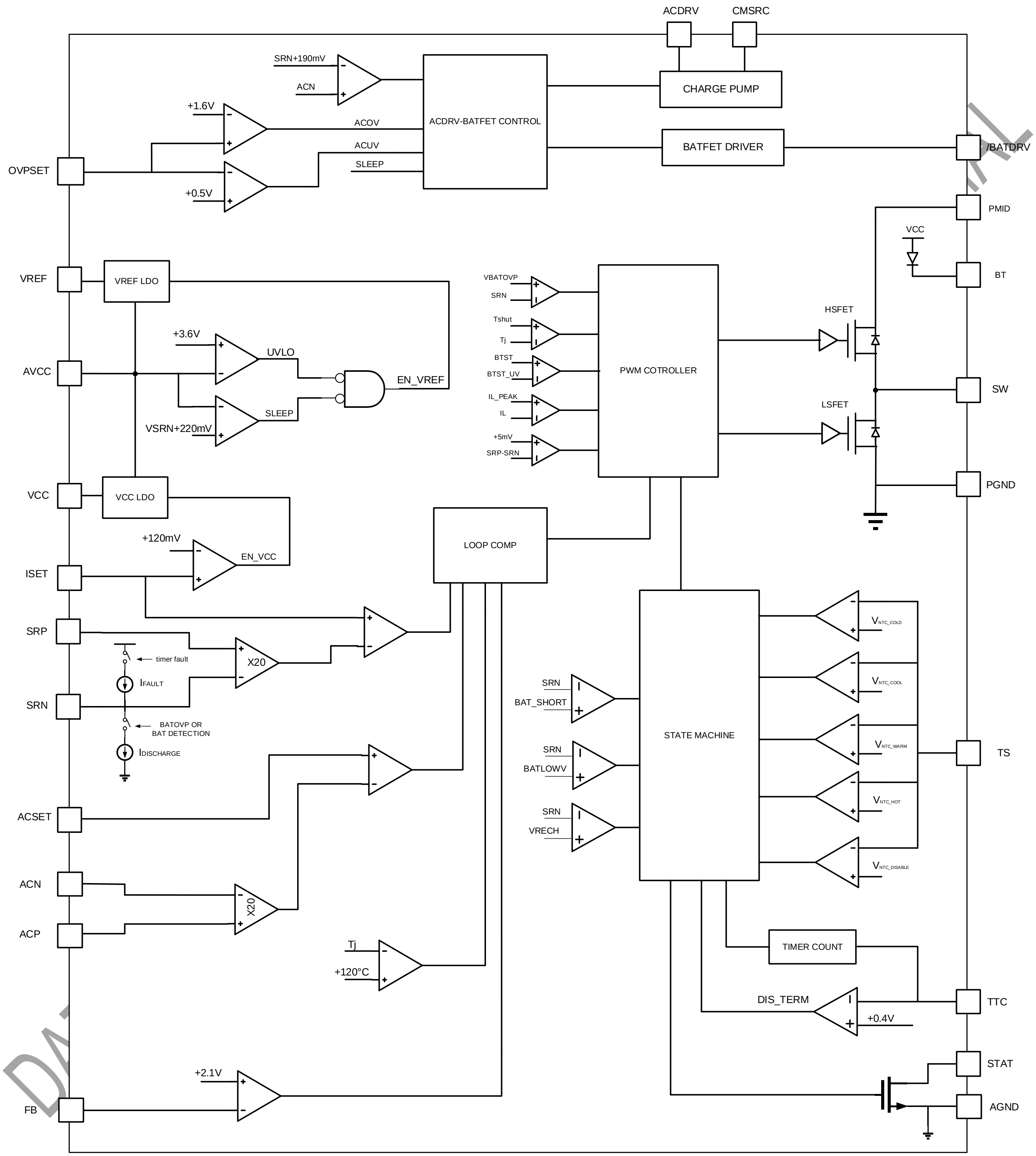
			Min.	Max.	Unit
V_{ESD}(1)	Human-body Model (HBM) (2)	All pins	-2	2	kV
	Charged-device Model (CDM) (3)		-750	750	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.
(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.4 Recommended Operation Conditions

		MIN	TYP	MAX	UNIT
V_{BUS}	VBUS voltage range	4		24	V
V_{PMID}	PMID voltage range			24	V
V_{BAT}	VBAT voltage range			17.6	V
L	Inductance	2.2	3.3		µH
RS1	Input current sense resistor	5	10		mΩ
RS2	Charging current sense resistor	5	10		mΩ
T_A	Operating ambient temperature	-40		85	°C
T_J	Operating junction temperature	-40		125	°C

8 Function Block Diagram



9 Electrical Characteristics (TBD)

4.5V≤ (PVCC, AVCC) ≤24V, –40°C<T_J< +125°C, typical values are at T_A= 25°C, T_A= 25°C unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
V_{AVCC_UVLO}	input under-voltage lockout threshold	Rising edge		3.6		V
		Hysteresis		200		mV
I_{Q_AVCC}	Quiescent current into AVCC	V_{AVCC}>V_{UVLO}, V_{AVCC} > V_{SRN}, V_{ISET}< 40mV, VBAT=16.8V, charger disabled		45	100	µA
		V_{AVCC} > V_{UVLO}, V_{AVCC} > V_{SRN}, V_{ISET} > 120mV, charger enabled, no switching			2	mA
		V_{AVCC} > V_{UVLO}, V_{AVCC} > V_{SRN}, V_{ISET}>120 mV, charger enabled, switching		5		mA
I_{Q_VBAT}	Quiescent current into SRN	V_{AVCC} > V_{UVLO}, V_{SRN} > V_{AVCC} (sleep mode), VBAT=16.8V, 4cells			15	µA
		V_{AVCC} > V_{UVLO}, V_{AVCC}> V_{SRN}, V_{ISET} < 40mV, VBAT=16.8V, Charge disabled			15	µA
		V_{AVCC} > V_{UVLO}, V_{AVCC}> V_{SRN}, V_{ISET} > 120mV, VBAT=16.8V, 4cells, charge termination		17	25	µA
POWERPATH						
V_{SLEEP}	Sleep mode threshold	VAVCC – VSRN falling		160		mV
		VAVCC – VSRN rising		220		mV
$V_{ACN\text{-}SRN}$	Threshold to turn on BATFET	VACN – VSRN falling		190		mV
	Hysteresis threshold to turn off BATFET	VACN – VSRN rising		280		mV
POWER STAGE						
R_{dson_HS}	Rdson resistance of high side FET			22		mΩ
R_{dson_LS}	Rdson resistance of low side FET			35		mΩ
F_{sw}	Switching frequency			1200		kHz
$V_{BT\_REFRESH}$	Bootstrap refresh comparator threshold voltage		3			V
VREF						
V_{REF}	V_{REF} output voltage	V_{AVCC} > V_{AVCC_UVLO}, No load	3.267	3.3	3.333	V
I_{VREF}	V_{REF} current limit	V_{REF} = 0 V, V_{AVCC} > V_{UVLO}		60	80	mA
VCC DRIVER						
V_{CC}	VCC output voltage	V_{AVCC}= 12V, I_{VCC} = 1~70mA	4.9	5.0	5.1	V
I_{VCC}	VCC current limit	VREGN = 0 V, VAVCC > 10V, ISET > 120 mV			120	mA

ACDRV DRIVER						
I_{ACFET}	ACDRV charge pump current limit	VACDRV - VCMSRC = 2 V		60		µA
V_{ACFET}	Gate drive voltage on ACFET	VACDRV - VCMSRC when VAVCC > VUVLO		4.8		V
BATFET DRIVER						
$R_{DS\_BAT\_OFF}$	BATFET turnoff resistance			50		Ω
$R_{DS\_BAT\_ON}$	BATFET turn-on resistance			16		kΩ
V_{BATDRV}	BATFET drive voltage	VBATDRV= VACN - VBATDRV when VAVCC > 9V and BATFET is on		6		V
INPUT CURRENT LIMIT						
K_{IDPM}	input current limit factor	RS1 = 10mΩ		5		A/V
I_{BUS}	Input current accuracy	RS1* IBUS=80mV	-2		2	%
		RS1* IBUS=40mV	-3		3	%
		RS1* IBUS=20mV	-5		5	%
		RS1* IBUS=10mV	-5		5	%
		RS1* IBUS=5mV	-10		10	%
		RS1* IBUS=2.5mV	-25		25	%
I_{ACSET_LEAK}	Leakage current into ACSET pin				10	nA
CHARGER FUNCTION						
V_{CHG}	Charge disable threshold	ISET falling	40	50		mV
	Charge enable threshold	ISET rising		100	120	mV
K_{ICHG}	Charge current limit factor	RS2 = 10mΩ		5		A/V
I_{CHG}	Charge constant current accuracy	RS2* IBUS=40mV	-3		3	%
		RS2* IBUS=20mV	-5		5	%
		RS2* IBUS=10mV	-5		5	%
		RS2* IBUS=5mV	-10		10	%
I_{ISET_LEAK}	Leakage current into ISET pin				10	nA
K_{ITRK}	Trickle charging current ratio, respect to ICHG			10%		
I_{TRK}	Trickle charging current accuracy	RS2* ICHG=4mV	-15		15	%
		RS2* ICHG=2mV	-25		25	%
K_{ITERM}	Termination charging current ratio, respect to ICHG			10%		
I_{TERM}	Termination charging current accuracy	RS2* ICHG=4mV	-15		15	%
		RS2* ICHG=2mV	-40		40	%
V_{BAT_TRGT}	VBAT target voltage	FB voltage	2.089	2.1	2.111	V
V_{BAT_RECH}	Recharge threshold over VBAT target voltage	FB voltage		50		mV
t_{RECH_dgl}	Recharge deglitch time			10		ms

V_{BAT_TRK}	Trickle charge threshold	Rising edge		1.45		V
		Falling hysteresis		100		mV
t_{TRK_CC}	Trickle charge to CC charge deglitch			25		ms
V_{BAT_SHORT}	Battery short threshold	Falling, Measure on SRN		2		V
		Rising hysteresis		200		mV
I_{SHORT}		V_{BAT}<V_{BAT_SHORT}		100		mA
$t_{BATSHORT\_dgl}$	Deglitch on both edges			1		us
Safety timer						
K_{Timer_TRK}	Trickle charge timer factor			0.3		min/nF
t_{TRK}	Trickle charge timer	C_{TTC}=100nF		30		min
K_{timer_CC}	Trickle charge timer factor			6		min/nF
t_{CC}	Trickle charge timer	C_{TTC}=100nF		10		H
V_{TTC_LOW}	TTC pin low threshold				0.4	V
I_{TTC}	TTC source/sink current			5		μA
Battery Detection						
t_{WAKE}	Wake timer	Max time charge is enabled		500		ms
I_{WAKE}	Wake current	RS2 = 10mΩ	50	125	200	mA
$t_{Discharge}$	Discharge timer	Max time discharge current is applied		1		s
$I_{Dischage}$	Discharge current			10		mA
I_{FAULT}	Charge current after a time-out fault			2		mA
V_{Wake}	Wake threshold to trigger battery detection	Measure on FB		2.05		V
V_{DISCH}	Discharge threshold to detect battery absent	Measure on FB		1.5		V
Protection						
V_{ACOV}	Overvoltage rising threshold to turn off ACFET	OVPSET rising		1.6		V
		Falling hysteresis		50		mV
t_{ACOV_dgl}	Overvoltage rising deglitch	Rising edge		120		ns
		Falling edge		30		ms
V_{ACUV}	Undervoltage falling threshold to turn off ACFET	OVPSET falling		0.5		V
		Rising hysteresis		50		mV
t_{ACOV_dgl}	Undervoltage falling deglitch	Falling edge		40		ns
		Rising edge		30		ms
I_{LIM_PK}	Peak current limit			9		A
V_{BATOVP}	VBAT over voltage protection	Rising edge, over VBAT target		104		%
		Hysteresis, over VBAT target		2		%
I_{BATOVP_DSG}	VBAT over voltage discharge current	VBAT=4.6V		5		mA

NTC						
V_{COLD}	NTC cold temp threshold, refer to V_{REF}	Rising	70.3	70.8	71.3	%
		Falling hysteresis		0.6		%
V_{COOL}	NTC cool temp threshold, refer to V_{REF}	Rising	68.1	68.6	69.1	%
		Falling hysteresis		0.6		%
V_{WARM}	NTC warm temp threshold, refer to V_{REF}	Falling	55.6	56.1	56.6	%
		Falling hysteresis		0.9		%
V_{HOT}	NTC hot temp threshold, refer to V_{REF}	Falling	47.6	48.1	48.6	%
		Rising hysteresis		0.9		%
V_{DISNTC}	Disable NTC threshold, refer to V_{REF}	Falling		5		%
t_{NTC_dgl}	NTC status deglitch time	for NTC enter hot and cold		64		ms
		quit hot or cold		4		ms
STAT						
$STAT_{LO}$	STAT output low saturation voltage	Sink current = 5 mA			0.5	V
STARTUP						
t_D	Input delay time			5		µs
$t_{DEBOUNCE}$	Input debounce time			1.5		s
THERMAL REGULATION AND SHUTDOWN						
T_{REG}	Thermal loop regulation temperature			120		°C
T_{SD}	Thermal shutdown temperature	Rising edge		150		°C
		Hysteresis		20		°C
t_{SD_dgl}	Thermal shutdown rising deglitch	Rising edge		100		µs
	Thermal shutdown falling deglitch	Hysteresis		10		ms

10 Feature Description

10.1 Power Up

SC89171 is powered up when AVCC is above V_{UVLO} threshold. AVCC is supplied by adapter or battery internally. IC will start charging cycle if IC exits sleep mode.

10.2 Sleep Mode

if V_{AVCC} is above V_{UVLO} but V_{AVCC}<V_{SRN}+160mV, SC89171 enters sleep mode to minimize current drain from the battery. In sleep mode, V_{REF} is disabled and charger is disabled, the STAT pin goes to high impedance.

10.3 VREF LDO

SC89171 integrates a 3.3V VREF LDO to provide reference voltage for input current limit and charge current setting. When AVCC is above UVLO and IC is not into sleep mode, the VREF LDO is initialed.

10.4 VCC driver

SC89171 integrates 5V VCC LDO to provider power for switching MOSFET driver. VCC is initiated when V_{ISET}>120mV and AVCC is powered up.

SC89171 enters standby mode when V_{ISET}<120mV, VCC is disabled, charger is disabled.

10.5 Powerpath management

System power is switched from adapter or battery automatically. During sleep mode such as only battery exists, the BATFET is turned on to provide power from battery.

When adapter plugs in, SC89171 exits sleep mode, BATFET switches off and ACFET is turned on to provide power path from adapter to system.

When adapter is removed or an OV adapter plug-in, ACFET is turned off, then BATFET is turned on to supply system from battery.

10.6 Charge management

The SC89171 provides charge management functions for 1-4 cell Li-ion battery. The typical charge profile is shown in Figure 3.

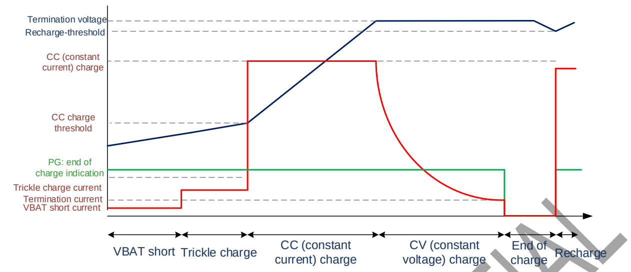


Figure 3. Typical charge profile

Charger cycle starts when following conditions is satisfied:

(1) ISET pin above 120 mV.
(2) Not in UVLO mode (V_{AVCC}> V_{UVLO}).
(3) Not in SLEEP mode (V_{AVCC} > V_{SRN}).
(4) Not in ACOV or ACUV mode. (0.5 V< V_{OVPSET} <1.6 V)
(5) 1.5s delay is complete after initial power up.
(6) VCC LDO and VREF LDO voltages are at correct levels.
(7) Thermal shut down is not valid.
(8) TS fault is not detected.
(9) ACFET turns on
(10) No safety timer is triggered

10.6.1 Battery Detection

When AVCC power on or VBAT falls down <V_{RECH} (battery recharge voltage), IC initials a battery detection flow.

Step1: POR and VBAT < recharge voltage is triggered.

Step2: 8mA discharge current from SRN to GND and 1s timer starts. If V_{BAT} > V_{LOWV} and 1s timer expires, battery is present and IC start charging. Otherwise battery is absent, then go to next step.

Step3: 125mA charging current to VBAT and 500ms timer starts. If V_{BAT} < V_{LOWV} and lasting for 500ms, battery is present and IC start charging. Otherwise battery is absent, STAT pin is blinking, then repeat the battery detection cycle.

10.6.2 Trickle current Charge

When VBAT is lower than V_{TRK} (trickle charge threshold), the SC89171 charges the battery cells in trickle charge mode. In this mode, the charge current is regulated at 1/10 of the constant charge current programmed by ICHG pin resistor.

If the 1/10 of the CC current is lower than 120mA, the trickle charge current will be clamped to 120mA. the trickle charge current is set as 10% of the fast charge rate set by ICHG voltage.

$$I_{TRKLE} = \frac{V_{ISET}}{200 \times RS2}$$

10.6.3 Constant Current (CC) Charge

When VBAT voltage is charged above V_{TRK}, the SC89171 enters into constant charge (CC) mode.

In this mode, the IC regulates VBAT sense current, and control the charging current at ICHG decided by ICHG pin. Use a voltage divider from VREF to ICHG to AGND to set the fast charge current:

$$I_{CC} = \frac{V_{ISET}}{20 \times RS2}$$

The charger is disabled when ICHG pin voltage is below 40 mV and enabled when ICHG pin voltage is above 120 mV. ICHG can be used as chip enable pin.

10.6.4 Constant Voltage (CV) Charge

The SC89171 operates in constant voltage (CV) mode after VBAT exceeds 98% of the termination voltage target VBAT_TRGT. In CV mode, the battery voltage is regulated at VBAT_TRGT. The charge current automatically drops until the battery is fully charged.

The battery target voltage can be configured through FB pin voltage. Below table shows the relationship between the FB setting and the VBAT target voltage.

$$\text{CV target} = V_{FB} \times \left[1 + \frac{R2}{R1}\right]$$

Where,

VFB is the internal reference voltage, 2.1V.

R1 and R2 is the resistor divider of VBAT.

10.6.5 Charge Termination / End of Charge

When below conditions are valid, the SC89171 recognizes the battery cells are fully charged:

1) Termination voltage: the VBAT voltage is higher than 98% of VBAT_TRGT

2) Termination current: the charge current is less than termination current.

$$I_{TERM} = \frac{V_{ISET}}{200 \times RS2}$$

3) above two conditions are met together and with 500ms deglitch time

When batteries are fully charged, the SC89171 outputs floating at STAT pin, so the LED connected at STAT pin is off, indicating the end of charge (EOC). EOC is disabled when IC is in IINDPM or thermal regulation.

In EOC phase, the IC stops charging, ACFET is still turned on to provide power from adapter to system.

10.6.6 Recharge

After EOC, the SC89171 still monitors VBAT voltage. Once it detects the battery voltage falls below 96% of VBAT_TRGT, it turns on charger and returns to CC mode with soft start again.

10.7 Charging Status Indication

When the SC89171 charges the battery in trickle charge/CC charge/CV charge mode, the STAT pin outputs logic high, so the LED connected at STAT pin is turned on, indicating the charging is in process.

After the EOC conditions are met, the STAT pin outputs high impedance, indicating the battery cells are fully charged.

If the battery voltage drops below the recharge threshold V_{RECH}, the LED will be turned on again.

When fault happens, the STAT outputs high and low at 0.5Hz frequency.

The charging status is as follow:

Table 1 STAT pin and working status

STAT status	IC working status
ON	Normal charging (VBAT short/ TC /CC /CV /Recharge)
OFF	End of charging (EOC)/Sleep mode/ charger disable
0.5Hz blinking	Abnormal charging（ACOV/ACUV/ Safety timer triggered/ /NTC_HOT/ NTC_COLD /Tshut/battery Absent)

10.8 Input Current Limit

the SC89171 supports input current limit function. The input limit is set by voltage of IIN pin.

$$IBUS = \frac{VACSET}{20 \text{ x } RS1}$$

Where,

IBUS is the input limit current.

V_{ACSET} is the voltage of ACSET pin, connected with resistor divider from VREF to AGND.

RS1 is the current sense resistor of input current of IBUS.

10.9 NTC

The SC89171 integrates JEITA standard NTC pin to support battery temperature protection function. Once SC89171 exits sleep mode, it keeps monitoring the battery cells' temperature through NTC pin and compares with V_{REF} voltage. When NTC faults (NTC hot or NTC cold) happens, the charger suspends, and the STAT starts blinking to alarm host. Only when NTC fault disappears，SC89171 resume charging after 40ms deglitch.

Below shows the NTC operation summary. NTC function can be also disabled through shorting the pin to ground.

Table 2 NTC operation

V_{NTC}	Operation
$V_{NTC} > V_{COLD}$	Stop charging
$V_{COLD} > V_{NTC} > V_{COOL}$	0.5*Charging Current
$V_{COOL} > V_{NTC} > V_{WARM}$	Normal charging
$V_{WARM} > V_{NTC} > V_{HOT}$	Constant Voltage -100mV
$V_{HOT} > V_{NTC} > V_{DISNTC}$	Stop charging
$V_{DISNTC} > V_{NTC} >=0$	Disable NTC

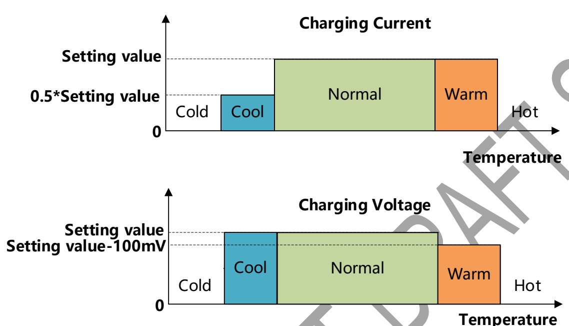


Figure 4. NTC Operation

SC89171 supports JEITA standard, IC monitors the voltage of NTC pin to check the temperature of battery. when IC detects the battery is in Cool State, it will decrease the constant charge current to be half of original value. Meanwhile, when IC detects the battery is in Warm State, the constant voltage decrease 100mV lower than setting battery charging voltage.

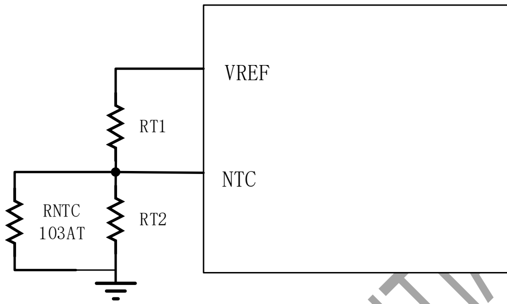


Figure 5. NTC Circuit

Use below equations to calculate the RT1/RT2 resistance when a 103AT NTC thermistor is used as shown in Figure 5.

$$R_{T2} = \frac{R_{COLD} \times R_{HOT} \times (\frac{1}{V_{COLD}} - \frac{1}{V_{HOT}})}{R_{HOT} \times (\frac{1}{V_{HOT}} - 1) - R_{COLD} \times (\frac{1}{V_{COLD}} - 1)}$$

$$R_{T1} = \frac{\frac{1}{V_{COLD}} - 1}{\frac{1}{R_{T2}} + \frac{1}{R_{COLD}}}$$

Where, R_{HOT} is the NTC resistance at the hot temperature threshold, R_{COLD} is the resistance at the cold threshold.

For example, set 0 °C(cold) to 60 °C (hot) to be the charging range. So R_{COLD} = 28.71 KΩ, R_{HOT} =2.99 KΩ (resistance of 103AT thermistor at 0°C and 60°C)

So the calculation results are:

R_{T1}=2.22 KΩ, R_{T2}=6.64 KΩ;

With above setting, the cool temperature and warm temperature are 10 °C and 45 °C.

10.10 Input Undervoltage Lockout

When AVCC voltage is above V_{UVLO} voltage, the IC is enabled to allow proper operation. If AVCC falls below UVLO voltage, the IC is disabled.

10.11 Input Over and Under Voltage Protection

The SC89171 supports input over and under voltage protection. Once the IC detects the OVPSET pin voltage is above 1.6V or is below 0.5V, it enters into over voltage protection or under voltage protection. SC89171 will stop switching instantly, ACFET is turned off to avoid abnormal adapter plug-in and BATFET is turned on to supply system from battery. At the same time, STAT pin blinks at 0.5Hz to indicate fault.

10.12 VBAT Over Voltage Protection

The SC89171 monitors VBAT voltage during the operation. Once it detects the VBAT is higher than 104% of the target voltage, over voltage protection is triggered and the IC stops switching at once, A 6mA discharging current path from SRP/SRN to AGND. the high-side FET is not turned on until the battery voltage goes below 102%. If battery overvoltage condition lasts for more than 30ms, charger is disabled.

10.13 VBAT Short Circuit Protection

Once the IC detects the VBAT voltage drops below V_{BAT_SHORT}, the VBAT short circuit protection is triggered. The IC regulates the short current to about 100mA.

After the short circuit fault is removed, the VBAT voltage is charged up. When VBAT voltage is higher than the short circuit threshold, the IC returns to normal operation.

10.14 Charging Over current Protection

The SC89171 monitor the peak inductor current cycle by cycle, it will clamp the peak inductor current to be about 9A.

10.15 Charging Under current Protection

When SRP-SRN voltage decreases below 5mV, the low-side FET is turned off for the rest of the switching cycle. IC Working in DCM mode. During discontinuous conduction mode, the low-side FET turns on for a short period of time when the bootstrap capacitor voltage drops below 4 V to provide refresh charge for the capacitor.

10.16 MOSFET Short Circuit and Inductor Short Circuit Protection

SC89171 integrates cycle by cycle current monitoring feature. it is achieved through monitoring the voltage drop across R_{dson} of the MOSFETs. The charger will be latched off, but the ACFET is turned on to power the system. STAT is blinking at 0.5Hz. Remove adapter then plug adapter in again

10.17 Safety Timer

SC89171 integrates internal timer to avoid over-time charging. safety timer in trickle charge phases is fixed 30 minutes. When SC89171 enters into constant current charge phase, safety timer is programmed by the capacitor connected between the TIM pin and AGND, and is given by the formula:

$$t = C_{TTC} \times K_{TTC}$$

Where,

K_{TTC} = 6min/nF for fast charge phase (including CC and CV phase), 0.3min/nF for trickle charge phase.

C_{TTC} is the capacitor connected to TTC pin.

For C_{TTC}= 100nF typical application, the safety timer is 10 hours for fast charge phase. The safety timer is 30min for trickle charge phase.

TTC pin can be also used for mode selection function. Pull the TIM pin to AGND to disable both termination and fast charge safety timer. Pull the TTC pin to VREF to disable the safety timer but allow charge termination.

When the IC detects EOC condition, the IC clears the timer, and it does not restart the timer unless recharge phase starts, VBUS toggle happens or ISET pin toggles.

When IC enters VINREG, IDPM and thermal regulation, the timer related safety timer counting rate is slowed.

If the charging cycle does not end when the timer expires, SC89171 will transition to shutdown mode. The STAT starts blinking at 0.5Hz to indicate fault. SC89171 provides two Recovery ways to deal with timer fault according to battery voltage.

Condition 1: VBAT > V_{RECH} and safety timer is triggered.

Recovery Method: VBAT<V_{RECH} will clear the timer fault and battery detection will begin. A POR or taking ICHG below 40 mV will also clear the fault.

Condition 2: VBAT < V_{RECH} and safety timer is triggered.

2mA charging current (typ) is used to detect a battery removal condition and remains on as long as the battery voltage stays below the recharge threshold. If battery is removed, VBAT>V_{RECH}, 2mA charging current is disabled, and executes the recovery method in condition 1.

10.18 Thermal Regulation and Shutdown

In charging process, SC89171 keeps monitoring junction temperature. When IC detects Tj >120°C, it enters into thermal regulation loop and charging current is decreased gradually. If Tj still exceeds 120°C, charging current can be decreased to 0.

Once the SC89171 detects the junction temperature rises above 150°C, it shuts down the whole chip. When the temperature falls below 130°C, the chip is enabled again.

11 Application information(TBD)

11.1 Input and Output Capacitor

The input current of the Buck converter is discontinuously, and the input capacitor should be carefully selected. The ripple current through input capacitor can be calculated as:

$$I_{RMS}=I_{CC}\sqrt{\frac{V_{BAT}}{V_{IN}}(1-\frac{V_{BAT}}{V_{IN}})}$$

where the I_{CC} is battery charging current, the V_{IN} is the input voltage (V_{BUS} or P_{MID}), V_{BAT} is the battery voltage. Since MLCC ceramic capacitor has good high frequency filtering and low ESR, X5R or X7R capacitors are recommended for input capacitors. Three 10uF input capacitors in PMID is enough for most applications.

The output voltage ripple of output capacitor can be calculated as:

$$V_{RIPPLE}=\frac{V_{BAT}}{f_{sw}\cdot L}(C_{ESR}+\frac{1}{8\cdot f_{sw}\cdot C_{OUT}})(1-\frac{V_{BAT}}{V_{IN}})$$

Where the f_{sw} is the switching frequency, C_{ESR} is the ESR of output capacitor. Also, X5R or X7R MLCC capacitors are recommended for output capacitors. 2x10uF output capacitors is enough for most applications.

MLCC capacitor of small package size normally has better high frequency filtering, so a 1 µF MLCC of 0402 package size is highly recommended to added in parallel and put as close to VBUS and PMID pin as possible.

When selecting capacitors, the degrading effect of MLCC effective capacitance under DC bias must be considered. Ceramic capacitors can lose most capacitance at rated voltage. If the highest operating VBUS voltage is 12V, 25V voltage rating capacitor is recommended. Check the effective capacitance at the operating voltage to make sure the voltage ripple can be maintained.

11.2 Inductor Selection

2.2µH ~ 3.3 µH inductor is recommended for loop stability.

The peak inductor current in charging mode can be calculated as

$$IL_{peak} = I_{BAT} + \frac{V_{BAT}\cdot(V_{BUS}-V_{BAT})}{2\cdot f_{sw}\cdot L\cdot V_{BUS}\cdot \eta}$$

where IBAT is the battery charging current at VBAT side.

η is the power conversion efficiency. User can use 90% for calculation.

fsw is the switching frequency

L is the inductor value

When selecting inductor, the inductor saturation current must be higher than the peak inductor current with enough margin (20% margin is recommended). The rating current of the inductor must be higher than the battery current.

The inductor DC resistance value (DCR) affects the conduction loss of switching regulator, so low DCR inductor is recommended especially for high power application. The conductor loss of inductor can be calculated roughly as

$$PL\_DC = IL^2\cdot DCR$$

IL is the average value of inductor current, and it equals to IBAT.

Besides DC power loss, there are also inductor AC winding loss and inductor core loss, which are related to inductor peak current. Normally, higher peak current causes higher AC loss and core loss. The user shall consult with the inductor vendor to select the inductor which has small ESR at high frequency and small core loss.

11.3 Current Sense Resistor

10 mΩ should be used to sense IBAT current. Resistor of 1% or higher accuracy and low temperature coefficient is recommended. The resistor power rating and temperature coefficient should be considered. The power dissipation can be roughly calculated as $P=I^2R$, and I is the RMS current flowing through the resistor. The resistor power rating should be higher than the calculated value.

Normally the resistor value is varied if the temperature increased and the variation is decided by temperature coefficient. If high accuracy of current limit is required, select lower temperature coefficient resistor as much as possible.

11.4 SW Snubber Circuit

To adjust MOSFET switching time and switching overshoot for EMI debugging, it is recommended to add RC snubber (0603 size) circuit at SW, as shown in Figure 5.

The RC snubber is helpful in absorbing the high frequency spike at SW node, so to improve EMC performance. User can leave RC components as NC at the beginning and adjust the value to improve the EMC performance if necessary. Normally user can try 2.2Ω and 1nF for the snubber. If EMC should be improved further, reduce the resistor value (like 1Ω or even lower) and increase the capacitor value (like 2.2nF or even higher).

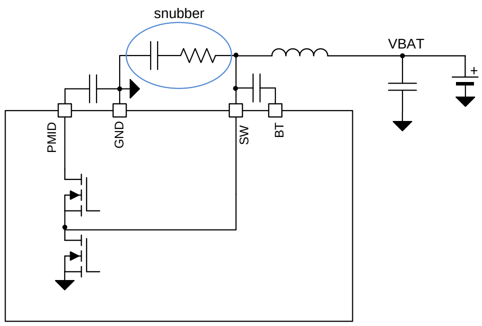


Figure 6. Snubber circuit

11.5 Layout Guide

1. The capacitors connected at VBUS/PMID/VBAT/VCC pins should be placed near the IC, and their ground connection to the ground pins should be as short as possible.
2. The current sense resistor should be close to the IC.The current sense traces should be connected to the current sense resistor's pads in Kelvin sense way as below, and routed in parallel (differential routing), and the filter for current sense should be placed near the IC.

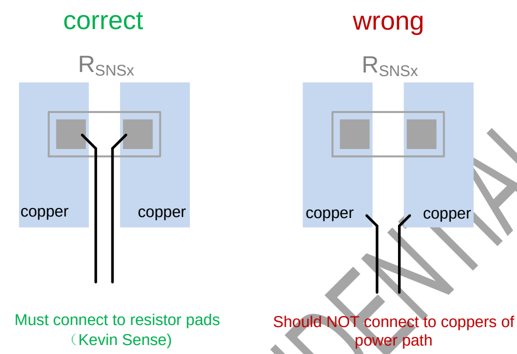
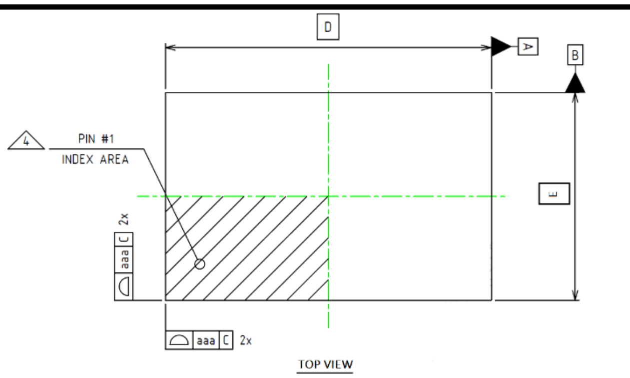


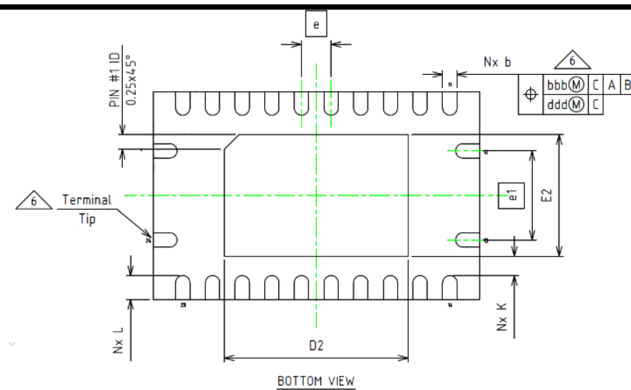
Figure 7. Current sense circuit

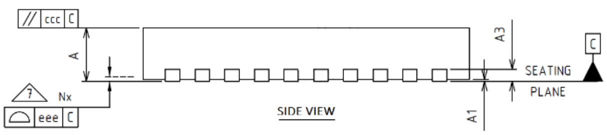
3. The AGND should be single connected to PGND close to IC.
4. The SW RC snubber circuit should be very close to IC SW and PGND pin.

MECHANICAL DATA

QFN (3.5mm x 5.5mm x 0.75mm)



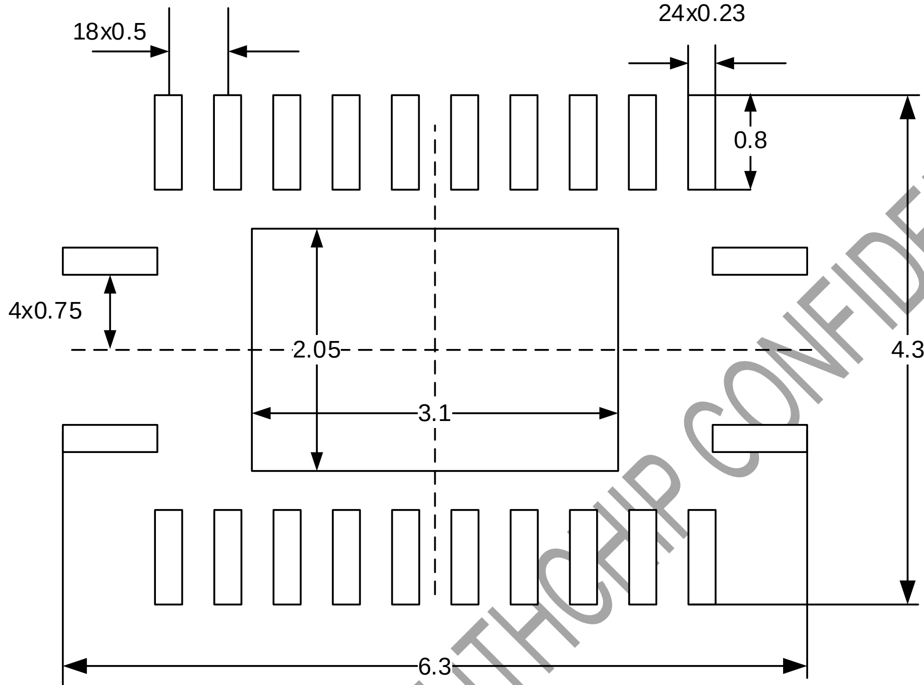




Dimension Table				
Thickness / Symbol	W			NOTE
	MINIMUM	NOMINAL	MAXIMUM	
A	0.70	0.75	0.80	
A1	0.00	0.02	0.05	
A3	---	0.20 Ref	---	
b	0.19	0.24	0.29	6
D	5.50 BSC			
E	3.50 BSC			
e	0.50 BSC			
e1	1.50 BSC			
D2	3.00	3.10	3.20	
E2	1.95	2.05	2.15	
K	0.20	---	---	
L	0.30	0.40	0.50	
aaa	0.05			
bbb	0.10			
ccc	0.10			
ddd	0.05			
eee	0.08			
N	24			3
ND	10			5
NE	2			5
NOTES	1, 2			
LF PART NO.	445431			

RECOMMENDED FOOTPRINT

QFN-24 (3.5x5.5x0.75) (Unit: mm)



Note:

A. All linear dimensions are in millimeters

B. Publication IPC-7351 is recommended for alternate designs

C. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad

单击下面可查看定价，库存，交付和生命周期等信息

[>>SOUTHCHIP(南芯)]