High Performance Fly-back Controller for USB-PD

1 Descriptions

SC3002 is a high performance, multi-mode fly-back PWM controller (CCM/QR/DCM).

SC3002 provides an adaptive switching frequency fold-back to achieve higher efficiency in the whole loading range. At heavy load or full load, it operates up to maximum switching frequency. When loading decreases, it operates in green mode with valley switching for high efficiency. And at no load, the IC will operate in Burst mode to reduce power consumption.

SC3002 provides functions of low start-up current, fast start-up, low standby power consumption. The burst mode with extremely low operation current (185uA) and significantly reduces standby power consumption to meet the efficiency regulations.

The controller integrates a segmented power supply control circuit, which is especially suitable for applications with a wide output voltage range, reducing power consumption and greatly reducing peripheral devices.

SC3002 integrated the adaptive over current protection (AOCP), which allows controlling the maximum output current from primary-side. The AOCP is specially designed for USB-PD solutions, together with PD controller, such as SC21xx serials. The AOCP can reduce the current stress of secondary synchronous rectification.

The SC3002 offers comprehensive protection to prevent the circuit from damage under abnormal conditions.

Furthermore, the features of frequency jittering and smart driving function can minimize the noise and improve EMI performance.

2 Features

- Internal soft start
- Integrated segmented power supply control circuit for extra-wide output range
- High Efficiency
  - CCM @ Heavy Load and Low Line
  - Valley switching operation @ Green mode
  - Burst Mode @ Light Load & No Load
- Ultra-low operation current @Burst mode/Fault Mode
- Adaptive over current protection
- Adaptive loop gain compensation
- Frequency Jitter for EMI improvement
- Driver capability: 300mA/-600mA
- Comprehensive Protection
  - VDD over voltage protection
  - VDD under voltage protection
  - Cycle by cycle current limiting
  - Two level over current protection
  - Output over voltage protection
  - Output short protection
  - Over Load protection
  - Brown in/out with auto-recovery
- SOP8 package available

3 Applications

- USB-PD and QC Chargers
- AC-DC adapters for Portable Devices

4 Device Information

ORDER NUMBER	PACKAGE	BODY SIZE
SC3002XSEER	SOP8	6.0mm x 4.9mm x 1.55mm

SC3002XSEER Functional Table

ORDER NUMBER	SC3002A	SC3002B	SC3002C	SC3002D	SC3002E
Maximum Frequency	67KHz	85KHz	100KHz	67KHz	85KHz
AOCP	A	A	A	/	/
Brown In/Out	A				
Valley Switching	Y				
Others Protections	A				

A: Auto-recovery;

Y: The feature is enabled

/ : The feature is not enabled

5 Typical Application Circuit

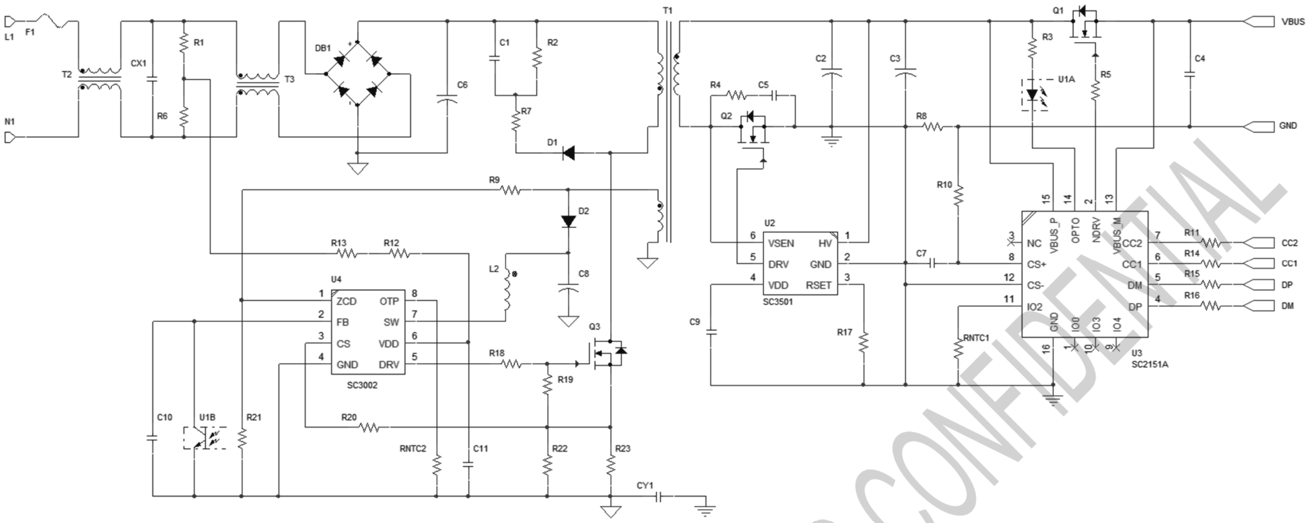


Fig. 1 Typical application circuit

6 Terminal Configuration and Functions

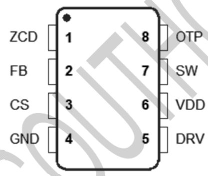


Fig. 2 Top view (SOP8)

TERMINAL		I/O	DESCRIPTION
SC3002	NAME		
1	ZCD	I	Voltage Sense. The ZCD voltage is used to detect resonant valleys for quasi-resonant switching. This pin detects the output voltage information and diode current discharge time based on the auxiliary winding voltage.
2	FB	I	Secondary side voltage feedback.
3	CS	I	Current Sense. This pin connects to a current-sense resistor to sense the MOSFET current for Peak-Current-Mode control for output regulation.
4	GND	PWR	Power Ground.
5	DRV	O	Totem-pole output to drive the external power MOSFET, Maximum Voltage is clamped to 12V internally.
6	VDD	PWR	Power Supply.
7	SW	PWR	Booster circuit switch control.
8	OTP	O	External OTP pin. This pin is typically connected to an NTC resistor.

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) [1]

Item	Description	Min.	Typ.	Max.	Unit
Voltage range at terminals [2]	VDD、SW to GND	-0.3	-	+40	V
	DRV to GND	-0.3	-	+20	V
	Other Pins to GND	-0.3	-	+6.5	V
T_J	Operating Junction temperature range	-40	-	150	°C
T_{stg}	Storage temperature range	-65	-	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

7.2 Thermal Information

THERMAL RESISTANCE [1]		SOP8 (6.0mm x 4.9mm)	UNIT
θ_{JA}	Junction to ambient thermal resistance	150	°C/W
θ_{JC}	Junction to case resistance	40	°C/W

(1) Measured on JESD51-7, 2-layer PCB.

7.3 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
ESD [1]	Human body model (HBM) ESD stress voltage [2]	-2	+2	kV
	Charged device model (CDM) ESD stress voltage [3]	-1	+1	kV

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.4 Recommended Operating Conditions

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDD to GND	VDD voltage range to GND	10		V_{DDOVP}	V
SW to GND	SW voltage range to GND		V_{DD}+0.7V	39	V
DRV to GND	DRV voltage range to GND	0		15	V
Others to GND	Other pins voltage range to GND	0		5.5	V
C_{VDD}	VDD Capacitor	2.2		22	uF
T_A	Operating ambient temperature	-40		85	°C
T_J	Operating junction temperature	-40		125	°C

7.5 Electrical Characteristics

VDD=15V, T_J= -40°C~125°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VDD)						
V_{DDON}	VDD on threshold voltage		15.4	16.2	17.0	V
V_{DDOFF}	VDD off threshold voltage		7.0	7.5	8.0	V
$V_{DDHOLDL}$	VDD holding entry point voltage			7.9		V
$V_{DDHOLDH}$	VDD holding exit point voltage			8.5		V
$V_{DDBSTOFF}$	Booster regulation voltage			10.0		V
$V_{DDBSTON}$	The booster circuit starts to work			8.5		V
I_{ST}	Startup current	VDD < V_{DDON} -1V		2.5	8.0	uA
I_{VDD}	Operating current	Cload = 1nF		2		mA
I_{VDDBT}	Burst mode current	V_{FB} < 0.5V		185	220	uA
$I_{VDDFAULT}$	Hold up current in fault mode			80		uA
T_{DFAULT}	Hold on time in fault mode			1		s
$I_{VDDFAULT1}$	VDD sink current, BO	After T_{DFAULT} 1S		1.2	2.0	mA
V_{DDOVP}	VDD OVP		34.5	36.2	38.0	V
I_{VDDOVP}	VDD OVP sink current	V_{DD} > V_{DDOVP}		5		mA
T_{VDDOVP}	VDD OVP debounce time			160		us
ZERO VOLTAGE DETECTION (ZCD)						
V_{ZCDOVP}	ZCD OVP		4.28	4.5	4.72	V
N_{ZCDOVP}	ZCD OVP debounce counter			4		Cycles
I_{ZCDMAX}	Maximum ZCD Clamp source current		1			mA
$V_{ZCDCLAMP}$	ZCD Clamp voltage	$I_{ZCDCLAMP}$=1.0mA		-120		mV
$T_{LEB1OVP}$	Leading edge blanking time1	FB = 0.65V		1.6		us
$T_{LEB2OVP}$	Leading edge blanking time2	FB = 2.20V		2.3		us
V_{ZCDH}	ZCD valley detection rising edge	V_{DRV} = low	0.40	0.45	0.50	V
I_{ZCDBI}	Line voltage brown in clamp current threshold in ZCD		135	155	175	uA
I_{ZCDBO}	Line voltage brown out clamp current threshold in ZCD		115	140	165	uA
T_{DZCDBO}	ZCD brown out debounce time			64		ms
$I_{LINECOMPST}$	Line voltage compensation threshold ZCD clamp current			210		uA
$K_{LINECOMP}$	The ratio of line voltage compensation		0.17	0.20	0.22	
FEEDBACK VOLTAGE (FB)						
V_{FBOPEN}	Open Loop Voltage	I_{FB} = 0	2.80	3.0	3.2	V

R_{FB}	FB pull-up resistor			8		kΩ
V_{FBOLP}	OLP or FB open loop		2.30	2.50	2.7	V
T_{FBOLP}	Debounce time of FB open loop protection	V_{FB} > 2.8V		64		ms
V_{FBBST}	FB voltage when DRV stops pulsing		0.4	0.6		V
$V_{FBBSTHYS}$	V_{FBBSTH} hysteresis voltage			0.1		V
CURRENT SENSE (CS)						
T_{SSCS}	Soft start time of CS threshold	After start up and no trigger protection		5		ms
$V_{CSLIMIT}$	Cycle by cycle current limited		0.47	0.495	0.52	V
T_{LEBCBC}	Leading edge blanking time			350		ns
V_{CS_SSCP}	Secondary rectifier short protection		0.9	1.0	1.1	V
N_{CS_SSCP}	Secondary rectifier short circuit protection debounce counter			3		Cycles
$T_{LEBSSCP}$	Leading edge blanking time			200		ns
$V_{CSSLOPE}$	Slope compensation		13.0	15.0	17.0	mV/us
V_{CSMIN}	CS minimum voltage			0.1		V
ΔV_{CS}	CS jitter			±5		%
T_{JIT}	CS jitter cycle			480		cycles
GATE DRIVER (DRV)						
V_{OL}	Driver output low voltage	VDD=15V			0.5	V
V_{OH1}	Driver output high voltage1	VDD=15V	8.0			V
V_{OH2}	Driver output high voltage2	VDD>V_{DDOFF}	6.0			V
$I_{DRVSOURCE}$	DRV maximum source current	V_{DRV} < 1V		300		mA
$I_{DRVSINK}$	DRV maximum sink current	V_{DRV} > 9V		600		mA
V_{CLAMP}	Output clamp voltage			11		V
T_R	Output rising time 1.2V ~ 10.8V	CL=1nF		200		ns
T_F	Output falling time 10.8V ~ 1.2V	CL=1nF		50		ns
External OTP (OTP)						
I_{OTP}	Current source for OTP			100		uA
V_{OTP}	External OTP trigger voltage			0.5		V
T_{OTPP}	External OTP detection period			10		ms
T_{OTPDEB}	OTP debounce time			560		us
Internal Segmented Power Supply Control Circuit (SW)						
I_{SWOFF}	Boost circuit turn off current			0.1		A
$T_{SWONMAX}$	Boost maximum on time			1.2		us

$T_{SWOFFMIN}$	Boost minimum off time		0.6	us
Oscillator for Switching Frequency				
F_{SWMAX}	Switching frequency	SC3002A/SC3002AL	67	kHz
		SC3002B/SC3002BL	85	
		SC3002C	100	
F_{SWMIN}	Minimum frequency		21	kHz
T_{OFFMAX}	Maximum off time	After SS, without ZCD	145	us
D_{MAX}	Maximum duty cycle		78	%
Internal Over-Temperature Protection (OTP)				
OTP_H	OTP Temperature		150	℃
OTP_{HYS}	OTP Hysteresis		30	℃

8 Functional Block Diagram

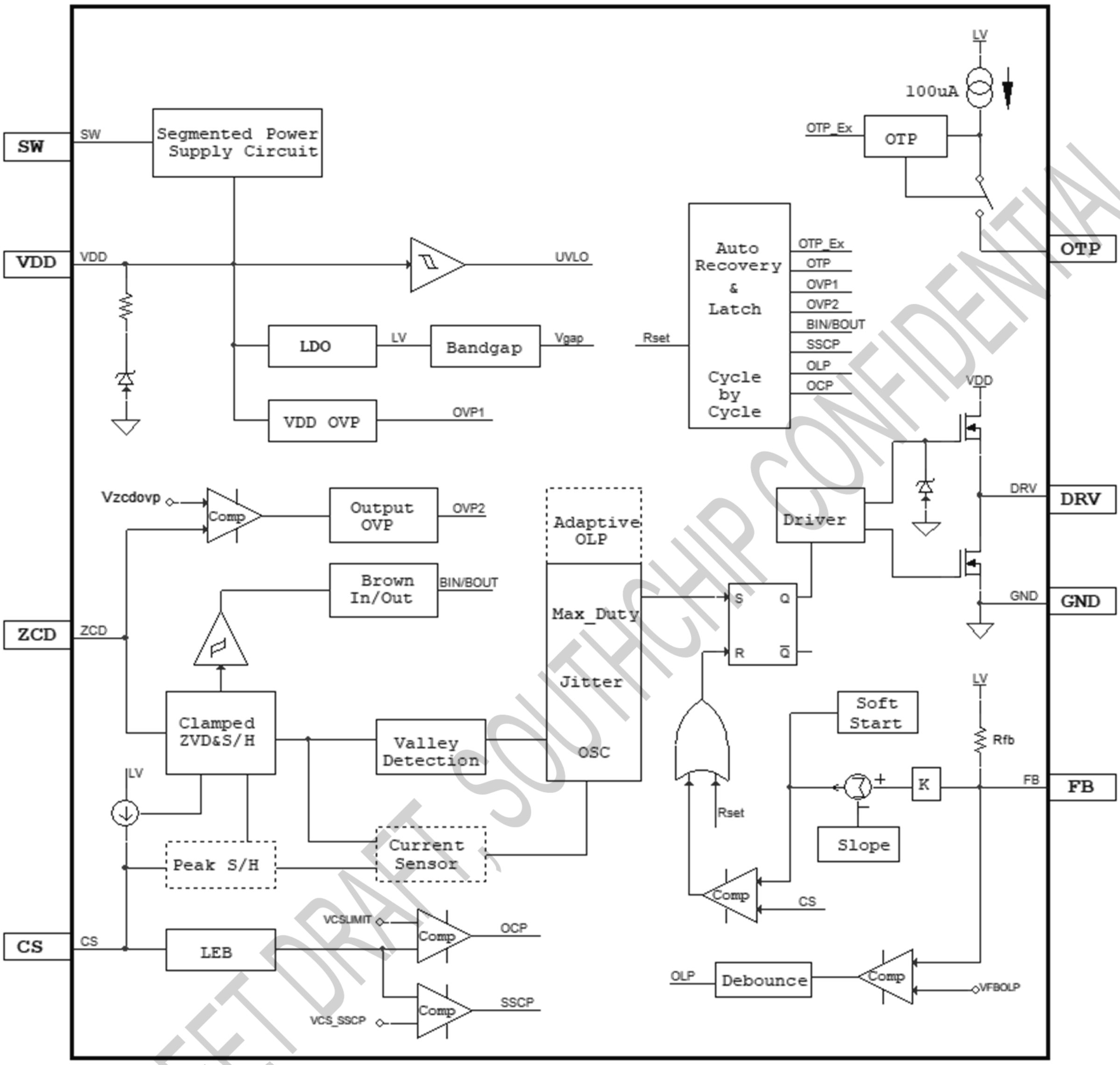


Fig.3 Function Block Diagram

9 Feature Description

SC3002 is designed for USB-PD solutions, together with PD controller, such as SC21xx serials. The controller integrates a segmented power supply control circuit, which is especially suitable for applications with a wide output voltage range, reducing power consumption and greatly reducing peripheral devices.SC3002 provides an adaptive switching frequency fold-back to achieve higher efficiency in the whole loading range. At heavy load or full load, it operates up to maximum switching frequency. When loading decreases, it operates in green mode with valley switching for high efficiency. And at no load, the IC will operate in Burst mode to reduce power consumption.

9.1 Start-up

During the startup period, the controller draws a little current I_{VDD} less than 2uA. This allows a high-impedance start-up resistor, which offers a convenient and efficient way to reduce the standby power.

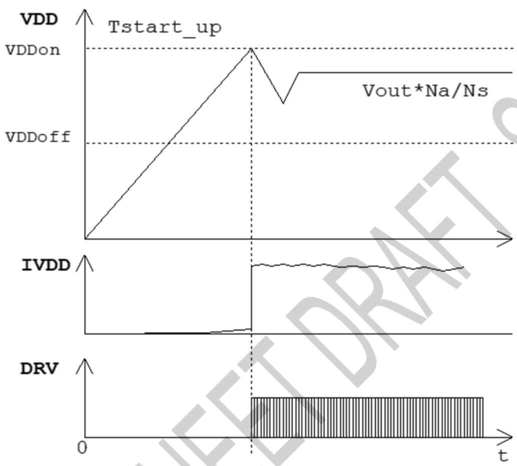


Fig. 3 VDD start-up waveform

The start-up time can be estimated by the following equation:

$$T_{START-UP} \approx \frac{C_{VDD} * V_{DDON}}{V_{BULK}} * R_{STARTUP}$$

Where, C_{VDD} is VDD cap, V_{BULK} is the bulk cap voltage, $R_{START-UP}$ is the resistor connected between bulk cap positive terminal and VDD cap.

An integrated 5ms soft start is used in the chip to reduce the voltage and current stress. During the soft start-up period, the Vcs threshold gradually rises from 0.1V to 0.5V. Once the secondary side regulation loop is stable, the Vcs is controlled by the feedback loop.

9.2 VDD UVLO

A hysteresis Under Voltage Lock Out (UVLO) comparator is implemented in SC3002. The turn-on and turn-off thresholds are fixed at 16.5V and 7.5V respectively. This hysteresis ensures that the VDD capacitor can be small enough during start-up. A large hysteresis is essential to ensure the IC work properly during the start-up period, even for a small VDD capacitor.

9.3 VDD Holding Mode

After the system starts, the VDD capacitor can be charged by the auxiliary winding. There are some operation condition changes (load changes, output voltage adjustment, burst mode), may lead the primary side DRV stop working when the output value is higher than the set value. Furthermore, the VDD voltage will be lower than V_{DDOFF} and the system will stop. To avoid this situation, a VDD holding circuitry is designed, which starts working when VDD drops below $V_{DDHOLDL}$ and stops working when VDD rises above $V_{DDHOLDH}$. The working process is shown in below:

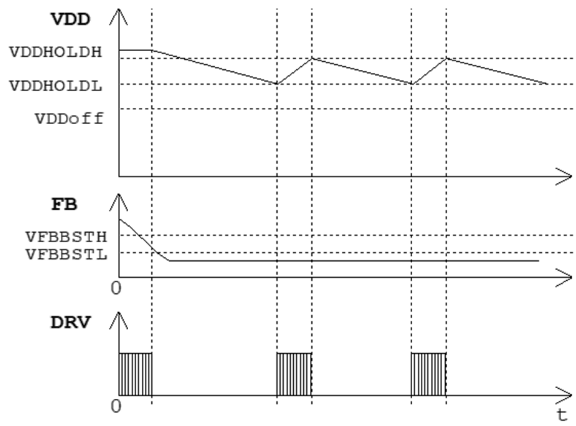


Fig. 4 VDD holding circuitry

9.4 Segmented Power Supply Control Circuit for VDD Power Supply

In some applications with a wide output voltage range, especially for chargers that need to support PPS, the output voltage range is 3.3V ~ 21V. In order to meet the power supply of the SSR controller, additional circuits need to be added. This makes the circuit complicated and increases system power consumption, which is very unfavorable. The SC3002 integrates a segmented power supply control circuit, and only needs to add an inductor, which can also guarantee the power supply of VDD under the low output voltage of auxiliary winding. The working process of this circuit is shown below:

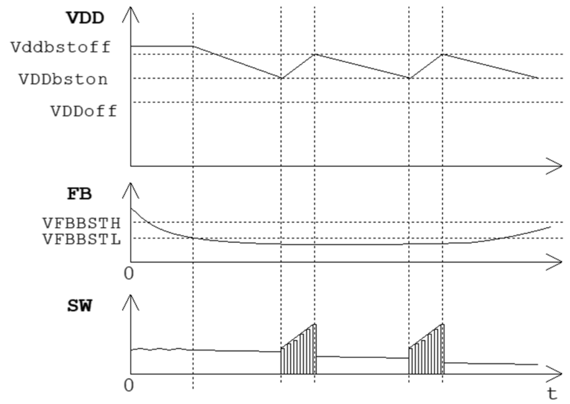


Fig. 5 The Boost Circuit

9.5 Brown IN/OUT Detection

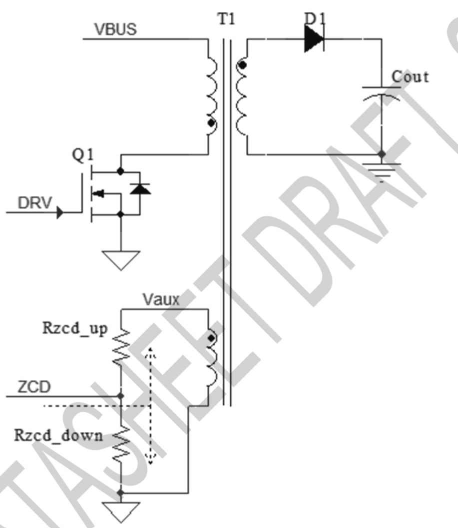


Fig. 6 Brown In/Out detection

The ZCD pin is used to monitor the voltage on the Bulk capacitor and perform brown In/Out. Working principle: When the primary switch is turned on, the voltage V_{AUX} on the auxiliary winding is negative. The value of V_{AUX} is proportional to the line voltage. The clamp circuit built in the ZCD pin clamps the voltage of the ZCD to $V_{ZCDCLAMP}$ through a current source.

The detailed equations are shown as below:

$$\frac{V_{AUX}}{R_{ZCD-UP}} = I_{ZCD} \quad \text{and} \quad V_{AUX} = \frac{V_{BULK}}{N_P} * N_{AUX}$$

The V_{AUX} is negatively associated with I_{ZCD}. V_{AUX} is a negative value. When I_{ZCD} is greater than I_{ZCDBI}, the Brown in process is executed and the system starts to work. When the value of I_{ZCD} is less than I_{ZCDBO} and lasts for a certain period of time, the line voltage is considered to be too low and brown out protection is triggered.

9.6 Operation Mode

SC3002 provides an adaptive switching frequency fold-back to achieve higher efficiency in the whole loading range. At heavy load or full load, it operates up to 85kHz switching frequency. When loading decreases, it operates in green mode with valley switching for high efficiency. And at no load, the IC will operate in Burst mode to reduce power consumption.

When the system is under no load or extremely light load, the IC will operate in BURST mode to reduce power dissipation. In this condition, switching loss of MOSFET is the main power dissipation. The DRV will be disabled immediately if V_{FB} drops below V_{FBBSTL}. When V_{FB} rises up to V_{FBBSTH}, the DRV starts to pulse again.

When under medium load condition, the system operates in green mode (DCM or QR). The switching frequency will linearly increase from 21kHz to maximum switching frequency. That means, when load increases, the switching frequency is increased.

9.7 Valley Switching

ZCD pin can detect the freewheel information on the secondary side. In QR mode, when the voltage of ZCD turns to a negative value, it means that after a quarter of the resonant period, the primary MOS can be turned on, and valley opening helps to improve efficiency and improve EMI performance. In order to achieve the best valley opening, it can be achieved by appropriately adjusting T_{DZCD} and T_{DDRV}, where T_{DPG} is an internal fixed delay. T_{DZCD} can be adjusted by connecting a small capacitor in parallel with $R_{ZCDDWON}$. The recommended value is 10 ~ 22pF. T_{DDDRV} can be adjusted by connecting DRV resistors in series.

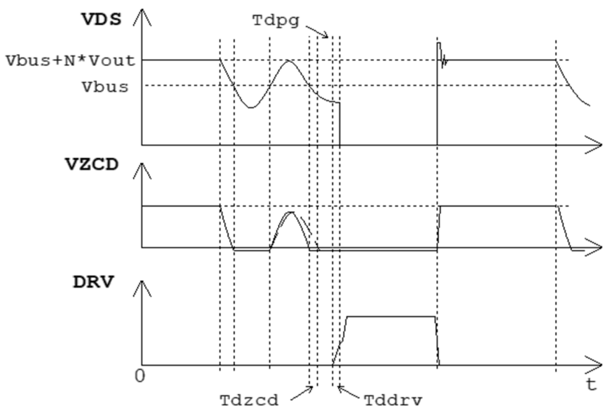


Fig. 7 Valley Switching

9.8 Internal Slope Compensation

A slope compensation circuitry is built-in to simplify the system design. When the switcher is on, a ramp voltage is added to the sensed voltage across the CS pin, which helps to stabilize the system and prevent sub-harmonic oscillations.

9.9 Auto-Recovery after Failure

SC3002 has complete protection functions, such as: VDD over voltage protection, VDD under voltage lock out, two level over current protection, output over voltage protection, Output short protection, over Load protection, brown IN/Out with auto-recovery. Unless otherwise specified, these protections are auto-recovery. After the protection is triggered, the system enters the protection mode, and the VDD power consumption is reduced. After the T_{DFAULT} delay, the VDD sink current increases until V_{DDOFF}, and VDD starts the restart process. The detailed process is as follows.

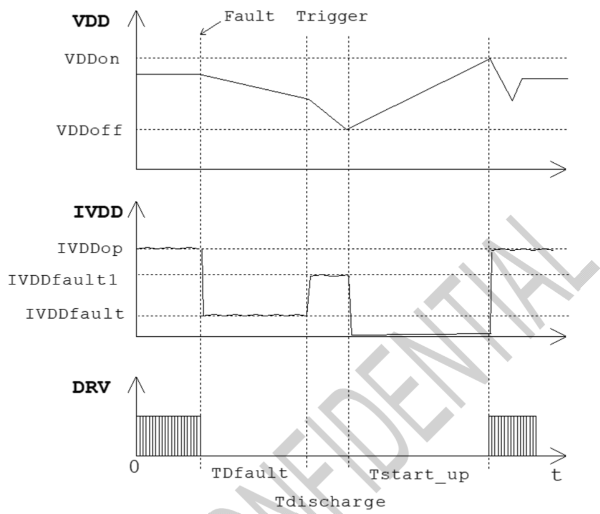


Fig. 8 Auto-Recovery Process

9.10 VDD OVP

When the VDD voltage is higher than the V_{DDOVP} threshold voltage at least T_{VDDOVP}, in the case of a sink current of I_{VDDOVP}, DRV will be shut down. The VDD OVP function is an auto-recovery protection.

9.11 ZCD OVP

The auxiliary winding demagnetization voltage V_{AUX} is proportional to the output voltage. V_{ZCD} sensing the V_{AUX} via the divided resistors can be used to sample the output voltage after some blanking time. The output over voltage can be calculated as:

$$\frac{V_{AUX} * R_{ZCD-DOWN}}{R_{ZCD-DOWN} + R_{ZCD-UP}} > V_{ZCDOVP}$$

$$\frac{V_{AUX}}{N_A} = \frac{V_{OUT}}{N_S}$$

The blanking time can ignore the voltage ringing from leakage inductance of transformer. With the increase of VFB, the blanking time is from 1.4uS to 2.15uS.

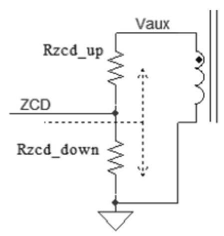


Fig. 9 ZCD Over Voltage Protection

9.12 Over Current Protection

Two levels of overcurrent protection are integrated. One is cycle-by-cycle current limiting for overload protection. V_{CSSSCP} is the fast protection for the case of secondary rectifier rectification shorted. The overcurrent protection and its shielding time are shown in the figure below.

SC3002 integrated the adaptive over current protection (AOCP), which allows controlling the maximum output current from primary-side in width output voltage range.

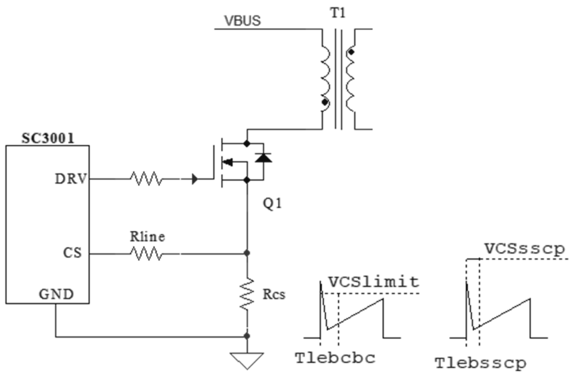


Fig. 10 LEB of OCP

9.13 Adaptive Over Load Protection (AOLP)

An adaptive over load protection is implemented in the SC3002. When the voltage of VFB is higher than V_{FBOLP} and lasts for a period of time T_{FBOLP}, overload protection will be triggered. In particular, when the voltage of VFB is higher than V_{FBOLP}, if the peak voltage of ZCD pin is lower than V_{ZCDH}, the delay of T_{FBOLP} will be shortened. In the Fig.10, when V_{ZCD} is lower than V_{ZCDH}, the coefficient K is less than 1. The AOLP can reduce the power loss when secondary side is shorted.

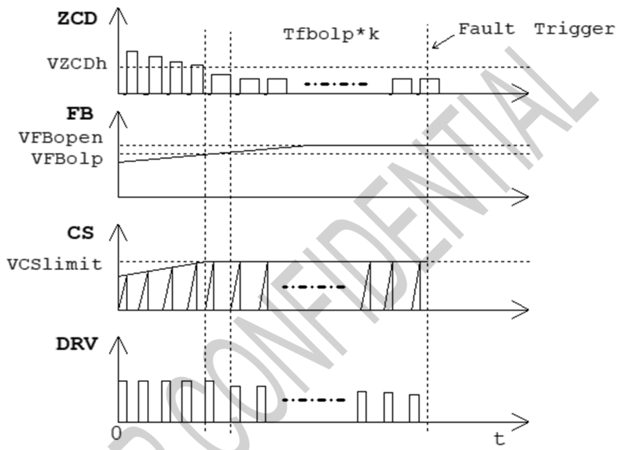


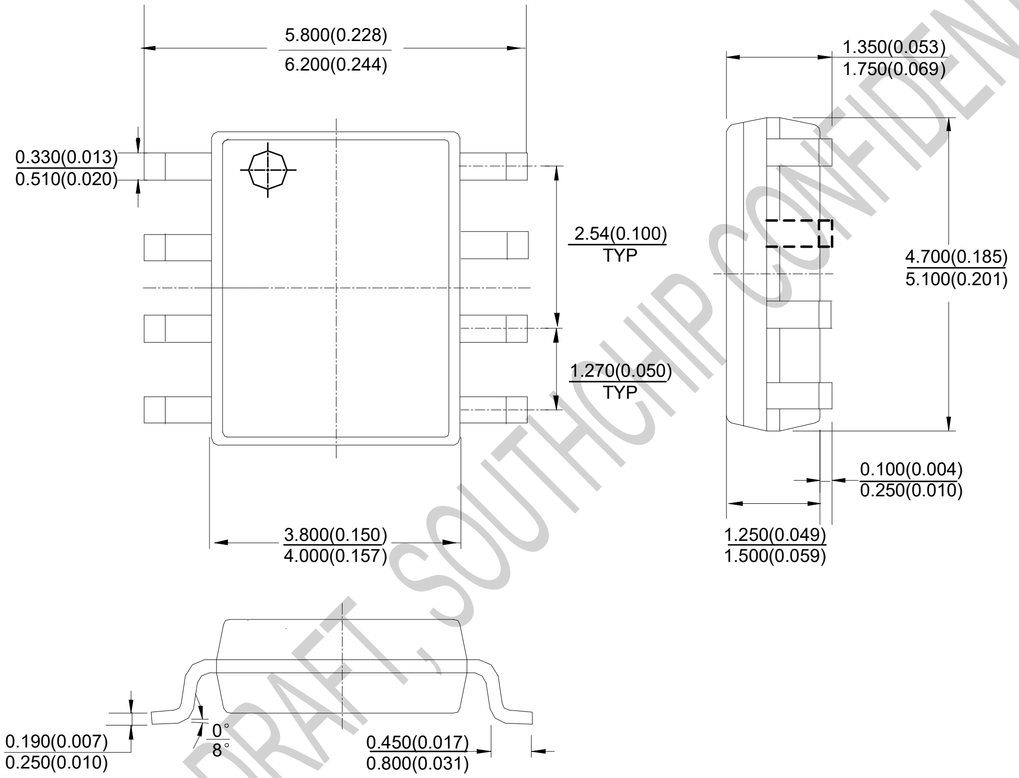
Fig. 11 Adaptive Over Load Protection

9.14 On-Chip OTP

An internal OTP circuit is embedded inside to provide the worst-case protection for SC3002. When the chip temperature rises higher than the OTP_H, the controller will be disabled and works in the failure mode until the chip is cooled down below the hysteresis OTP_{HYS}.

MECHANICAL DATA

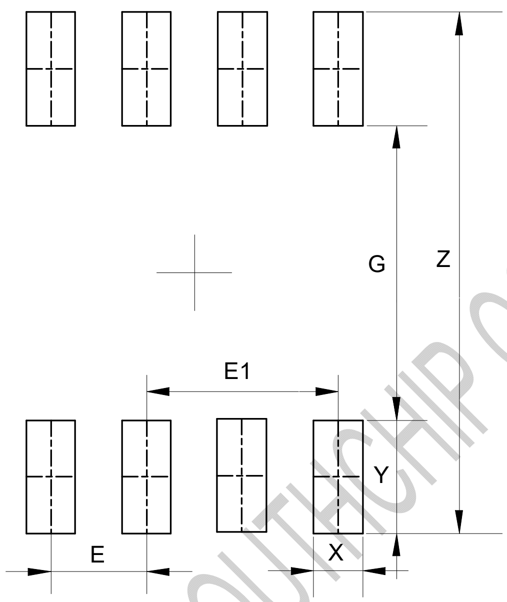
SOP8 (6.0mmx4.9mmx1.55mm)



Note: Eject hole, oriented hole and mold mark is optional.

RECOMMENDED FOOTPRINT

Example Board Layout



Dimensions	Z (mm)/(inch)	G (mm)/(inch)	X (mm)/(inch)	Y (mm)/(inch)	E (mm)/(inch)	E1 (mm)/(inch)
Value	6.900/0.272	3.900/0.154	0.650/0.026	1.500/0.059	1.270/0.050	2.540/0.100

NOTES:

A. Publication IPC-7351 is recommended for alternate designs

B. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad