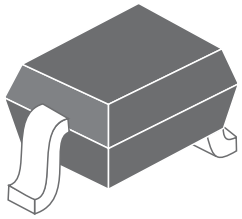
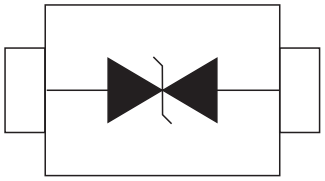
Electro-Static Discharge for Automobile
AESD36FB
Bidirectional TVS Diode

SOD-323



Pin Configuration



Features

- 320 Watts Peak Pulse Power per Line (tp=8/20μs)
- Protects one I/O or power line
- Low clamping voltage
- Working voltages: 36V
- Low leakage current
- AEC-Q101

IEC Compatibility

- IEC61000-4-2 (ESD) ±30kV (air), ±30kV (contact)
- IEC61000-4-4 (EFT) 40A (5/50ns)

Applications

- Cell Phone Handsets and Accessories
- Microprocessor based equipment
- Personal Digital Assistants(PDA's)
- Notebooks,Desktops,and Servers
- Portable Instrumentation
- Peripherals
- Pagers

Mechanical Characteristics

- JEDEC SOD-323 Package
- Molding Compound Flammability Rating:UL 94V-O
- Weight 0.5 Millgrams(Approximate)
- Quantity Per Reel:3000pcs
- Reel Size:7 inch
- Lead Finish:Lead Free

Maximum Ratings(T_A=25℃ unless otherwise noted)

Parameter	Symbol	Value	Units
Peak Pulse Power(tp=8/20μs)	P_{PP}	320	Watts
Lead Soldering Temperature	T_L	260(10 sec.)	℃
Operating Temperature Range	T_J	-55~150	℃
Storage Temperature Range	T_{STG}	-55~150	℃

Electrical Characteristics(T_A=25℃ unless otherwise specified)

AESD36FB(Marking:2N)

Parameter	Symbol	Conditions	Min.	Max.	Units
Reverse Stand-off Voltage	V_{RWM}			36	V
Breakdown Voltage	V_{BR}	I_T=1mA	40		V
Clamping Voltage	V_C	I_{PP}=1A,tp=8/20μs		60	V
		I_{PP}=5A,tp=8/20μs		75	V
Reverse Leakage Current	I_R	@V_{RWM}		1	μA
Junction Capacitance	$C_{I/O}$	0Vdc,f=1MHz Between I/O Pins and GND		40	pF

Ratings and Characteristic Curves

Fig.1 Non-Repetitive Pulse Power vs.Pulse Time

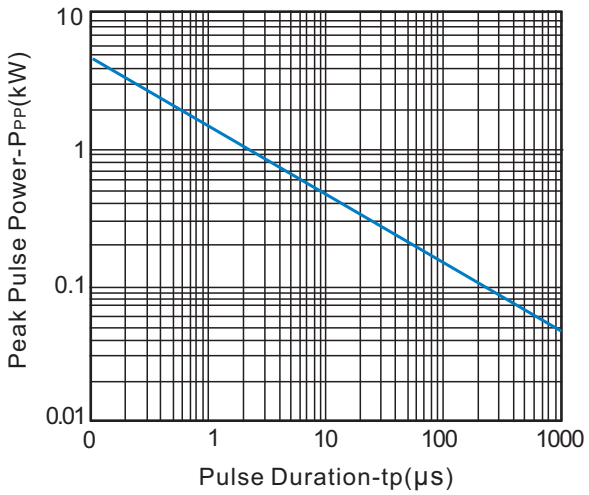
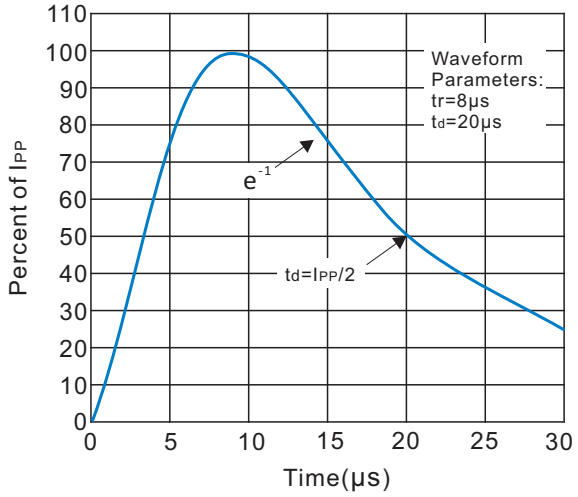
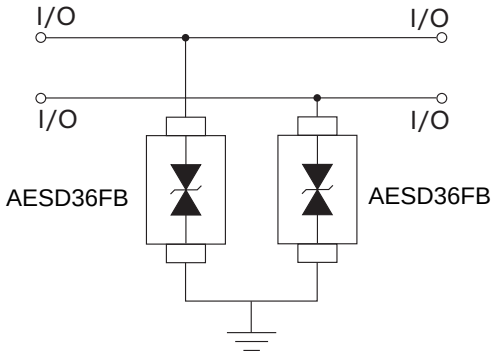


Fig.2 Pulse Waveform



Application Information

I/O Protection



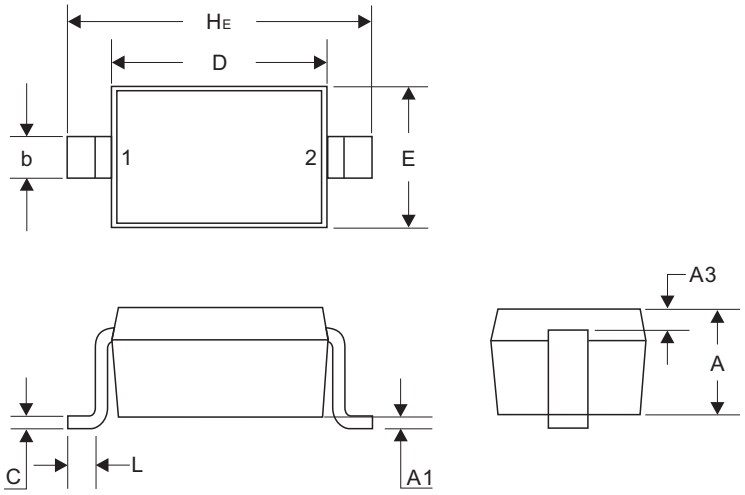
PCB Layout Recommendations

The location and circuit board layout is critical to maximize the effectiveness of the I/O protection circuit. The following guidelines are recommended:

- Locate the protection devices as close as possible to the I/O connector. This allows the protection devices to absorb the energy of the transient voltage before it can be coupled into the adjacent traces on the PCB.
- Minimize the loop area for the high.speed data lines, power and ground lines to reduce the radiated emissions.
- Avoid running protection conductors in parallel with unprotected conductors
- Use ground planes wherever possible to reduce the parasitic capacitance and inductance of the PCB that degrades the effectiveness of a filter device.
- Using shared transient return paths to a common ground point.

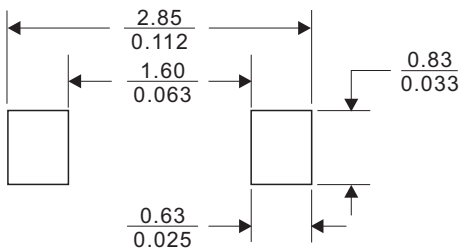
Dimensions(SOD-323)

SOD-323



DIM	Millimeters		Inches	
	Min	Max	Min	Max
A	0.80	1.00	0.031	0.040
A1	0.00	0.10	0.000	0.004
A3	0.15REF		0.006REF	
b	0.25	0.40	0.010	0.016
C	0.089	0.177	0.003	0.007
D	1.60	1.80	0.062	0.070
E	1.15	1.35	0.045	0.053
L	0.08		0.003	
HE	2.30	2.70	0.090	0.105

Recommended Mounting Pad Layout



Dimensions in (millimeters / inches)