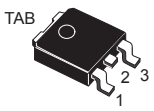
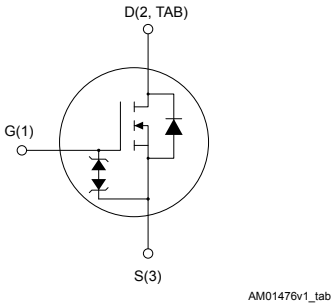
Automotive-grade N-channel 1000 V, 5.4 Ω typ., 2.2 A SuperMESH Power MOSFET in a DPAK package



DPAK



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STD4NK100Z	1000 V	6.8 Ω	2.2 A

- AEC-Q101 qualified
- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitance
- Zener-protected

Applications

- Switching applications

Description

This high-voltage device is a Zener-protected N-channel Power MOSFET developed using the SuperMESH technology by STMicroelectronics, an optimization of the well-established PowerMESH. In addition to a significant reduction in on-resistance, this device is designed to ensure a high level of dv/dt capability for the most demanding applications.

Product status link
STD4NK100Z

Product summary(1)	
Order code	STD4NK100Z
Marking	4NK100Z
Package	DPAK
Packing	Tape and reel

1. *The HTRB test was performed at 80% $V_{(BR)DSS}$ in compliance with AEC-Q101 rev. C. All the other tests were performed according to rev. D.*

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	1000	V
V_{GS}	Gate-source voltage	±30	V
I_D	Drain current (continuous) at T_C = 25 °C	2.2	A
	Drain current (continuous) at T_C = 100 °C	1	
I_{DM} (1)	Drain current (pulsed)	8.8	A
P_{TOT}	Total power dissipation at T_C = 25 °C	90	W
ESD	Gate-source human body model (R = 1.5 kΩ, C = 100 pF)	3	kV
dv/dt (2)	Peak diode recovery voltage slope	4.5	V/ns
T_{stg}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range		

1. *Pulse width limited by safe operating area.*
2. *I_{SD} ≤ 2.2 A, di/dt ≤ 200 A/µs, V_{DS} (peak) ≤ $V_{(BR)DSS}$, V_{DD} ≤ $V_{(BR)DSS}$.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	1.39	°C/W
R_{thJA} (1)	Thermal resistance, junction-to-ambient	50	°C/W

1. *When mounted on 1 inch² FR-4, 2 Oz copper board.*

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_J max.)	2.5	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	110	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 4. On/off-state

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	1000			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 1000 V			1	µA
		V_{GS} = 0 V, V_{DS} = 1000 V, T_C = 125 °C(1)			50	
I_{GSS}	Gate body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 50 µA	3.0	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 1.1 A		5.4	6.8	Ω

1. *Specified by design, not tested in production.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0 V	-	601	-	pF
C_{oss}	Output capacitance		-	53	-	pF
C_{rss}	Reverse transfer capacitance		-	12	-	pF
$C_{oss\ eq.}$ (1)	Equivalent output capacitance	V_{GS} = 0 V, V_{DS} = 0 to 800 V	-	15	-	pF
Q_g	Total gate charge	V_{DD} = 800, I_D = 2.5 A, V_{GS} = 0 to 10 V (see Figure 14. Test circuit for gate charge behavior)	-	18	-	nC
Q_{gs}	Gate-source charge		-	3.6	-	nC
Q_{gd}	Gate-drain charge		-	9.2	-	nC

1. *$C_{oss\ eq.}$ is defined as the constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 500 V, I_D = 1.25 A, R_G = 4.7 Ω, V_{GS} = 10 V see (Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	15	-	ns
t_r	Rise time		-	7.5	-	ns
$t_{d(off)}$	Turn-off delay time		-	32	-	ns
t_f	Fall time		-	39	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		2.2	A
I_{SDM}(1)	Source-drain current (pulsed)		-		8.8	A
V_{SD}(2)	Forward on voltage	I_{SD} = 2.5 A, V_{GS} = 0 V	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 2.5 A, di/dt = 100 A/µs,	-	584		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 100 V	-	2.3		µC
I_{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	8		A
t_{rr}	Reverse recovery time	I_{SD} = 2.5 A, di/dt = 100 A/µs,	-	628		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 100 V, T_J = 150 °C	-	2.5		µC
I_{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	8.1		A

1. *Pulse width limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

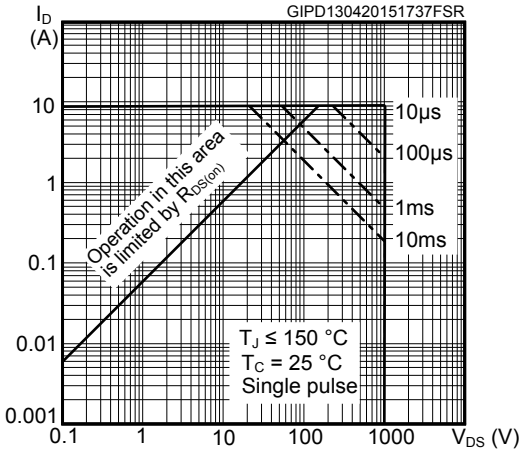


Figure 2. Normalized transient thermal impedance

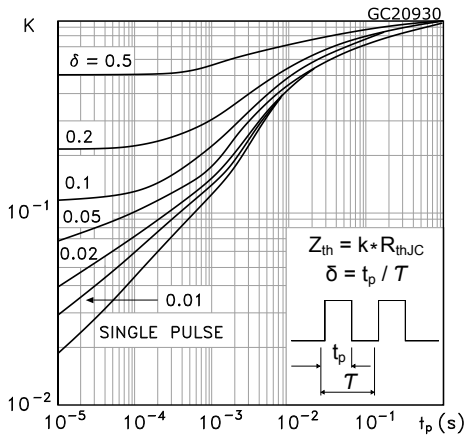


Figure 3. Typical output characteristics

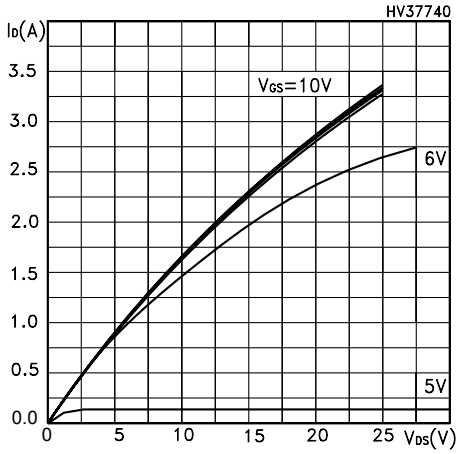


Figure 4. Typical transfer characteristics

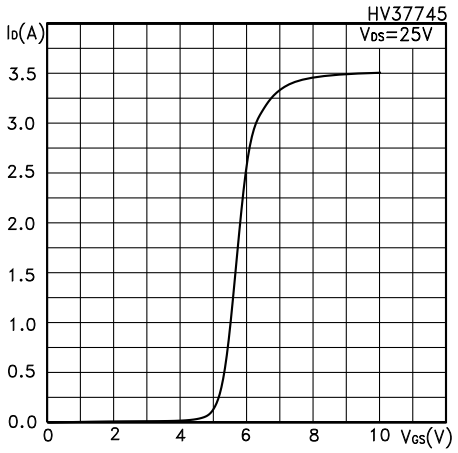


Figure 5. Typical drain-source on-resistance

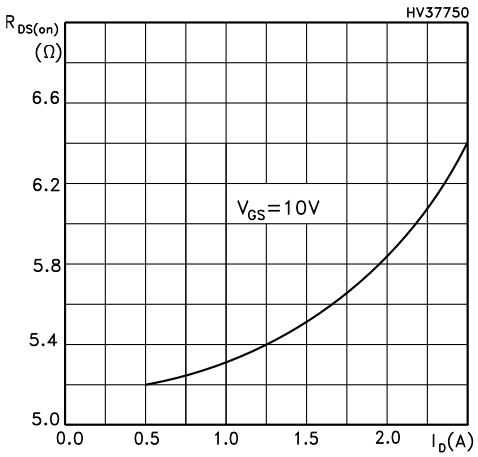


Figure 6. Typical gate charge characteristics

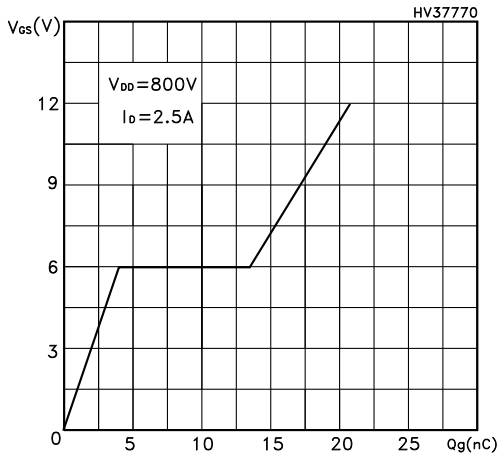


Figure 7. Typical capacitance characteristics

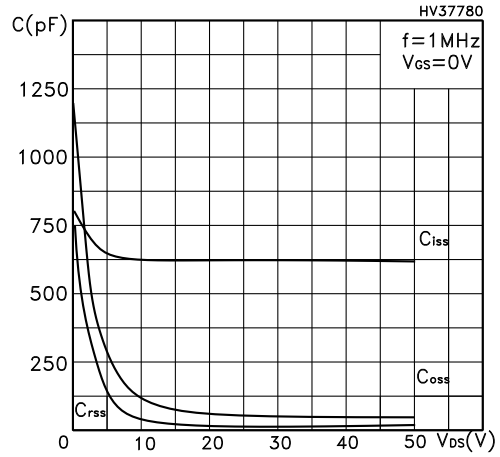


Figure 8. Normalized gate threshold vs temperature

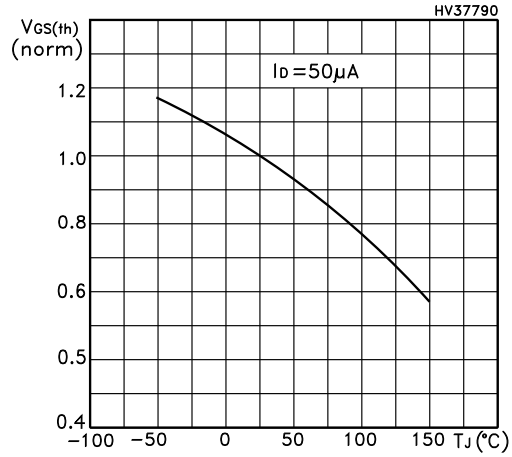


Figure 9. Normalized on-resistance vs temperature

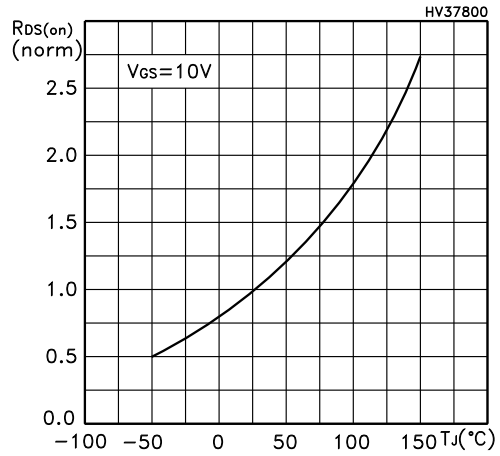


Figure 10. Typical reverse diode forward characteristics

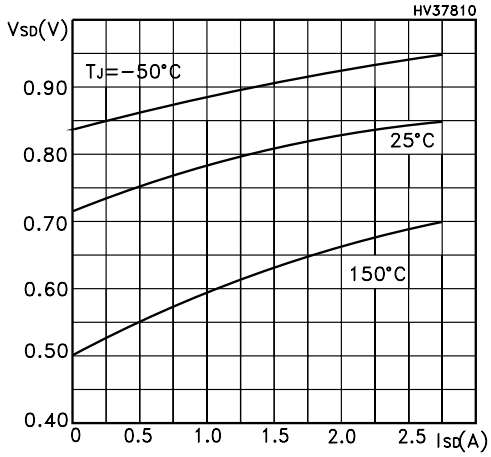


Figure 11. Normalized breakdown voltage vs temperature

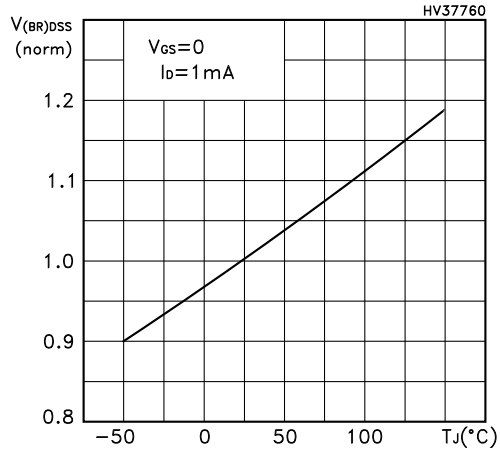
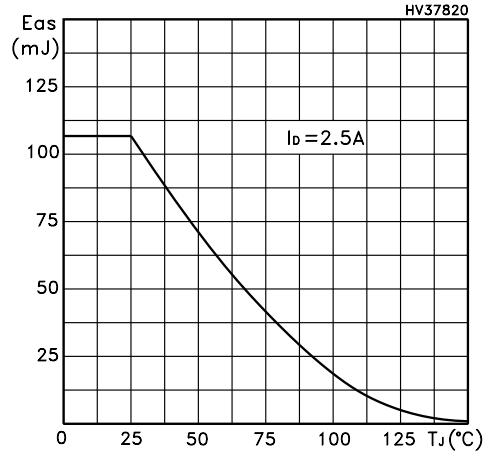


Figure 12. Maximum avalanche energy vs temperature



3 Test circuits

Figure 13. Test circuit for resistive load switching times

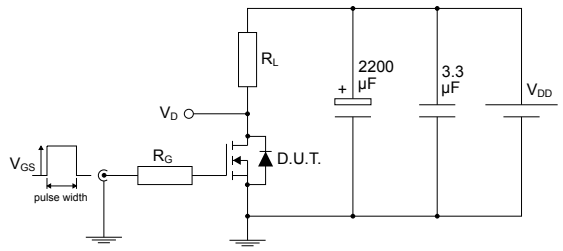


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Figure 14. Test circuit for gate charge behavior

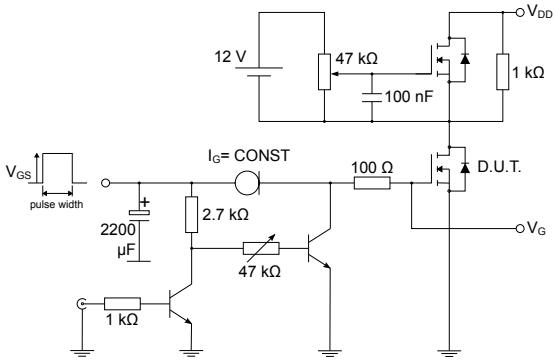

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Figure 15. Test circuit for inductive load switching and diode recovery times

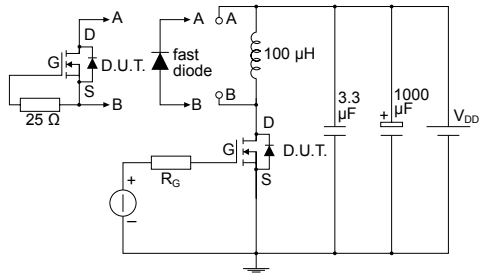

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Figure 16. Unclamped inductive load test circuit

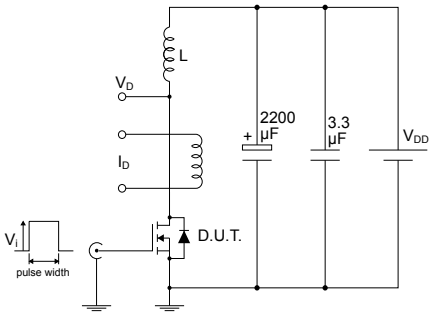

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Figure 17. Unclamped inductive waveform

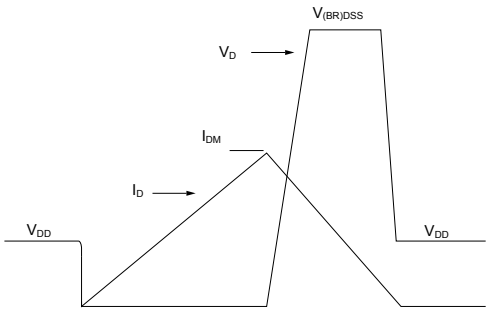

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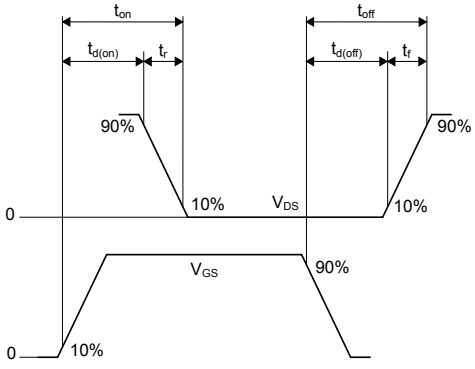
Figure 18. Switching time waveform



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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 DPAK (TO-252) type A2 package information

Figure 19. DPAK (TO-252) type A2 package outline

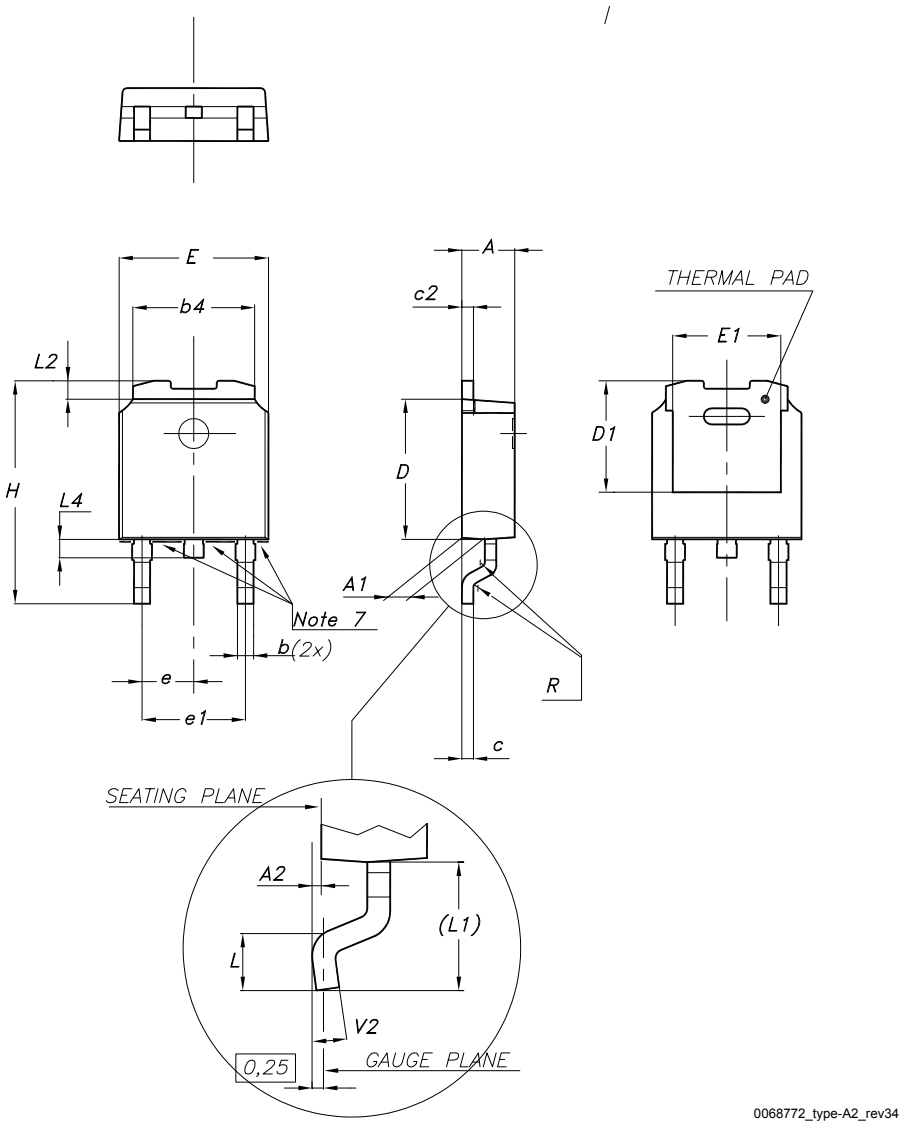
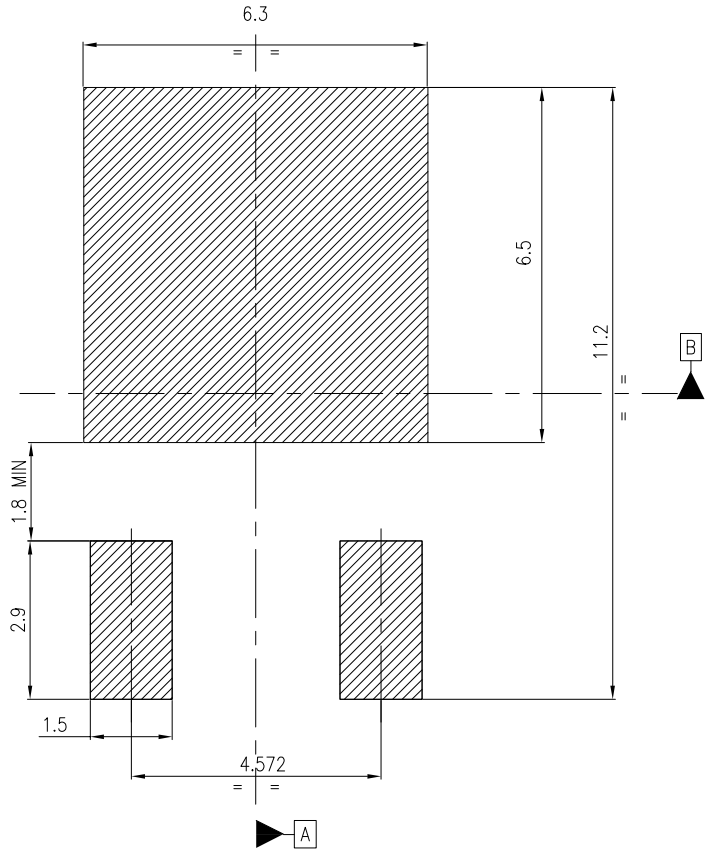


Table 8. **DPAK (TO-252) type A2 mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	5.10	5.20	5.30
e	2.159	2.286	2.413
e1	4.445	4.572	4.699
H	9.35		10.10
L	1.00		1.50
L1	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 20. DPAK (TO-252) recommended footprint (dimensions are in mm)



Notes:
1) This footprint is able to ensure insulation up to 630 Vrms (according to CEI IEC 664−1)
2) The device must be positioned within ⌖ 0.05 A B

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4.2 DPAK (TO-252) packing information

Figure 21. **DPAK (TO-252) tape outline**

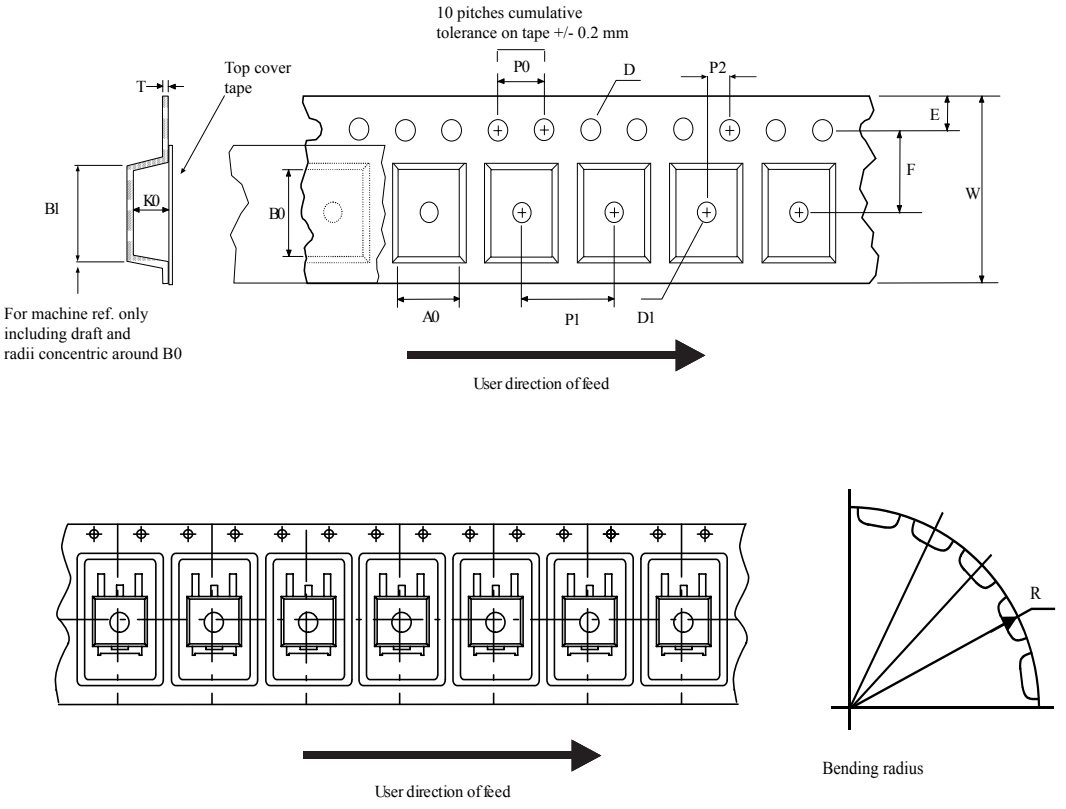

Figure 22. **DPAK (TO-252) reel outline**

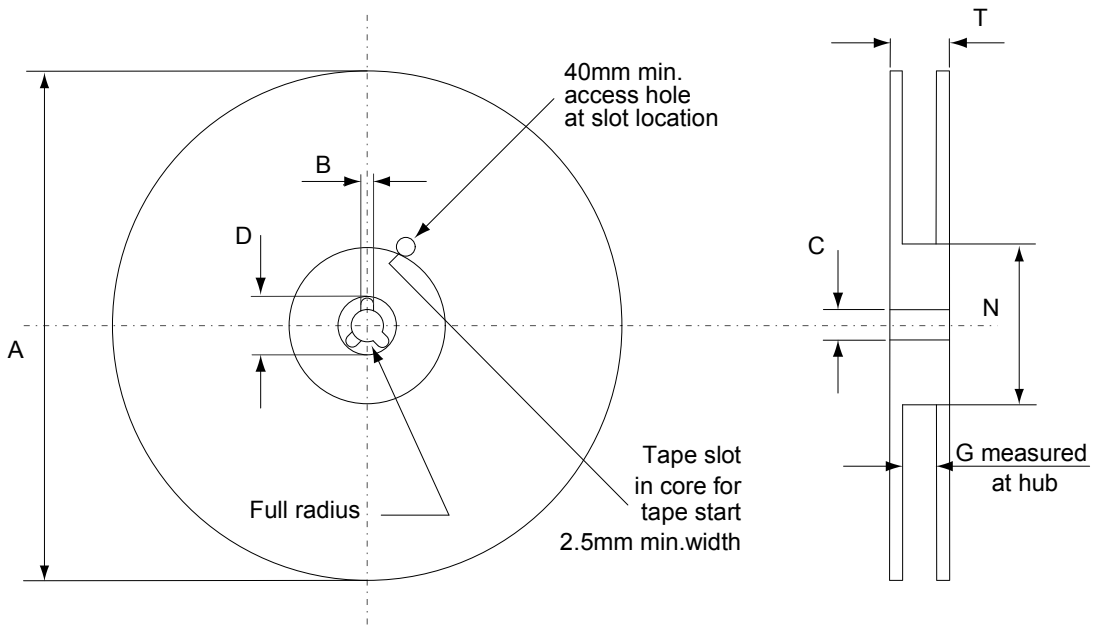

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Table 9. **DPAK (TO-252) tape and reel mechanical data**

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Revision history

Table 10. **Document revision history**

Date	Revision	Changes
01-Oct-2013	1	First release.
13-Apr-2015	2	Document status promoted from preliminary to production data. Updated *title* and *features* in cover page. Updated *Section 2.1: Electrical characteristics (curves)* and *Section 4: Package information.* Minor text changes.
04-Apr-2023	3	Updated Section 4 Package information Minor text changes.

Contents

单击下面可查看定价，库存，交付和生命周期等信息

>>STMicro(意法半导体)