VN7140AJ, VN7140AS

High-side driver with MultiSense analog feedback for automotive applications

SO-8

PowerSSO-16

Features

Max transient supply voltage	V_{CC}	40 V
Operating voltage range	V_{CC}	4 to 28 V
Typ. on-state resistance (per Ch)	R_{ON}	140 mΩ
Current limitation (typ)	I_{LIMH}	12 A
Standby current (max)	I_{STBY}	0.5 µA

- AEC-Q100 qualified
- General
  - Single channel smart high-side driver with MultiSense analog feedback
  - Very low standby current
  - Compatible with 3 V and 5 V CMOS outputs
- MultiSense diagnostic functions
  - Multiplexed analog feedback of: load current with high precision proportional current mirror, V_{CC} supply voltage and T_{CHIP} device temperature
  - Overload and short to ground (power limitation) indication
  - Thermal shutdown indication
  - OFF-state open-load detection
  - Output short to V_{CC} detection
  - Sense enable/disable
- Protections
  - Undervoltage shutdown
  - Overvoltage clamp
  - Load current limitation
  - Self limiting of fast thermal transients
  - Configurable latch-off on overtemperature or power limitation with dedicated fault reset pin
  - Loss of ground and loss of V_{CC}
  - Reverse battery with external components
  - Electrostatic discharge protection

Product status link
VN7140AJ
VN7140AS

Applications

- All types of automotive resistive, inductive and capacitive loads
- Specially intended for automotive signal lamps (up to R10W or LED Rear Combinations)
- Protected supply for ADAS systems: radars and sensors

Description

The devices are single channel high-side drivers manufactured using ST proprietary VIPower M0-7 technology and housed in PowerSSO-16 and SO-8 packages. The

devices are designed to drive 12 V automotive grounded loads through a 3 V and 5 V CMOS-compatible interface, and to provide protection and diagnostics.

The devices integrate advanced protective functions such as load current limitation, overload active management by power limitation and overtemperature shutdown with configurable latch-off.
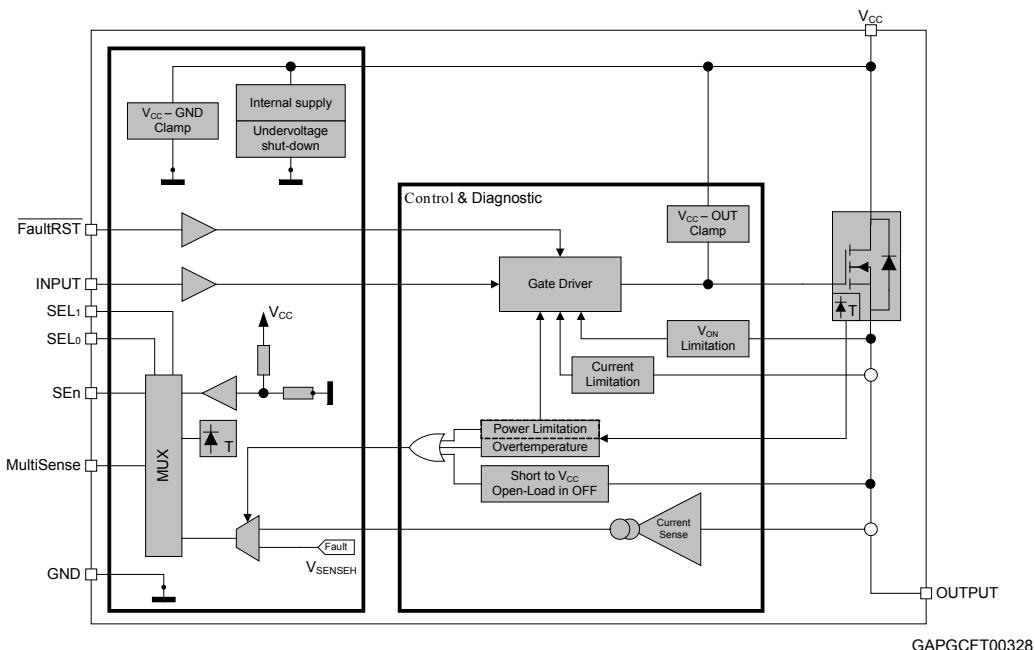
A $\overline{\text{FaultRST}}$ pin unlatches the output in case of fault or disables the latch-off functionality.

A dedicated multifunction multiplexed analog output pin delivers sophisticated diagnostic functions including high precision proportional load current sense, supply voltage feedback and chip temperature sense, in addition to the detection of overload and short circuit to ground, short to V_{CC} and OFF-state open-load.

A sense enable pin allows OFF-state diagnosis to be disabled during the module low-power mode as well as external sense resistor sharing among similar devices.

# 1 Block diagram and pin description

Figure 1. Block diagram
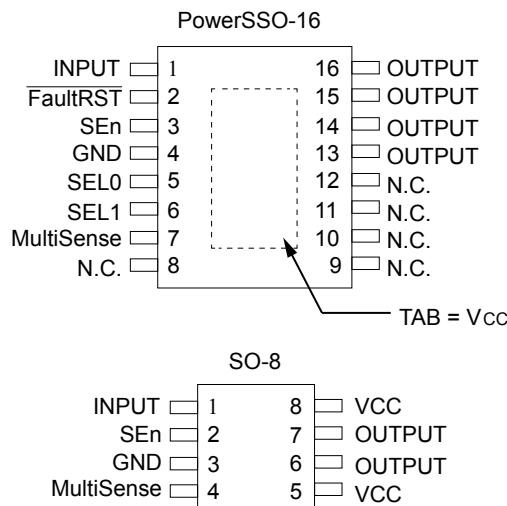
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Table 1. Pin functions

| Name	Function
V_{CC}	Battery connection.
OUTPUT	Power outputs.
GND	Ground connection. Must be reverse battery protected by an external diode / resistor network.
INPUT	Voltage controlled input pin with hysteresis, compatible with 3 V and 5 V CMOS outputs. It controls output switch state.
MultiSense	Multiplexed analog sense output pin; it delivers a current proportional to the selected diagnostic: load current, supply voltage or chip temperature.
SEn	Active high compatible with 3 V and 5 V CMOS outputs pin; it enables the MultiSense diagnostic pin.
$SEL_{0,1}$	Active high compatible with 3 V and 5 V CMOS outputs pin; they address the MultiSense multiplexer.
$\overline{FaultRST}$	Active low compatible with 3 V and 5 V CMOS outputs pin; it unlatches the output in case of fault; If kept low, sets the outputs in auto-restart mode.

Figure 2. Configuration diagram (top view)

PowerSSO-16

INPUT	1	16	OUTPUT
FaultRST̄	2	15	OUTPUT
SEn	3	14	OUTPUT
GND	4	13	OUTPUT
SEL0	5	12	N.C.
SEL1	6	11	N.C.
MultiSense	7	10	N.C.
N.C.	8	9	N.C.

TAB = V_{CC}

SO-8

INPUT	1	8	VCC
SEn	2	7	OUTPUT
GND	3	6	OUTPUT
MultiSense	4	5	VCC

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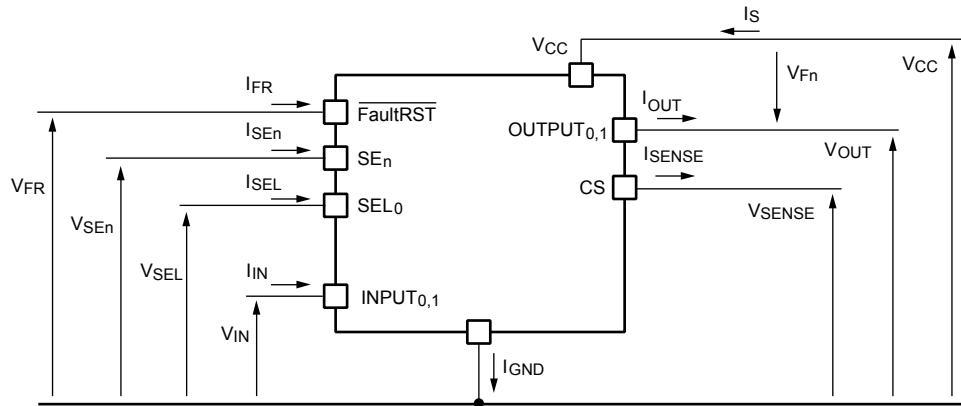
Table 2. Suggested connections for unused and not connected pins

Connection / pin	MultiSense	N.C.	Output	Input	SEn, SELx, FaultRST̄
Floating	Not allowed	X [1]	X	X	X
To ground	Through 1 kΩ resistor	X	Not allowed	Through 15 kΩ resistor	Through 15 kΩ resistor

1. X: do not care.

2 Electrical specification

Figure 3. Current and voltage conventions

GADG2203170950PS

Note: $V_F = V_{OUT} - V_{CC}$ *during reverse battery condition.*

2.1 Absolute maximum ratings

Stressing the device above the rating listed in Table 3. Absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions in table below for extended periods may affect device reliability.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	38	V
$-V_{CC}$	Reverse DC supply voltage	0.3	
V_{CCPK}	Maximum transient supply voltage (ISO 16750-2:2010 Test B clamped to 40 V; $R_L = 4\ \Omega$)	40	V
V_{CCJS}	Maximum jump start voltage for single pulse short circuit protection	28	V
$-I_{GND}$	DC reverse ground pin current	200	mA
I_{OUT}	OUTPUT DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	3	
I_{IN}	INPUT DC input current		
I_{SEn}	SEn DC input current		
I_{SEL}	$SEL_{0,1}$ DC input current	-1 to 10	mA
I_{FR}	FaultRST DC input current		
V_{FR}	FaultRST DC input voltage	7.5	V
I_{SENSE}	MultiSense pin DC output current ($V_{GND} = V_{CC}$ and $V_{SENSE} < 0$ V)	10	mA
	MultiSense pin DC output current in reverse ($V_{CC} < 0$ V)	-20	

Symbol	Parameter		Value	Unit
E$_{MAX}$	Maximum switching energy (single pulse) (T$_{DEMAG}$ = 0.4 ms; T$_{jstart}$ = 150 °C)		10	mJ
V$_{ESD}$	Electrostatic discharge (JEDEC 22A-114F)			V
		INPUT	4000	
		MultiSense	2000	
		SEn, SEL$_{0,1}$, FaultRST	4000	
		OUTPUT		
		V$_{CC}$		
V$_{ESD}$	Charge device model (CDM-AEC-Q100-011)		750	V
T$_j$	Junction operating temperature		-40 to 150	°C
T$_{stg}$	Storage temperature		-55 to 150	

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Typ. value		Unit
		SO-8	PowerSSO-16	
R$_{thj-board}$	Thermal resistance junction-board (JEDEC JESD 51-8) [1]	31	7.9	°C/W
R$_{thj-amb}$	Thermal resistance junction-ambient (JEDEC JESD 51-2)[2]	71	61	
R$_{thj-amb}$	Thermal resistance junction-ambient (JEDEC JESD 51-2)	48.5	26.5	

1. *Device mounted on four-layers 2s2p PCB*

2. *Device mounted on two-layers 2s0p PCB with 2 cm^2 heatsink copper trace*

2.3 Main electrical characteristics

7 V < V$_{CC}$ < 28 V; -40°C < T$_j$ < 150°C, unless otherwise specified.

All typical values refer to V$_{CC}$ = 13 V; T$_j$ = 25°C, unless otherwise specified.

Table 5. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V$_{CC}$	Operating supply voltage		4	13	28	V
V$_{USD}$	Undervoltage shutdown				4	V
V$_{USDReset}$	Undervoltage shutdown reset				5	V
V$_{USDhyst}$	Undervoltage shutdown hysteresis			0.3		V
R$_{ON}$	On-state resistance	I$_{OUT}$ = 1 A; T$_j$ = 25°C		140		mΩ
		I$_{OUT}$ = 1 A; T$_j$ = 150°C			280	
		I$_{OUT}$ = 1 A; V$_{CC}$ = 4 V; T$_j$ = 25°C			210	
V$_{clamp}$	Clamp voltage	I$_S$ = 20 mA; 25°C < T$_j$ < 150°C	41	46	52	V
		I$_S$ = 20 mA; T$_j$ = -40°C	38			V

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{STBY}	Supply current in standby at V_{CC} = 13 V [1]	V_{CC} = 13 V; V_{IN} = V_{OUT} = V_{FR} = V_{SEn} = 0 V; $V_{SEL0,1}$ = 0 V; T_j = 25°C			0.5	µA
		V_{CC} = 13 V; V_{IN} = V_{OUT} = V_{FR} = V_{SEn} = 0 V; $V_{SEL0,1}$ = 0 V; T_j = 85°C [2]			0.5	
		V_{CC} = 13 V; V_{IN} = V_{OUT} = V_{FR} = V_{SEn} = 0 V; $V_{SEL0,1}$ = 0 V; T_j = 125°C			3	
t_{D_STBY}	Standby mode blanking time	V_{CC} = 13 V; V_{IN} = V_{OUT} = V_{FR} = $V_{SEL0,1}$ = 0 V; V_{SEn} = 5 V to 5 V	60	300	550	µs
$I_{S(ON)}$	Supply current	V_{CC} = 13 V; V_{SEn} = 0 V; $V_{SEL0,1}$ = V_{FR} = 0 V; V_{IN} = 5 V; I_{OUT} = 0 A		3	5	mA
$I_{GND(ON)}$	Control stage current consumption in ON-state. All channels active.	V_{CC} = 13 V; V_{SEn} = 5 V; V_{FR} = $V_{SEL0,1}$ = 0 V; V_{IN} = 5 V; I_{OUT} = 1 A			6	mA
$I_{L(off)}$	Off-state output current at V_{CC} = 13 V	V_{IN} = V_{OUT} = 0 V; V_{CC} = 13 V; T_j = 25°C	0	0.01	0.5	µA
		V_{IN} = V_{OUT} = 0 V; V_{CC} = 13 V; T_j = 125°C	0		3	
V_F	Output - V_{CC} diode voltage	I_{OUT} = -1 A; T_j = 150°C			0.7	V

1. *PowerMOS leakage included.*
2. *Parameter specified by design; not subjected to production test.*

Table 6. Switching

V_{CC} = 13 V; -40°C < T_j < 150°C, unless otherwise specified						
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ [1]	Turn-on delay time at T_j = 25 °C	R_L = 13 Ω	10	70	120	µs
$t_{d(off)}$ [1]	Turn-off delay time at T_j = 25 °C		10	40	100	
$(dV_{OUT}/dt)_{on}$ [1]	Turn-on voltage slope at T_j = 25 °C	R_L = 13 Ω	0.1	0.27	0.7	V/µs
$(dV_{OUT}/dt)_{off}$ [1]	Turn-off voltage slope at T_j = 25 °C		0.1	0.35	0.7	
W_{ON}	Switching energy losses at turn-on (t_{won})	R_L = 13 Ω	—	0.15	0.18 [2]	mJ
W_{OFF}	Switching energy losses at turn-off (t_{woff})	R_L = 13 Ω	—	0.1	0.18 [2]	mJ
t_{SKEW} [1]	Differential Pulse skew (t_{PHL} - t_{PLH})	R_L = 13 Ω	-100	-50	0	µs

1. *See Figure 6. Switching time and Pulse skew.*
2. *Parameter guaranteed by design and characterization; not subjected to production test.*

Table 7. Logic inputs

7 V < V_{CC} < 28 V; -40°C < T_j < 150°C						
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
		INPUT characteristics				

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
**7 V < V_{CC} < 28 V; -40°C < T_j < 150°C**						
V_{IL}	Input low level voltage				0.9	V
I_{IL}	Low level input current	V_{IN} = 0.9 V	1			µA
V_{IH}	Input high level voltage		2.1			V
I_{IH}	High level input current	V_{IN} = 2.1 V			10	µA
$V_{I(hyst)}$	Input hysteresis voltage		0.2			V
V_{ICL}	Input clamp voltage	I_{IN} = 1 mA	5.3		7.2	V
		I_{IN} = -1 mA		-0.7		
$\overline{\text{FaultRST}}$ characteristics (VN7140AJ only)						
V_{FRL}	Input low level voltage				0.9	V
I_{FRL}	Low level input current	V_{IN} = 0.9 V	1			µA
V_{FRH}	Input high level voltage		2.1			V
I_{FRH}	High level input current	V_{IN} = 2.1 V			10	µA
$V_{FR(hyst)}$	Input hysteresis voltage		0.2			V
V_{FRCL}	Input clamp voltage	I_{IN} = 1 mA	5.3		7.5	V
		I_{IN} = -1 mA		-0.7		
$SEL_{0,1}$ characteristics (7 V < V_{CC} < 18 V) (VN7140AJ only)						
V_{SELL}	Input low level voltage				0.9	V
I_{SELL}	Low level input current	V_{IN} = 0.9 V	1			µA
V_{SELH}	Input high level voltage		2.1			V
I_{SELH}	High level input current	V_{IN} = 2.1 V			10	µA
$V_{SEL(hyst)}$	Input hysteresis voltage		0.2			V
V_{SELCL}	Input clamp voltage	I_{IN} = 1 mA	5.3		7.2	V
		I_{IN} = -1 mA		-0.7		
SEn characteristics (7 V < V_{CC} < 18 V)						
V_{SEnL}	Input low level voltage				0.9	V
I_{SEnL}	Low level input current	V_{IN} = 0.9 V	1			µA
V_{SEnH}	Input high level voltage		2.1			V
I_{SEnH}	High level input current	V_{IN} = 2.1 V			10	µA
$V_{SEn(hyst)}$	Input hysteresis voltage		0.2			V
V_{SEnCL}	Input clamp voltage	I_{IN} = 1 mA	5.3		7.2	V
		I_{IN} = -1 mA		-0.7		

Table 8. Protections

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
7 V < V_{CC} < 18 V; -40°C < T_j < 150°C
I_{LIMH}	DC short circuit current	V_{CC} = 13 V	8	12	16	A
		4 V < V_{CC} < 18 V [1]				
I_{LIML}	Short circuit current during thermal cycling	V_{CC} = 13 V; T_R < T_j < T_{TSD}		4		
T_{TSD}	Shutdown temperature		150	175	200	°C
T_R	Reset temperature[1]		T_{RS} + 1	T_{RS} + 7		
T_{RS}	Thermal reset of fault diagnostic indication	V_{FR} = 0 V; V_{SEn} = 5 V	135			
T_{HYST}	Thermal hysteresis(T_{TSD} - T_R)[1]			7		
ΔT_{J_SD}	Dynamic temperature	T_j = -40°C; V_{CC} = 13 V		60		K
t_{LATCH_RST}	Fault reset time for output unlatch (only for VN7140AJ) [1]	V_{FR} = 5 V to 0 V; V_{SEn} = 5 V; V_{IN} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V	3	10	20	µs
V_{DEMAG}	Turn-off output voltage clamp	I_{OUT} = 1 A; L = 6 mH; T_j = -40°C	V_{CC} - 38			V
		I_{OUT} = 1 A; L = 6 mH; T_j = 25°C to 150°C	V_{CC} - 41	V_{CC} - 46	V_{CC} - 52	V
V_{ON}	Output voltage drop limitation	I_{OUT} = 0.07 A		20		mV

1. *Parameter guaranteed by design and characterization; not subjected to production test.*

Table 9. MultiSense

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
7 V < V_{CC} < 18 V; -40°C < T_j < 150°C
V_{SENSE_CL}	MultiSense clamp voltage	V_{SEn} = 0 V; I_{SENSE} = 1 mA	-17		-12	V
		V_{SEn} = 0 V; I_{SENSE} = -1 mA		7		
CurrentSense characteristics
K_{OL}	I_{OUT}/I_{SENSE}	I_{OUT} = 0.01 A; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	295			
dK_{cal}/K_{cal} [1] [2]	Current sense ratio drift at calibration point	I_{OUT} = 0.01 A to 0.025 A; I_{cal} = 17.5 mA; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	-30		30	%
K_{LED}	I_{OUT}/I_{SENSE}	I_{OUT} = 0.025 A; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	330	580	820	
dK_{LED}/K_{LED} [1] [2]	Current sense ratio drift	I_{OUT} = 0.025 A; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	-25		25	%
K_0	I_{OUT}/I_{SENSE}	I_{OUT} = 0.07 A; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	375	550	720	
dK_0/K_0 [1] [2]	Current sense ratio drift	I_{OUT} = 0.07 A; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	-20		20	%
K_1	I_{OUT}/I_{SENSE}	I_{OUT} = 0.15 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	360	500	670	
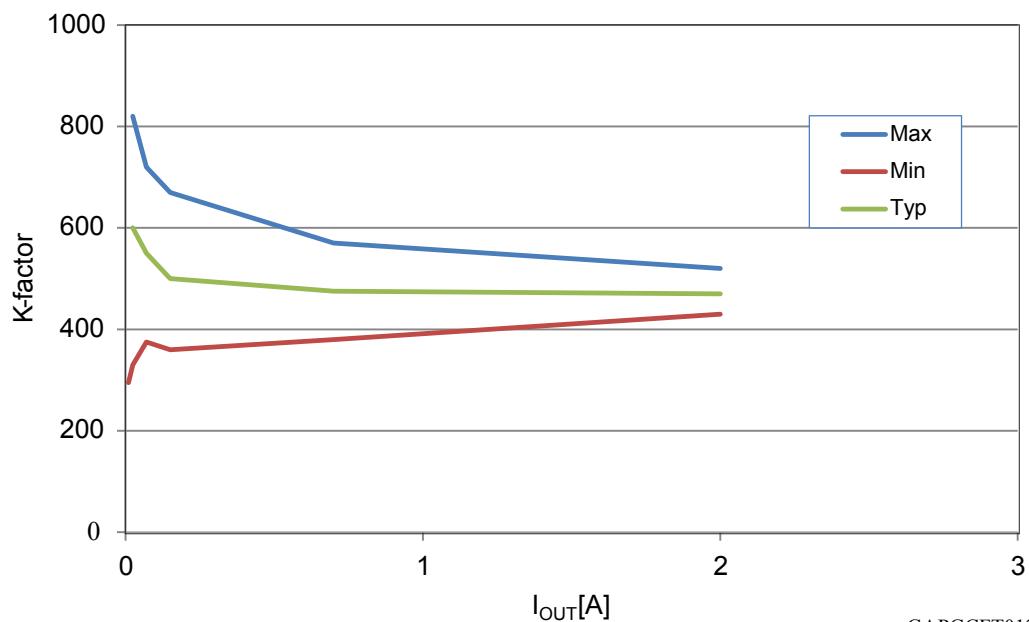
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
dK_1/K_1 [1] [2]	Current sense ratio drift	I_{OUT} = 0.15 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	-15		15	%
K_2	I_{OUT}/I_{SENSE}	I_{OUT} = 0.7 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	380	475	570	
dK_2/K_2 [1] [2]	Current sense ratio drift	I_{OUT} = 0.7 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	-10		10	%
K_3	I_{OUT}/I_{SENSE}	I_{OUT} = 2 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	430	470	520	
dK_3/K_3 [1] [2]	Current sense ratio drift	I_{OUT} = 2 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	-5		5	%
I_{SENSE0}	MultiSense leakage current	MultiSense disabled: V_{SEn} = 0 V	0		0.5	µA
		MultiSense disabled: $-1\,V < V_{SENSE} < 5\,V$[1]	-0.5		0.5	
		MultiSense enabled: V_{SEn} = 5 V; Channel ON; I_{OUT} = 0 A; Diagnostic selected; V_{IN} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V; I_{OUT} = 0 A	0		2	
		MultiSense enabled: V_{SEn} = 5 V; Channel OFF; Diagnostic selected: V_{IN} = 0 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V	0		2	
V_{OUT_MSD} [1]	Output voltage for MultiSense shutdown	V_{IN} = 5 V; V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V; R_{SENSE} = 2.7 kΩ; I_{OUT} = 1 A		5		V
V_{SENSE_SAT}	Multisense saturation voltage	V_{CC} = 7 V; R_{SENSE} = 2.7 kΩ; V_{SEn} = 5 V; V_{IN} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V; I_{OUT} = 2 A; T_j = 150°C	5			V
I_{SENSE_SAT} [1]	CS saturation current	V_{CC} = 7 V; V_{SENSE} = 4 V; V_{IN} = 5 V; V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V; T_j = 150°C	4			mA
I_{OUT_SAT} [1]	Output saturation current	V_{CC} = 7 V; V_{SENSE} = 4 V; V_{IN} = 5 V; V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V; T_j = 150°C	2.2			A
OFF-state diagnostic						
V_{OL}	OFF-state open-load voltage detection threshold	V_{IN} = 0 V; V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V	2	3	4	V
$I_{L(off2)}$	OFF-state output sink current	V_{IN} = 0 V; V_{OUT} = V_{OL}; T_j = -40 °C to 150°C	-100		-15	µA
t_{DSTKON}	OFF-state diagnostic delay time from falling edge of INPUT (see Figure 9. T$_{DSTKON}$)	V_{IN} = 5 V to 0 V; V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V; I_{OUT} = 0 A; V_{OUT} = 4 V	100	350	700	µs
$t_{D\_OL\_V}$	Settling time for valid OFF-state open load diagnostic indication from rising edge of SEn	V_{IN} = 0 V; V_{FR} = 0 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V; V_{OUT} = 4 V; V_{SEn} = 0 V to 5 V			60	µs
t_{D_VOL}	OFF-state diagnostic delay time from rising edge of V_{OUT}	V_{IN} = 0 V; V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V; V_{OUT} = 0 V to 4 V		5	30	µs
Chip temperature analog feedback (VN7140AJ only)						

Table header: **7 V < V_{CC} < 18 V; -40°C < T_j < 150°C**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
7 V < V_{CC} < 18 V; -40°C < T_j < 150°C						
V_{SENSE_TC}	MultiSense output voltage proportional to chip temperature	V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 5 V; V_{IN} = 0 V; R_{SENSE} = 1 kΩ; T_j = -40°C	2.325	2.41	2.495	V
		V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 5 V; V_{IN} = 0 V; R_{SENSE} = 1 kΩ; T_j = 25°C	1.985	2.07	2.155	V
		V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 5 V; V_{IN} = 0 V; R_{SENSE} = 1 kΩ; T_j = 125°C	1.435	1.52	1.605	V
dV_{SENSE_TC}/dT [1]	Temperature coefficient	T_j = -40°C to 150°C		-5.5		mV/K
Transfer function		V_{SENSE_TC} (T) = V_{SENSE_TC} (T_0) + dV_{SENSE_TC} / dT * (T - T_0)				
V_{CC} supply voltage analog feedback (VN7140AJ only)						
V_{SENSE_VCC}	MultiSense output voltage proportional to V_{CC} supply voltage	V_{CC} = 13 V; V_{SEn} = 5 V; V_{SEL0} = 5 V; V_{SEL1} = 5 V; V_{IN} = 0 V; R_{SENSE} = 1 kΩ	3.16	3.23	3.3	V
Transfer function [3]		V_{SENSE_VCC} = V_{CC} / 4				
Fault diagnostic feedback (see Table 10. Truth table)						
V_{SENSEH}	MultiSense output voltage in fault condition	V_{CC} = 13 V; V_{IN} = 0 V; V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V; I_{OUT} = 0 A; V_{OUT} = 4 V; R_{SENSE} = 1 kΩ;	5		6.6	V
I_{SENSEH}	MultiSense output current in fault condition	V_{CC} = 13 V; V_{SENSE} = 5 V	7	20	30	mA
MultiSense timings (current sense mode - see Figure 7. MultiSense timings (current sense mode)) [4]						
$t_{DSENSE1H}$	Current sense settling time from rising edge of SEn	V_{IN} = 5 V; V_{SEn} = 0 V to 5 V; R_{SENSE} = 1 kΩ; R_L = 13 Ω			60	µs
$t_{DSENSE1L}$	Current sense disable delay time from falling edge of SEn	V_{IN} = 5 V; V_{SEn} = 5 V to 0 V; R_{SENSE} = 1 kΩ; R_L = 13 Ω		5	20	µs
$t_{DSENSE2H}$	Current sense settling time from rising edge of INPUT	V_{IN} = 0 V to 5 V; V_{SEn} = 5 V; R_{SENSE} = 1 kΩ; R_L = 13 Ω		100	250	µs
$Δt_{DSENSE2H}$	Current sense settling time from rising edge of I_{OUT} (dynamic response to a step change of I_{OUT})	V_{IN} = 5 V; V_{SEn} = 5 V; R_{SENSE} = 1 kΩ; I_{SENSE} = 90 % of $I_{SENSEMAX}$; R_L = 13 Ω			100	µs
$t_{DSENSE2L}$	Current sense turn-off delay time from falling edge of INPUT	V_{IN} = 5 V to 0 V; V_{SEn} = 5 V; R_{SENSE} = 1 kΩ; R_L = 13 Ω		50	250	µs
MultiSense timings (chip temperature sense mode - see Figure 8. Multisense timings (chip temperature and V_{CC} sense mode) (VN7140AJ only)) [4]						
$t_{DSENSE3H}$	V_{SENSE_TC} settling time from rising edge of SEn	V_{SEn} = 0 V to 5 V; V_{SEL0} = 0 V; V_{SEL1} = 5 V; R_{SENSE} = 1 kΩ			60	µs
$t_{DSENSE3L}$	V_{SENSE_TC} disable delay time from falling edge of SEn	V_{SEn} = 5 V to 0 V; V_{SEL0} = 0 V; V_{SEL1} = 5 V; R_{SENSE} = 1 kΩ			20	µs
MultiSense timings (V_{CC} voltage sense mode - see Figure 8. Multisense timings (chip temperature and V_{CC} sense mode) (VN7140AJ only)) [4]						
$t_{DSENSE4H}$	V_{SENSE_VCC} settling time from rising edge of SEn	V_{SEn} = 0 V to 5 V; V_{SEL0} = 5 V; V_{SEL1} = 5 V; R_{SENSE} = 1 kΩ			60	µs
$t_{DSENSE4L}$	V_{SENSE_VCC} disable delay time from falling edge of SEn	V_{SEn} = 5 V to 0 V; V_{SEL0} = 5 V; V_{SEL1} = 5 V; R_{SENSE} = 1 kΩ			20	µs

		7 V < V_{CC} < 18 V; -40°C < T_j < 150°C				
Symbol	**Parameter**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
		MultiSense timings (Multiplexer transition times) (VN7140AJ only) [4]				
t_{D_CStoTC}	MultiSense transition delay from current sense to T_C sense	V_{IN} = 5 V; V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V to 5 V; I_{OUT} = 0.5 A; R_{SENSE} = 1 kΩ			60	µs
t_{D_TCtoCS}	MultiSense transition delay from T_C sense to current sense	V_{IN} = 5 V; V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 5 V to 0 V; I_{OUT} = 0.5 A; R_{SENSE} = 1 kΩ			20	µs
$t_{D\_CStoVCC}$	MultiSense transition delay from current sense to V_{CC} sense	V_{IN} = 5 V; V_{SEn} = 5 V; V_{SEL0} = 5 V; V_{SEL1} = 0 V to 5 V; I_{OUT} = 0.5 A; R_{SENSE} = 1 kΩ			60	µs
$t_{D\_VCCtoCS}$	MultiSense transition delay from V_{CC} sense to current sense	V_{IN} = 5 V; V_{SEn} = 5 V; V_{SEL0} = 5 V; V_{SEL1} = 5 V to 0 V; I_{OUT} = 0.5 A; R_{SENSE} = 1 kΩ			20	µs
$t_{D\_TCtoVCC}$	MultiSense transition delay from T_C sense to V_{CC} sense	V_{CC} = 13 V; T_j = 125°C; V_{SEn} = 5 V; V_{SEL0} = 0 V to 5 V; V_{SEL1} = 5 V; R_{SENSE} = 1 kΩ			20	µs
$t_{D\_VCCtoTC}$	MultiSense transition delay from V_{CC} sense to T_C sense	V_{CC} = 13 V; T_j = 125°C; V_{SEn} = 5 V; V_{SEL0} = 5 V to 0 V; V_{SEL1} = 5 V; R_{SENSE} = 1 kΩ			20	µs

1. *Parameter specified by design; not subjected to production test.*
2. *All values refer to V_{CC} = 13 V; T_j = 25°C, unless otherwise specified.*
3. *V_{CC} sensing and T_C are referred to GND potential.*
4. *Transition delays are measured up to +/- 10% of final conditions.*

Figure 4. I_{OUT}/I_{SENSE} versus I_{OUT}

GAPGCFT01217

Figure 5. Current sense accuracy versus I$_{OUT}$

GAPGCFT01218
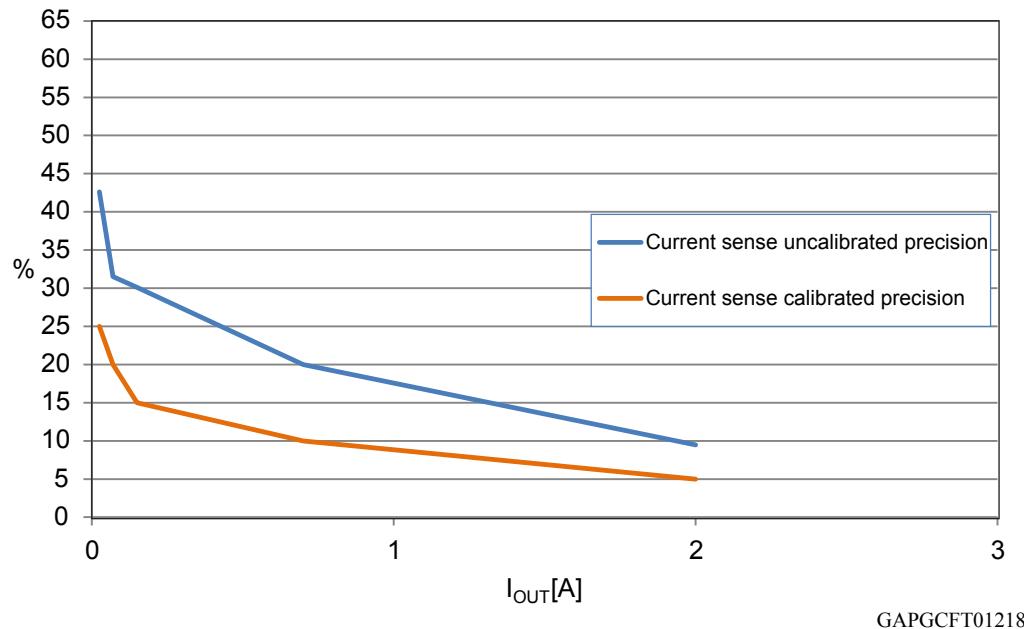
Figure 6. Switching time and Pulse skew
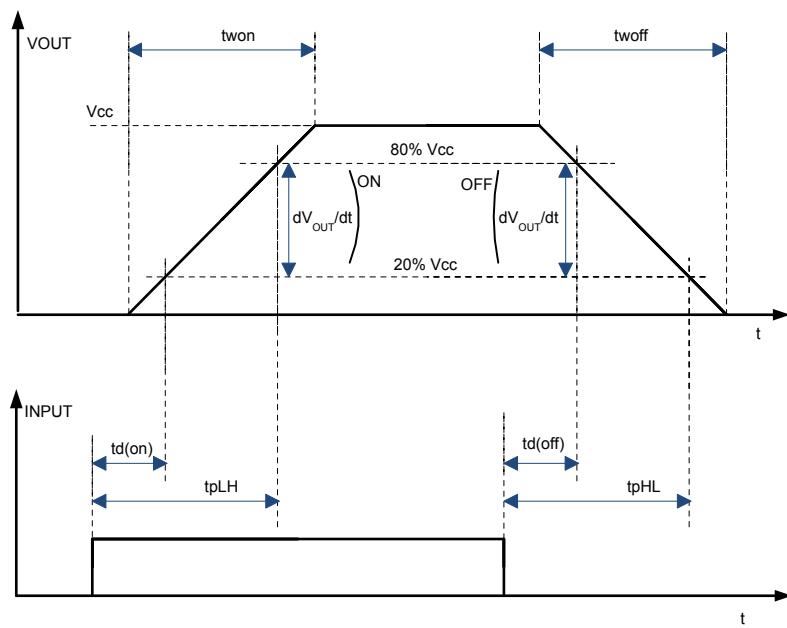
Figure 7. MultiSense timings (current sense mode)
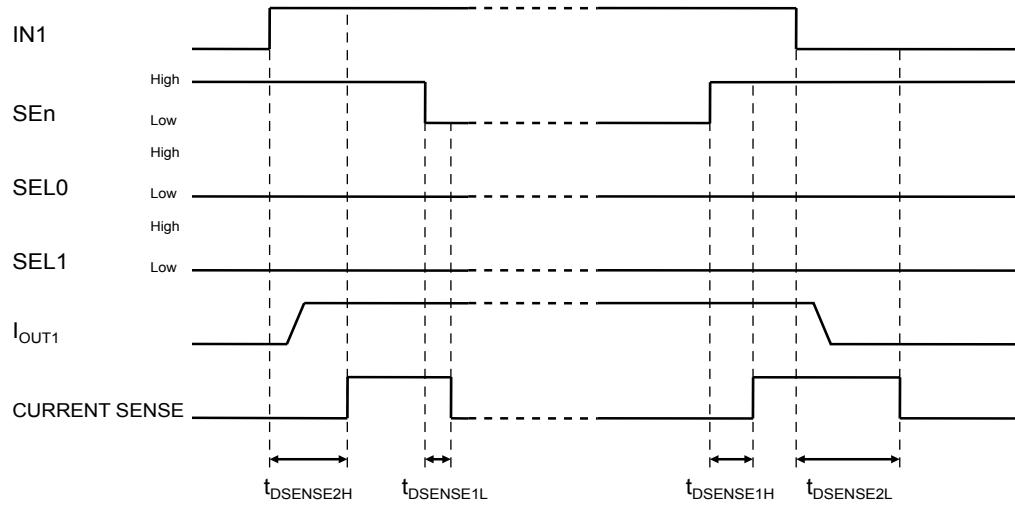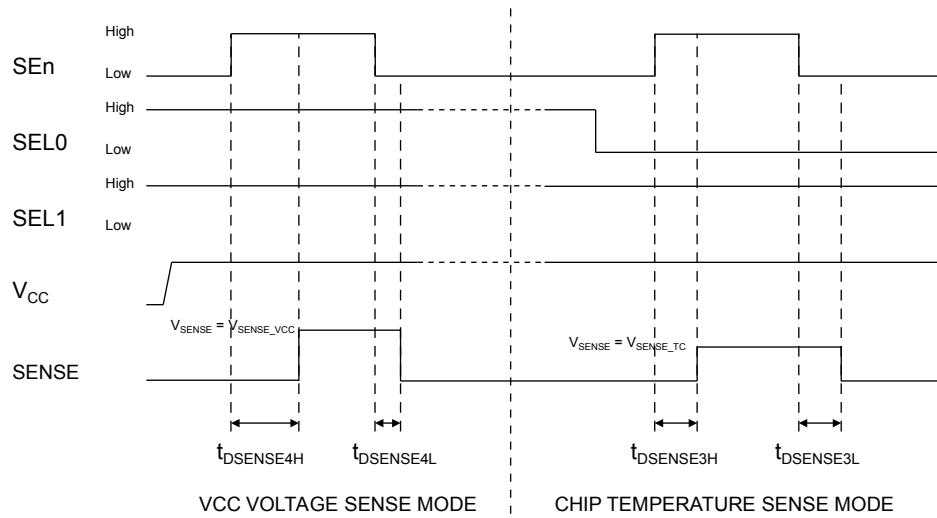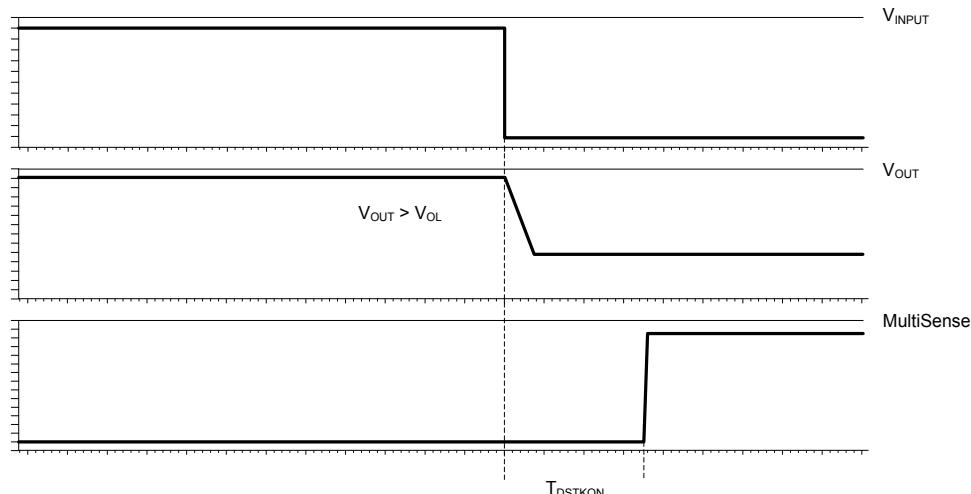
Figure 8. Multisense timings (chip temperature and V_{CC} sense mode) (VN7140AJ only)

GAPGCFT00319

Figure 9. T$_{DSTKON}$

GAPG2609141140CFT

Table 10. Truth table

Mode	Conditions	IN$_X$	FR [1]	SEn	SEL$_X$ [1]	OUT$_X$	MultiSense	Comments
Standby	All logic inputs low	L	L	L	L	L	Hi-Z	Low quiescent current consumption
Normal	Nominal load connected; T$_j$ < 150 °C	L	X	See [2]		L	See [2]	
		H	L			H	See [2]	Outputs configured for auto-restart
		H	H			H	See [2]	Outputs configured for latch-off[1]
Overload	Overload or short to GND causing: T$_j$ > T$_{TSD}$ or ΔT$_j$ > ΔT$_{j\_SD}$	L	X	See [2]		L	See [2]	
		H	L			H	See [2]	Output cycles with temperature hysteresis
		H	H			L	See [2]	Output latches-off[1]
Undervoltage	V$_{CC}$ < V$_{USD}$ (falling)	X	X	X	X	L	Hi-Z	Re-start when V$_{CC}$ > V$_{USD}$ + V$_{USDhyst}$ (rising)
						L	Hi-Z	
OFF-state diagnostics	Short to V$_{CC}$	L	X	See [2]		H	See [2]	
	Open-load	L	X			H	See [2]	External pull-up
Negative output voltage	Inductive loads turn-off	L	X	See [2]		< 0 V	See [2]	

1. *VN7140AJ only*

2. *Refer to Table 11. MultiSense multiplexer addressing*

Table 11. MultiSense multiplexer addressing

SEn	SEL$_1$	SEL$_0$	MUX channel	MultiSense output			
				Normal mode	Overload	OFF-state diag. [1]	Negative output
				SO-8			

SEn	SEL$_1$	SEL$_0$	MUX channel	MultiSense output			
				Normal mode	**Overload**	**OFF-state diag.** [1]	**Negative output**
L	N.A.	N.A.	N.A.	Hi-Z			
H	N.A.	N.A.	Channel diagnostic	$I_{SENSE} = 1/K * I_{OUT}$	$V_{SENSE} = V_{SENSEH}$	$V_{SENSE} = V_{SENSEH}$	Hi-Z
PowerSSO-16							
H	L	L	Channel diagnostic	$I_{SENSE} = 1/K * I_{OUT}$	$V_{SENSE} = V_{SENSEH}$	$V_{SENSE} = V_{SENSEH}$	Hi-Z
H	L	H	Channel diagnostic	$I_{SENSE} = 1/K * I_{OUT}$	$V_{SENSE} = V_{SENSEH}$	$V_{SENSE} = V_{SENSEH}$	Hi-Z
H	H	L	T_{CHIP} Sense	$V_{SENSE} = V_{SENSE\_TC}$			
H	H	H	V_{CC} Sense	$V_{SENSE} = V_{SENSE\_VCC}$			

1. *In case the output channel corresponding to the selected MUX channel is latched off while the relevant input is low, Multisense pin delivers feedback according to OFF-State diagnostic. Example 1: FR = 1; IN = 0; OUT = L (latched); MUX channel = channel 0 diagnostic; Mutisense = 0. Example 2: FR = 1; IN = 0; OUT = latched, $V_{OUT} > V_{OL}$; MUX channel = channel 0 diagnostic; Mutisense = V_{SENSEH}*

2.4 Waveforms

Figure 10. Latch functionality - behavior in hard short-circuit condition ($T_{AMB} \ll T_{TSD}$)

GADG1703171451PS
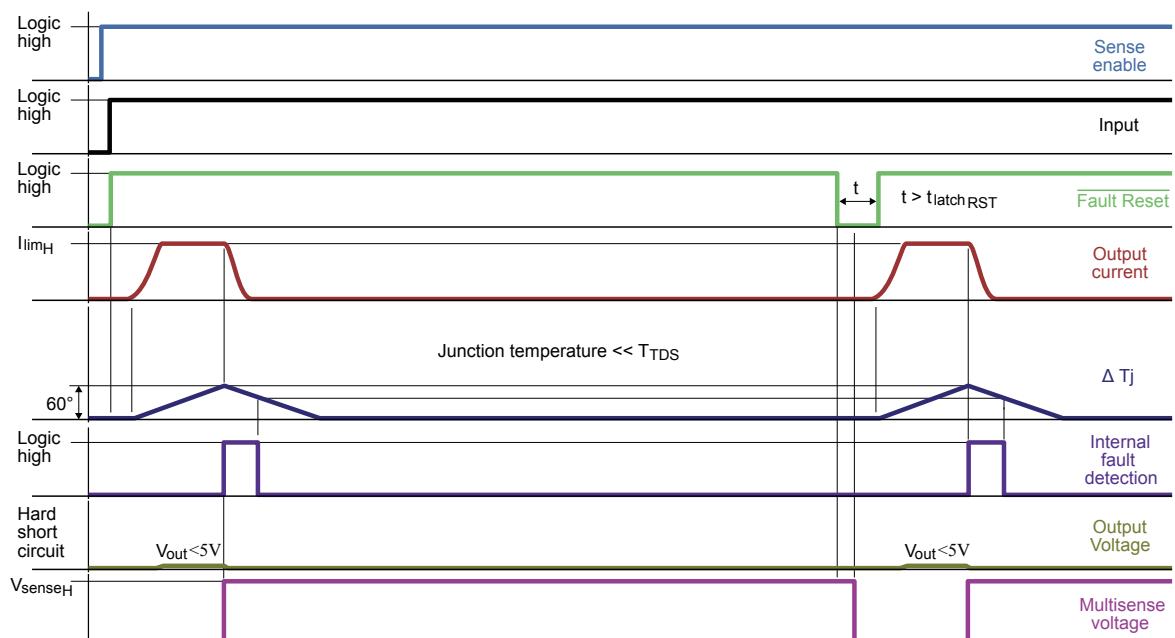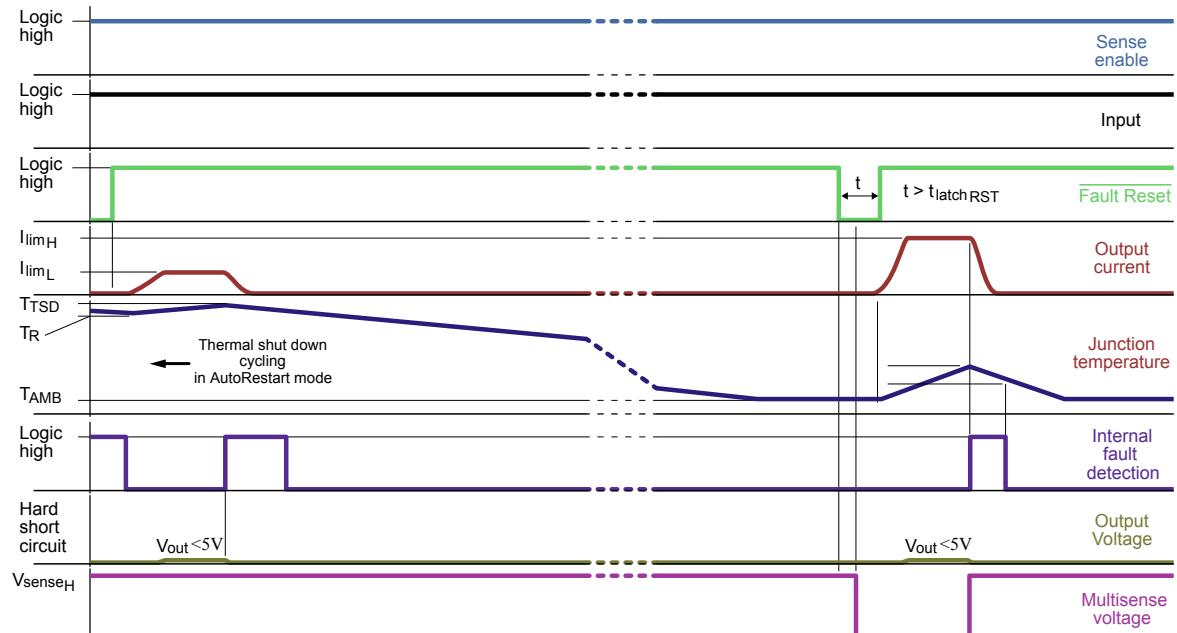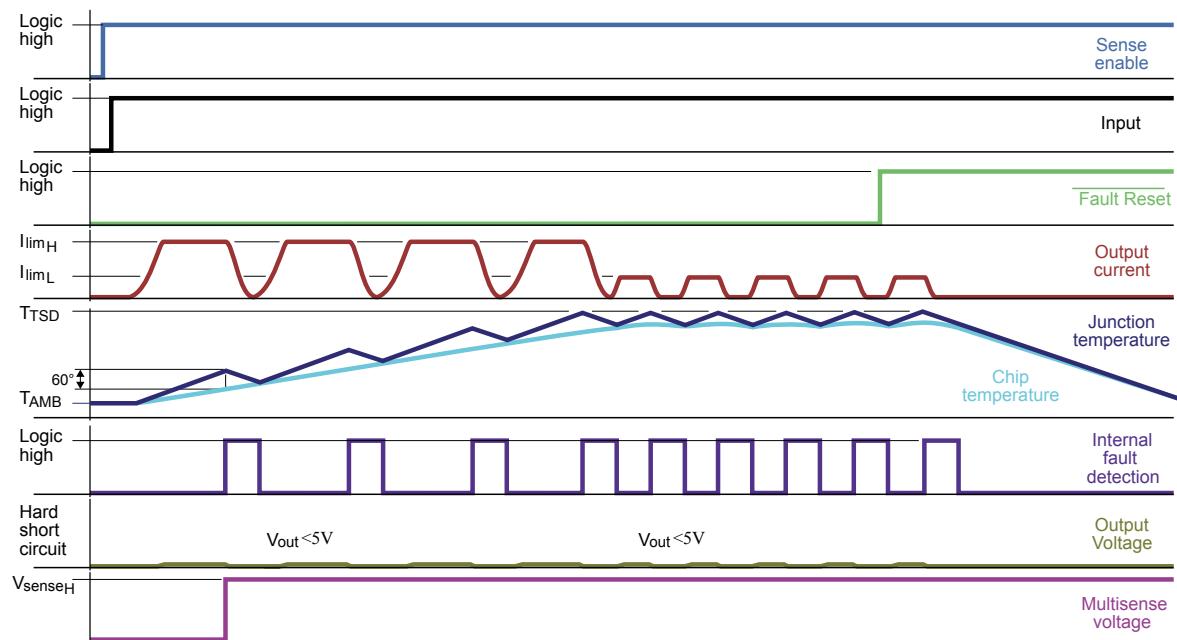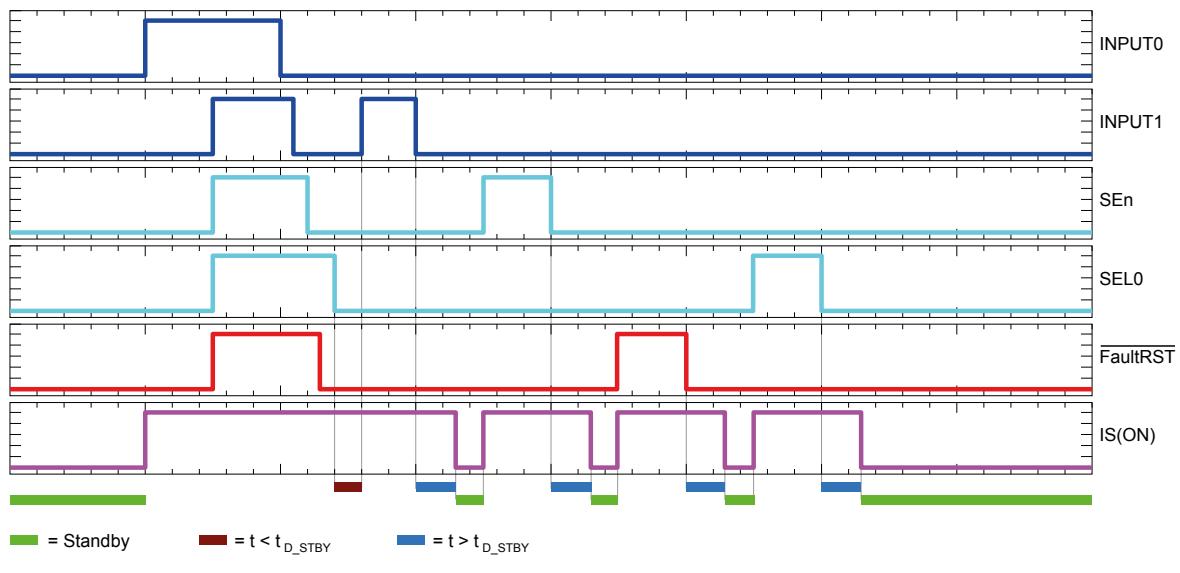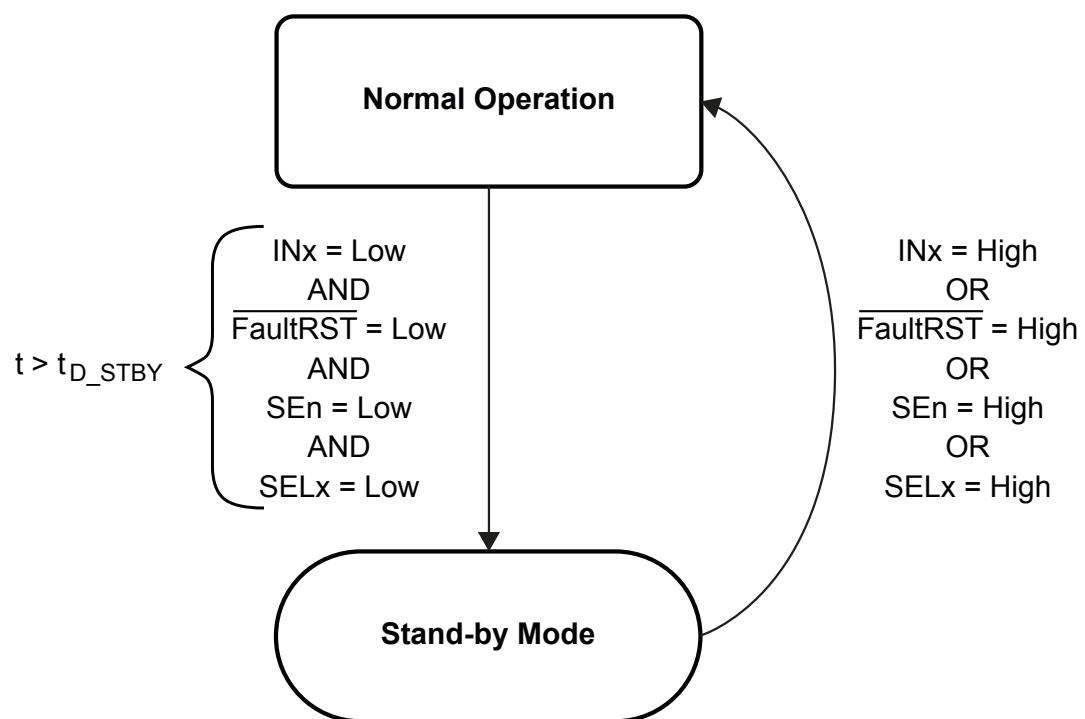
Figure 11. Latch functionality - behavior in hard short-circuit condition

Figure 12. Latch functionality - behavior in hard short-circuit condition (autorestart mode + latch off)

GADG2103171742PS

Figure 13. Standby mode activation

GADG1703171116PS

Figure 14. Standby state diagram

GAPGCFT00598

2.5 Electrical characteristics curves

Figure 15. OFF-state output current

Iloff [nA]

Off State
Vcc = 13V
Vin = Vout = 0

T [°C]

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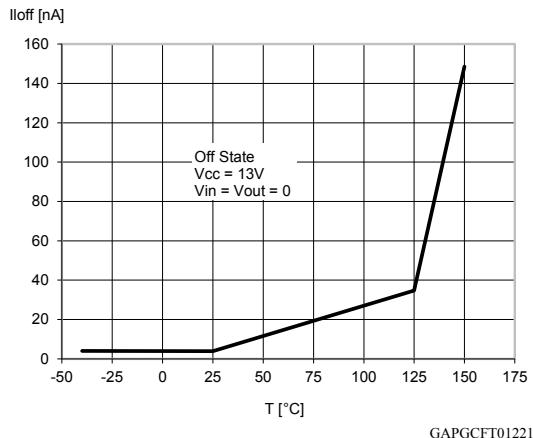
Figure 16. Standby current

ISTBY [µA]

Vcc = 13V

T [°C]

GAPGCFT01222
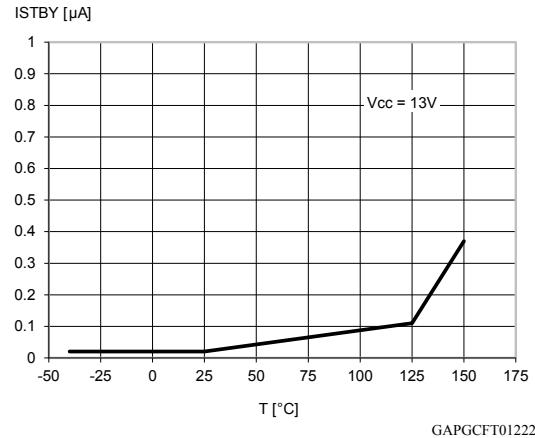
Figure 17. I$_{GND(ON)}$ vs. Tcase

IGND(ON) [mA]

Vcc = 13V
Iout0 = Iout1 = 1A

T [°C]

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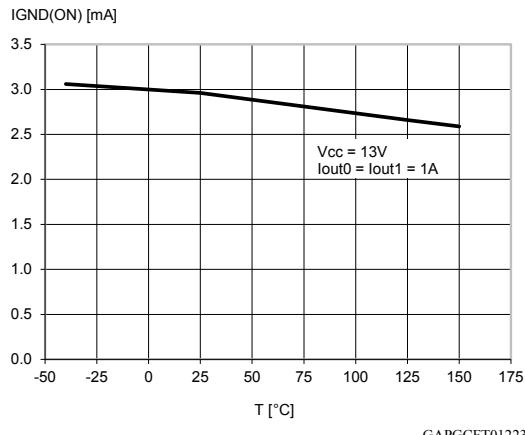
Figure 18. Logic Input high level voltage

ViH, VFRH, VSELH, VSEnH [V]

T [°C]

GAPGCFT01224
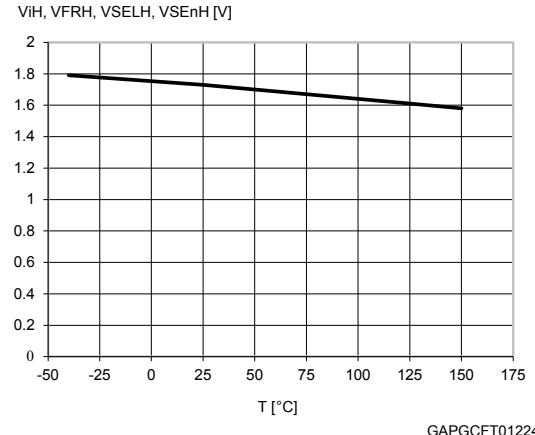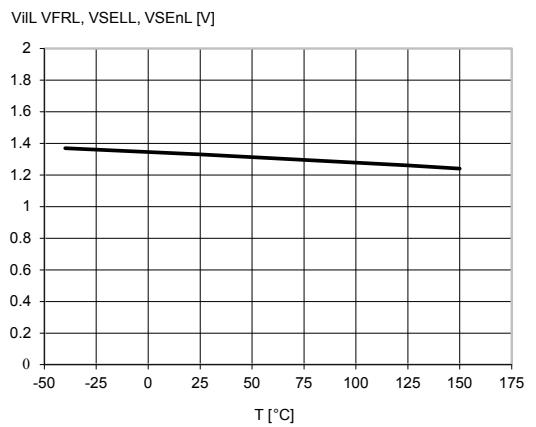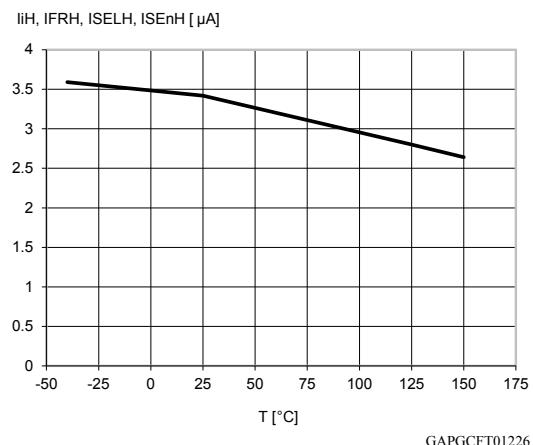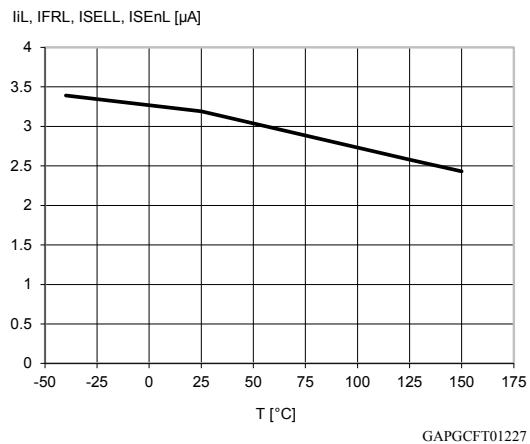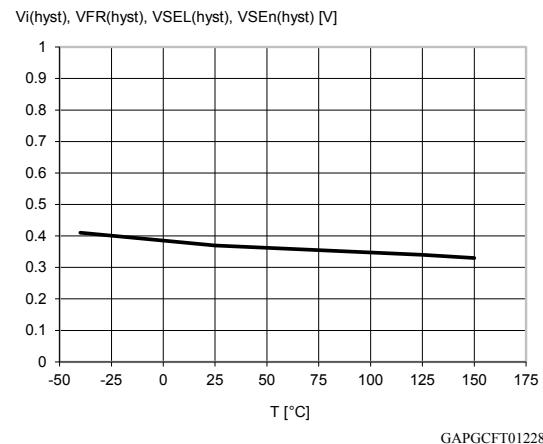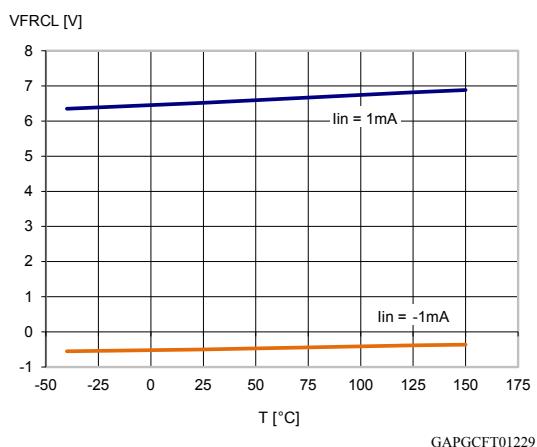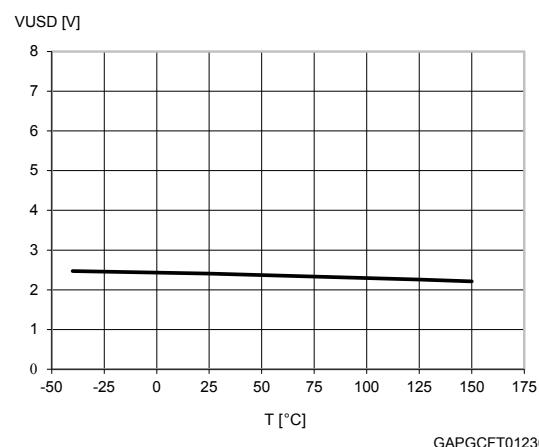
Figure 19. Logic Input low level voltage

VilL VFRL, VSELL, VSEnL [V]

GAPGCFT01225

Figure 20. High level logic input current

IiH, IFRH, ISELH, ISEnH [µA]

GAPGCFT01226

Figure 21. Low level logic input current

IiL, IFRL, ISELL, ISEnL [µA]

GAPGCFT01227

Figure 22. Logic Input hysteresis voltage

Vi(hyst), VFR(hyst), VSEL(hyst), VSEn(hyst) [V]

GAPGCFT01228

Figure 23. FaultRST Input clamp voltage

VFRCL [V]

Iin = 1mA

Iin = -1mA

GAPGCFT01229

Figure 24. Undervoltage shutdown

VUSD [V]

GAPGCFT01230
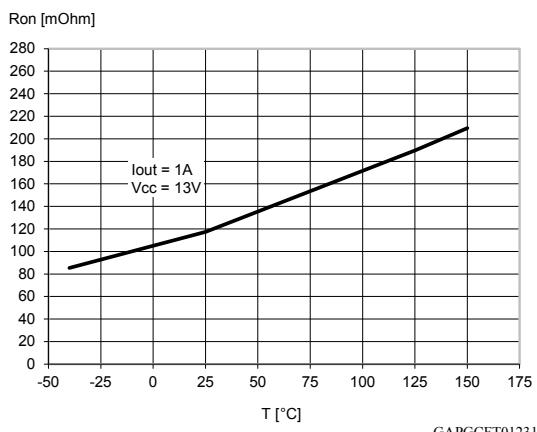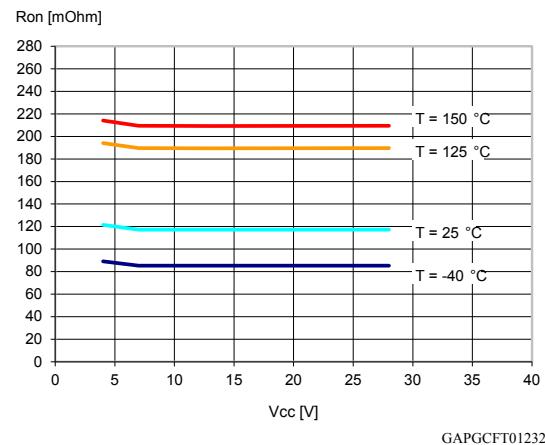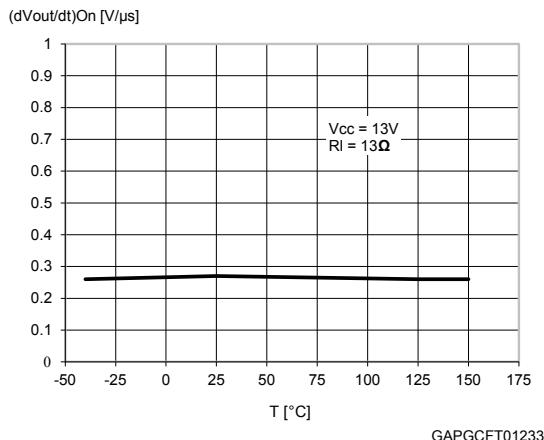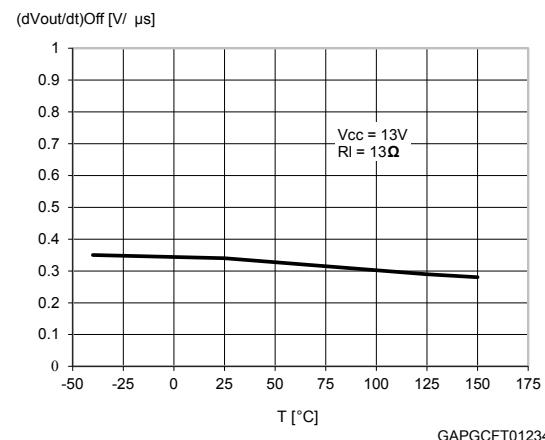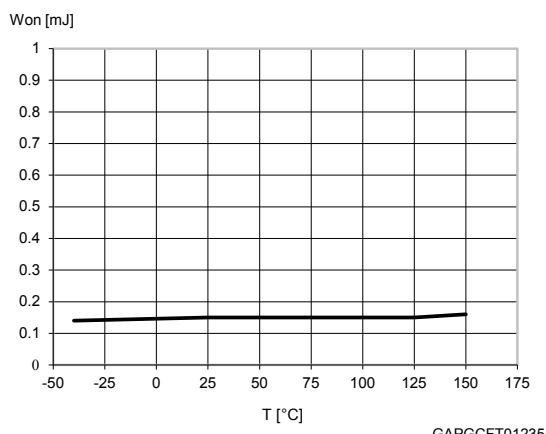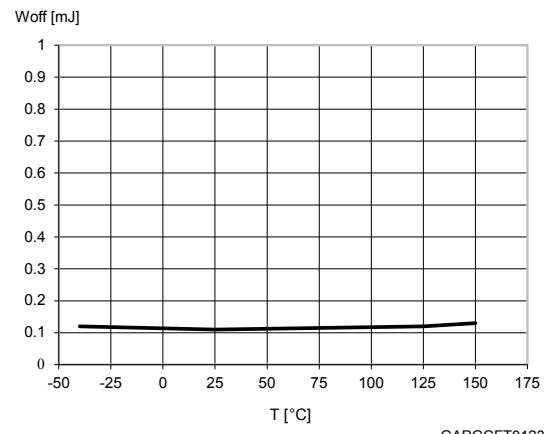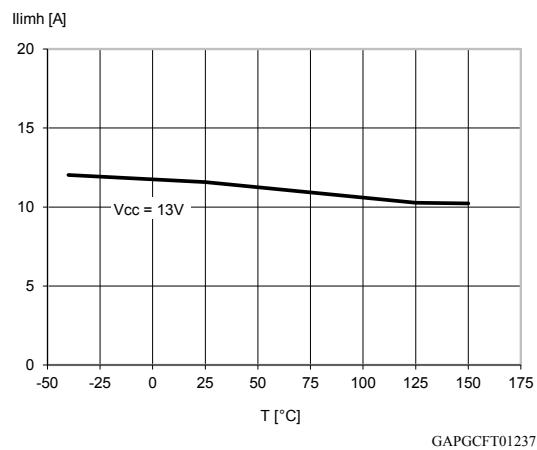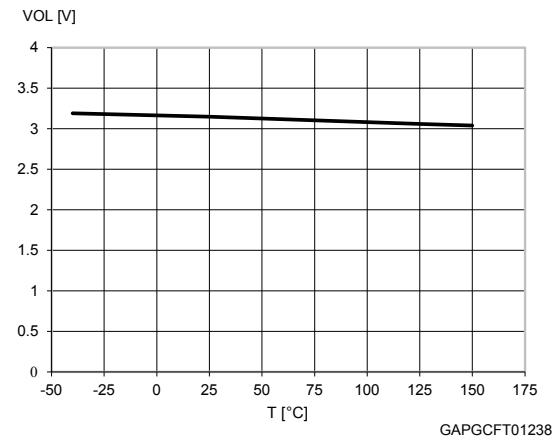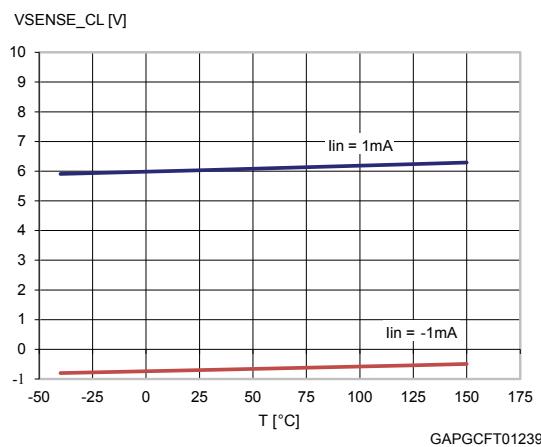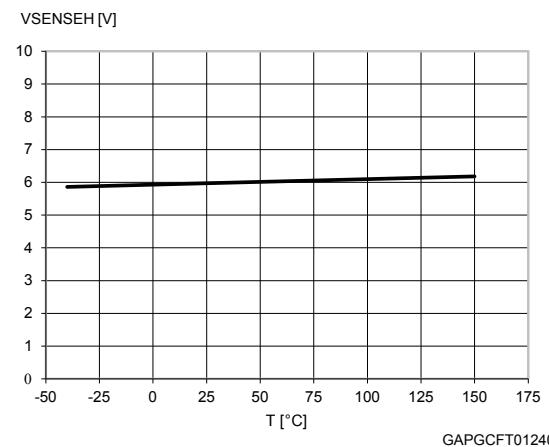
Figure 25. On-state resistance vs. T$_{case}$

Ron [mOhm]

Iout = 1A
Vcc = 13V

T [°C]

GAPGCFT01231

Figure 26. On-state resistance vs. V$_{CC}$

Ron [mOhm]

T = 150 °C

T = 125 °C

T = 25 °C

T = -40 °C

Vcc [V]

GAPGCFT01232

Figure 27. Turn-on voltage slope

(dVout/dt)On [V/µs]

Vcc = 13V
Rl = 13Ω

T [°C]

GAPGCFT01233

Figure 28. Turn-off voltage slope

(dVout/dt)Off [V/ µs]

Vcc = 13V
Rl = 13Ω

T [°C]

GAPGCFT01234

Figure 29. Won vs. T$_{case}$

Won [mJ]

T [°C]

GAPGCFT01235

Figure 30. Woff vs. T$_{case}$

Woff [mJ]

T [°C]

GAPGCFT01236

Figure 31. I_{LIMH} vs. T_{case}

GAPGCFT01237

Figure 32. OFF-state open-load voltage detection threshold

GAPGCFT01238

Figure 33. V_{sense} clamp vs. T_{case}

GAPGCFT01239

Figure 34. V_{senseh} vs. T_{case}

GAPGCFT01240

3 Protections

3.1 Power limitation

The basic working principle of this protection consists of an indirect measurement of the junction temperature swing ΔT_j through the direct measurement of the spatial temperature gradient on the device surface in order to automatically shut off the output MOSFET as soon as ΔT_j exceeds the safety level of ΔT_{j_SD}. According to the voltage level on the $\overline{\text{FaultRST}}$ pin, the output MOSFET switches on and cycles with a thermal hysteresis according to the maximum instantaneous power which can be handled ($\overline{\text{FaultRST}}$ = Low) or remains off ($\overline{\text{FaultRST}}$ = High). The protection prevents fast thermal transient effects and, consequently, reduces thermo-mechanical fatigue.

3.2 Thermal shutdown

In case the junction temperature of the device exceeds the maximum allowed threshold (typically 175°C), it automatically switches off and the diagnostic indication is triggered. According to the voltage level on the $\overline{\text{FaultRST}}$ pin, the device switches on again as soon as its junction temperature drops to T_R ($\overline{\text{FaultRST}}$ = Low) or remains off ($\overline{\text{FaultRST}}$ = High).

3.3 Current limitation

The device is equipped with an output current limiter in order to protect the silicon as well as the other components of the system (e.g. bonding wires, wiring harness, connectors, loads, etc.) from excessive current flow. Consequently, in case of short circuit, overload or during load power-up, the output current is clamped to a safety level, I_{LIMH}, by operating the output power MOSFET in the active region.
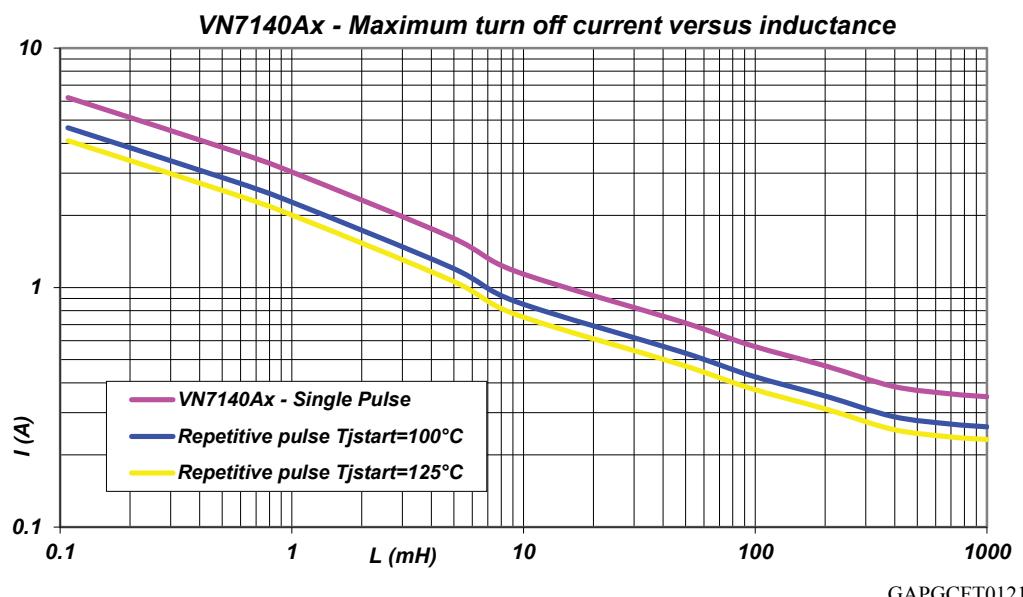
3.4 Negative voltage clamp

In case the device drives inductive load, the output voltage reaches a negative value during turn off. A negative voltage clamp structure limits the maximum negative voltage to a certain value, V_{DEMAG}, allowing the inductor energy to be dissipated without damaging the device.

4   Maximum demagnetization energy (VCC = 16 V)

Figure 35. Maximum turn off current versus inductance

VN7140Ax - Maximum turn off current versus inductance

GAPGCFT01212
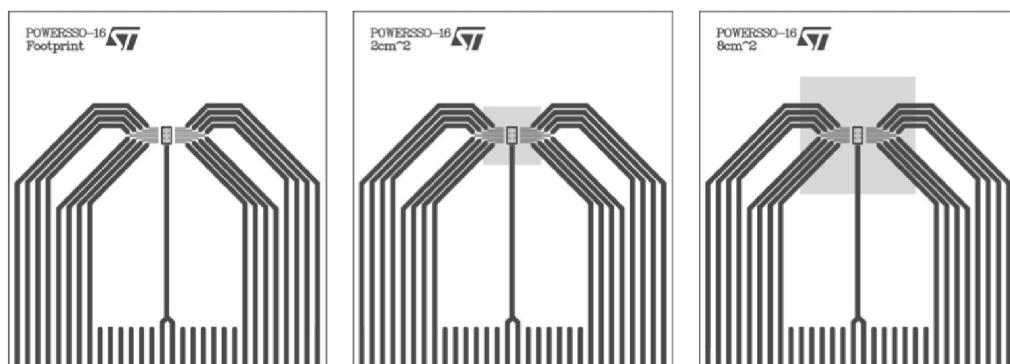
Note: Values are generated with R_L = 0 Ω.

In case of repetitive pulses, T_{jstart} (at the beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

5 Package and PCB thermal data
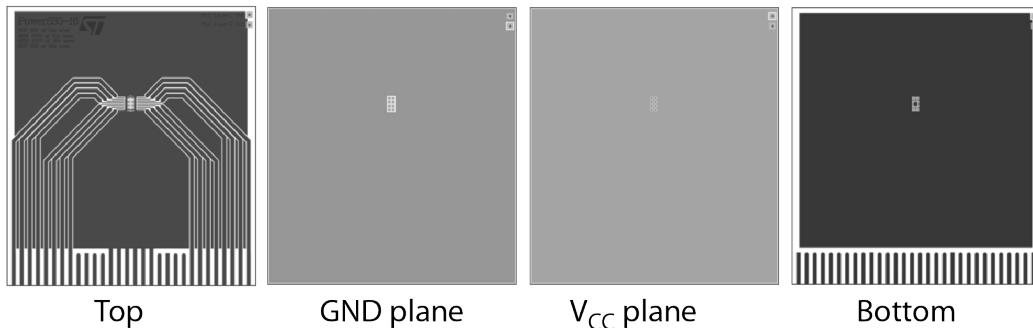
5.1 PowerSSO-16 thermal data

Figure 36. PowerSSO-16 on two-layers PCB (2s0p to JEDEC JESD 51-5)

GAPGCFT00321

Figure 37. PowerSSO-16 on four-layers PCB (2s2p to JEDEC JESD 51-7)

| Top | GND plane | V_{CC} plane | Bottom |
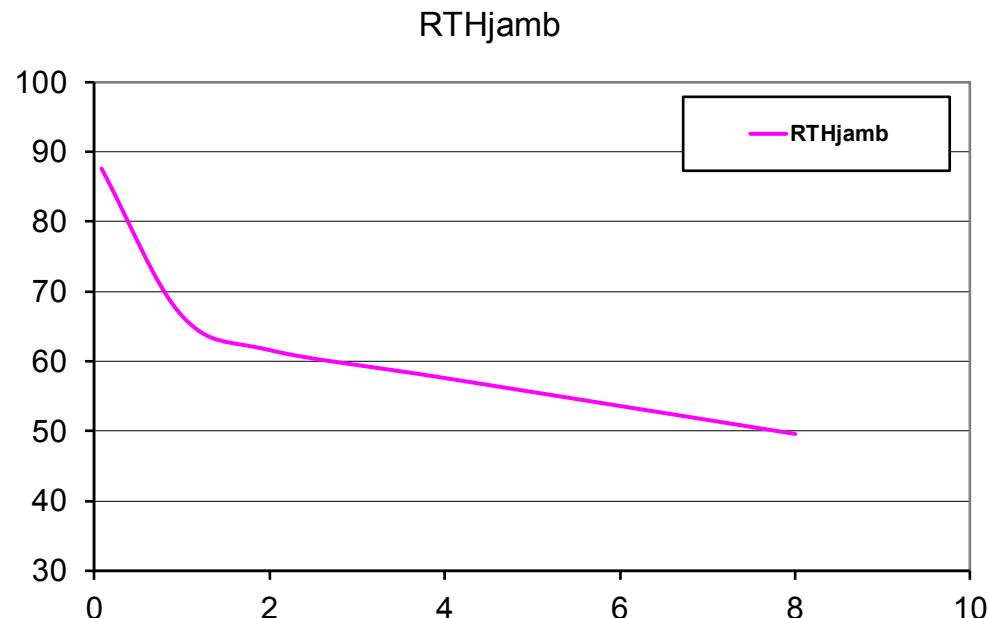
GAPGCFT00322

Table 12. PCB properties

Dimension	Value
Board finish thickness	1.6 mm +/- 10%
Board dimension	77 mm x 86 mm
Board Material	FR4
Copper thickness (top and bottom layers)	0.070 mm
Copper thickness (inner layers)	0.035 mm
Thermal vias separation	1.2 mm
Thermal via diameter	0.3 mm +/- 0.08 mm
Copper thickness on vias	0.025 mm
Footprint dimension (top layer)	2.2 mm x 3.9 mm

Dimension	Value
Heatsink copper area dimension (bottom layer)	Footprint, 2 cm^2 or 8 cm^2

Figure 38. PowerSSO-16 R$_{thj-amb}$ vs PCB copper area in open box free air condition (one channel on)

RTHjamb

RTHj_amb on 4Layer PCB: 26.8°C/W
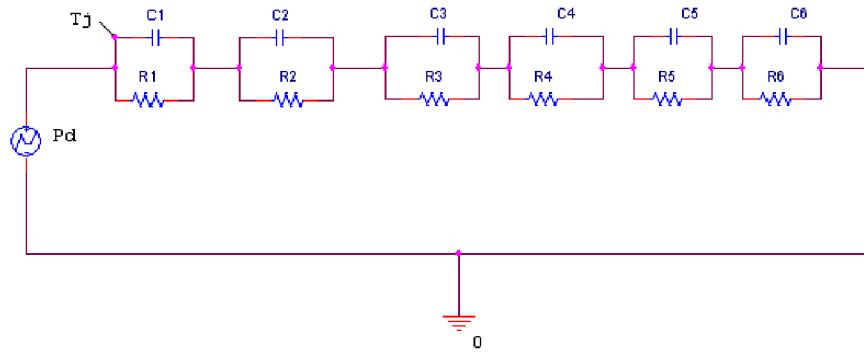
GAPGCFT01213

Figure 39. PowerSSO-16 thermal impedance junction ambient single pulse (one channel on)

Z_{TH} (°C/W)

Cu=foot print
Cu=2 cm2
Cu=8 cm2
4 Layer

Time (s)

GAPGCFT01214

Equation: pulse calculation formula

$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp} (1 - \delta)$

where $\delta = t_P/T$

Figure 40. Thermal fitting model of a double-channel HSD in PowerSSO-16

TAPG2001151031CFT
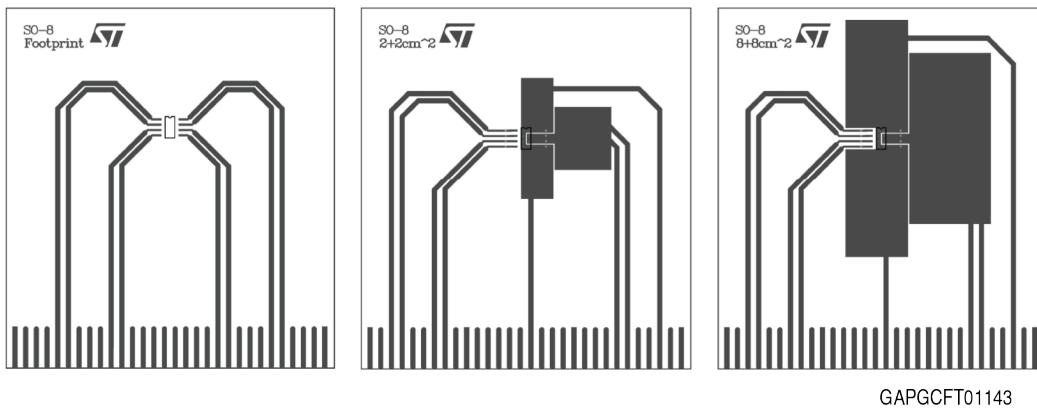
Note: *The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.*

Table 13. Thermal parameters

Area/island (cm^2)	Footprint	2	8	4L
R1 (°C/W)	3.2			
R2 (°C/W)	4.4			
R3 (°C/W)	8	8	8	5
R4 (°C/W)	16	6	6	4
R5 (°C/W)	30	20	10	3
R6 (°C/W)	26	20	18	7
C1 (W.s/°C)	0.00012			
C2 (W.s/°C)	0.005			
C3 (W.s/°C)	0.1			
C4 (W.s/°C)	0.2	0.3	0.3	0.4
C5 (W.s/°C)	0.4	1	1	4
C6 (W.s/°C)	3	5	7	18
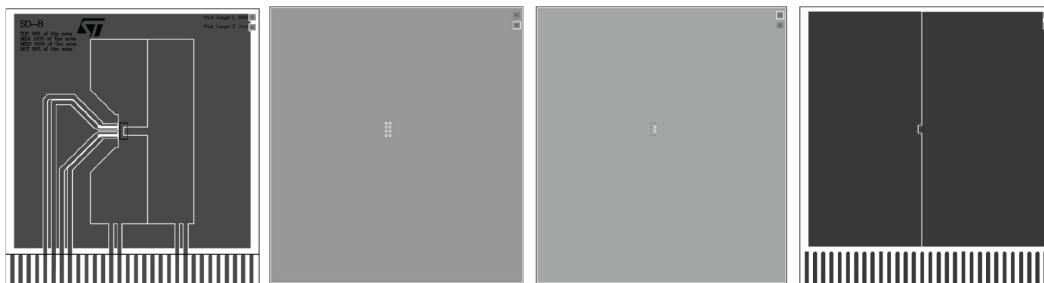
5.2 SO-8 thermal data

Figure 41. **S0-8 on two-layers PCB (2s0p to JEDEC JESD 51-5)**

GAPGCFT01143
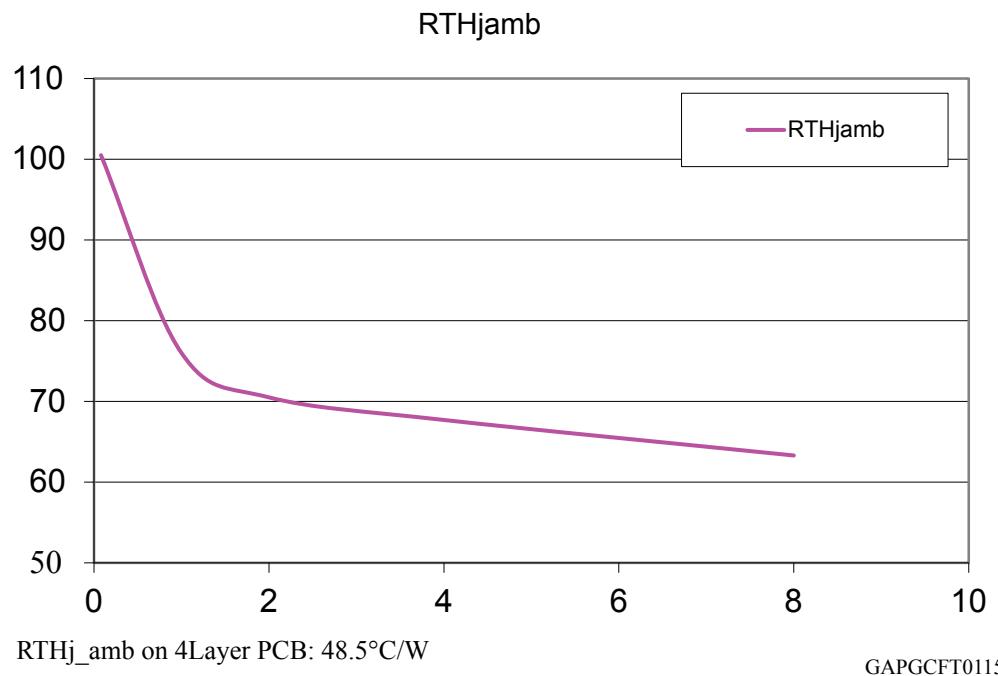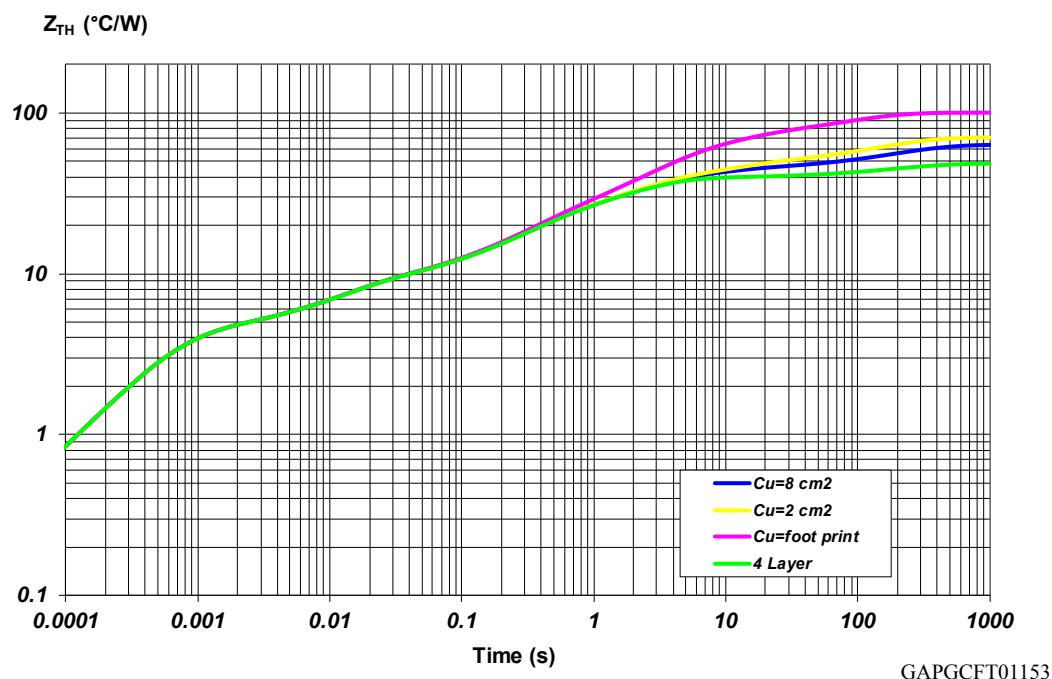
Figure 42. **SO-8 on four-layers PCB (2s2p to JEDEC JESD 51-7)**

GAPGCFT01144
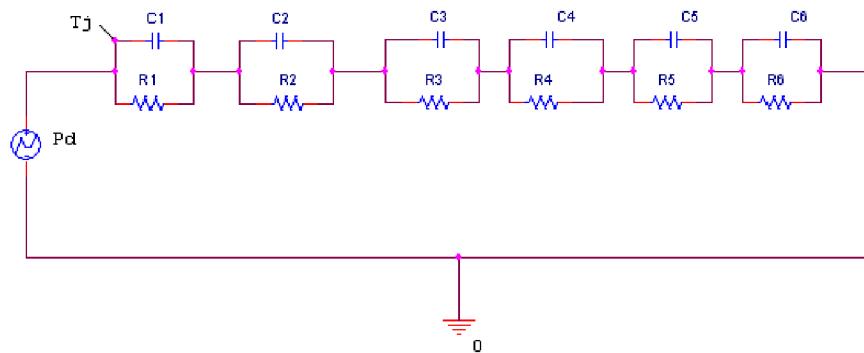
Table 14. **PCB properties**

Dimension	Value
Board finish thickness	1.6 mm +/- 10%
Board dimension	77 mm x 86 mm
Board Material	FR4
Copper thickness (top and bottom layers)	0.070 mm
Copper thickness (inner layers)	0.035 mm
Thermal vias separation	1.2 mm
Thermal via diameter	0.3 mm +/- 0.08 mm
Copper thickness on vias	0.025 mm
Heatsink copper area dimension (bottom layer)	Footprint, 2 + 2 cm^2 or 8 + 8 cm^2

Figure 43. SO-8 R$_{thj-amb}$ vs PCB copper area in open box free air condition (one channel on)

RTHjamb

RTHj_amb on 4Layer PCB: 48.5°C/W

GAPGCFT01152

Figure 44. SO-8 thermal impedance junction ambient single pulse (one channel on)

Z_{TH} (°C/W)

GAPGCFT01153

Equation: pulse calculation formula

$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp} (1 - \delta)$

where $\delta = t_P/T$

Figure 45. Thermal fitting model of a double-channel HSD in SO-8

TAPG2001151031CFT

Note: *The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.*

Table 15. Thermal parameters

Area/island (cm^2)	Footprint	2	8	4L
R1 (°C/W)	4.2			
R2 (°C/W)	4.3			
R3 (°C/W)	10			
R4 (°C/W)	28	17	17	17
R5 (°C/W)	24	12	9	4
R6 (°C/W)	30	23	19	9
C1 (W.s/°C)	0.00012			
C2 (W.s/°C)	0.003			
C3 (W.s/°C)	0.03			
C4 (W.s/°C)	0.1			
C5 (W.s/°C)	0.4	0.8	0.8	0.8
C6 (W.s/°C)	3	7	11	22

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

6.1 PowerSSO-16 package information

Figure 46. PowerSSO-16 package outline
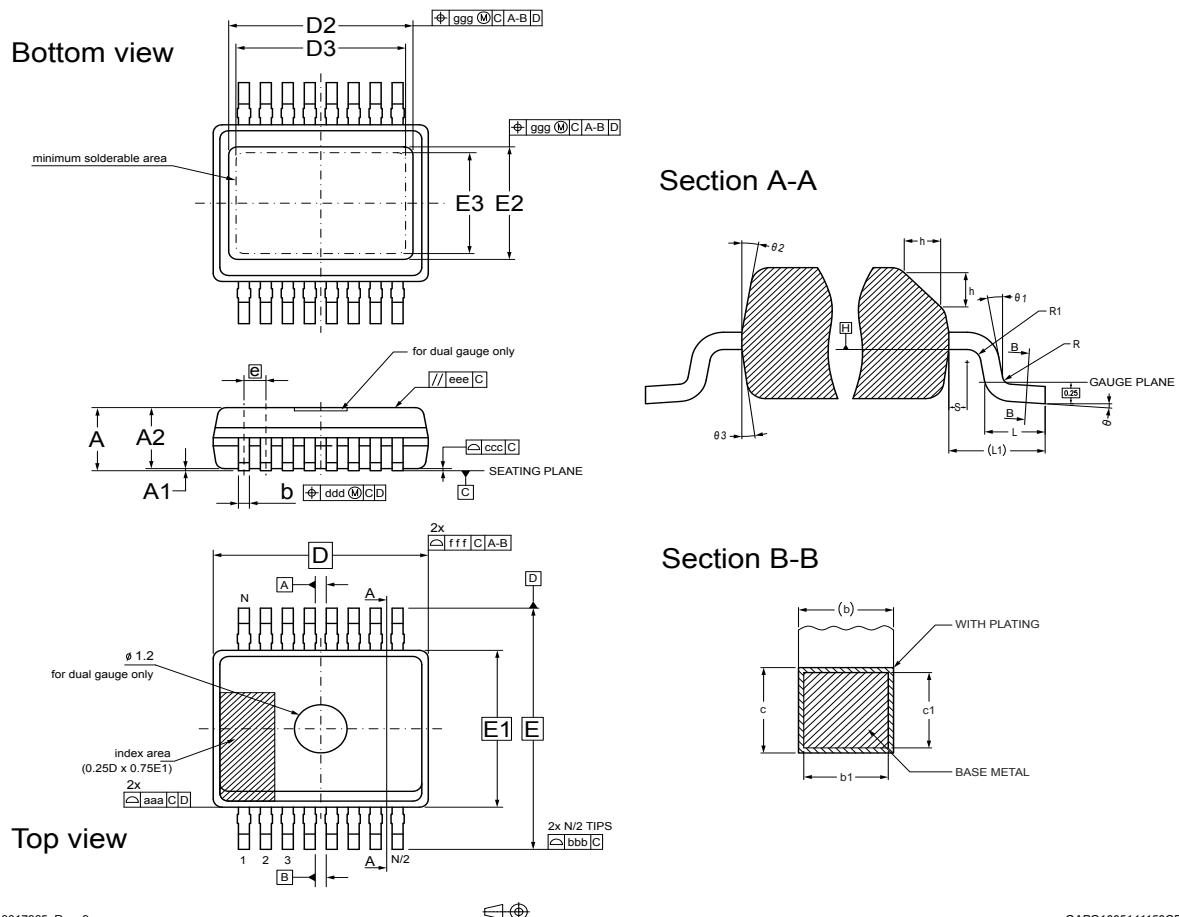
Table 16. PowerSSO-16 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
Θ	0°		8°
Θ1	0°		
Θ2	5°		15°
Θ3	5°		15°
A			1.70
A1	0.00		0.10
A2	1.10		1.60
b	0.20		0.30
b1	0.20	0.25	0.28
c	0.19		0.25
c1	0.19	0.20	0.23
D	4.9 BSC		
D2	2.90		3.50
D3	2.20		
e	0.50 BSC		
E	6.00 BSC		
E1	3.90 BSC		
E2	2.20		2.80
E3	1.50		
h	0.25		0.50
L	0.40	0.60	0.85
L1	1.00 REF		
N	16		
R	0.07		
R1	0.07		
S	0.20		
Tolerance of form and position			
aaa	0.10		
bbb	0.10		
ccc	0.08		
ddd	0.08		
eee	0.10		
fff	0.10		
ggg	0.15		

6.2 SO-8 package information

Figure 47. **SO-8 package outline**

GAPG1605141113CFT
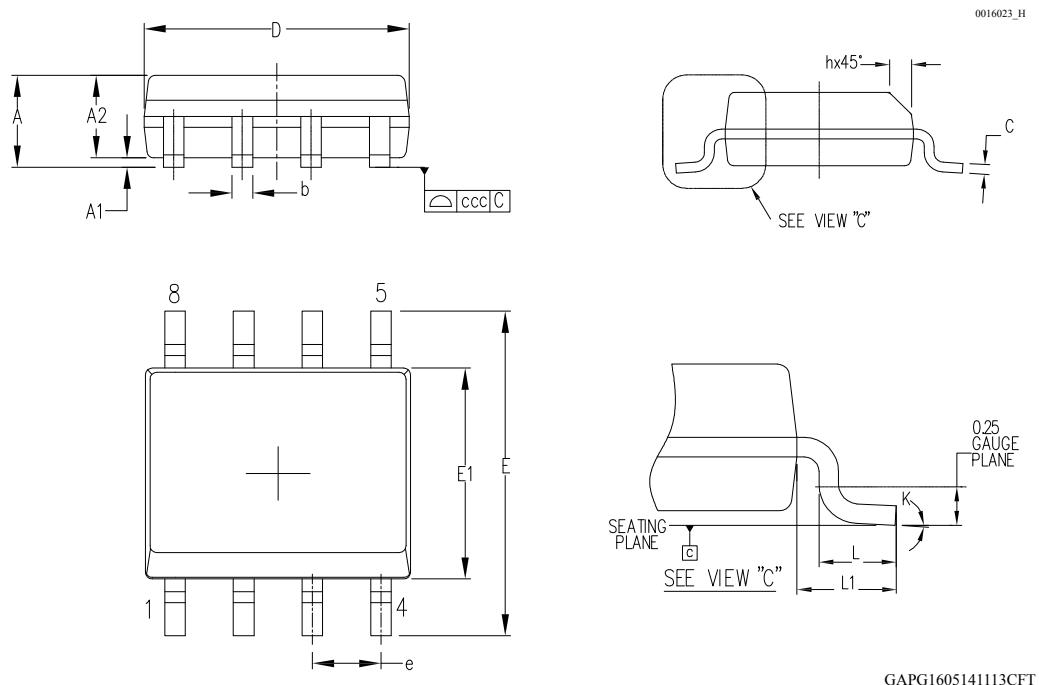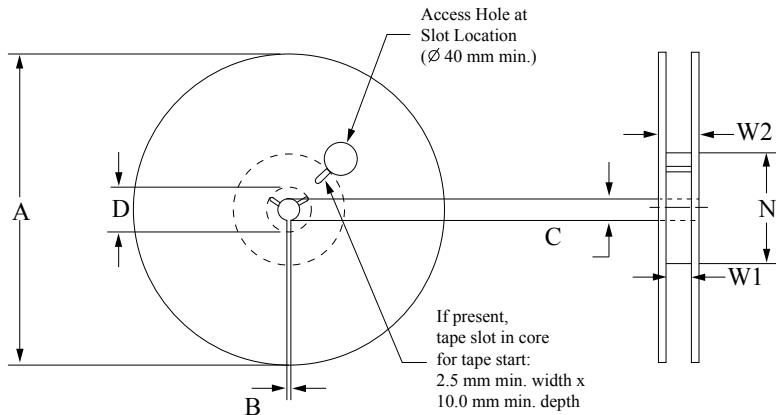
Table 17. **SO-8 mechanical data**

Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.28		0.48
c	0.17		0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
k	0°		8°
ccc			0.10

6.3 PowerSSO-16 packing information

Figure 48. PowerSSO-16 reel 13"
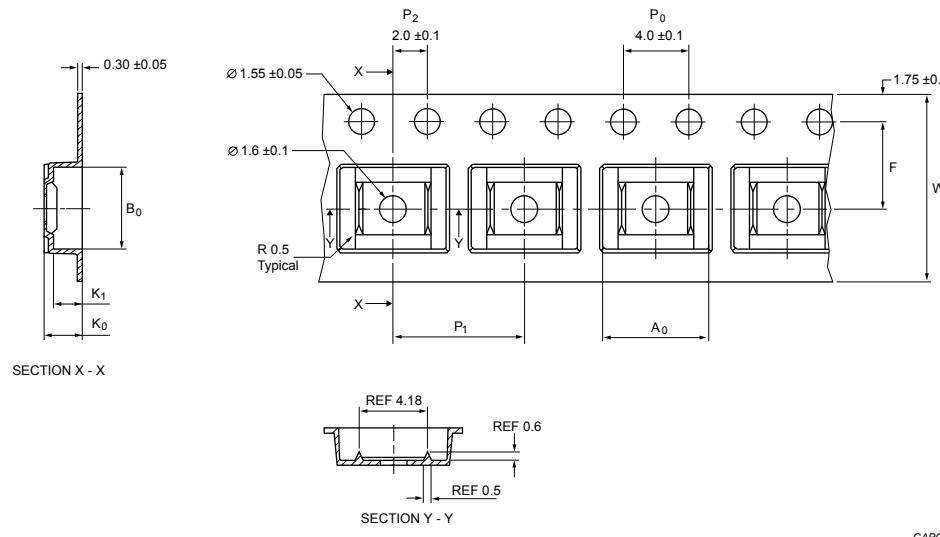
TAPG2004151655CFT

Table 18. Reel dimensions

Description	Value[1]
Base quantity	2500
Bulk quantity	2500
A (max)	330
B (min)	1.5
C (+0.5, -0.2)	13
D (min)	20.2
N	100
W1 (+2 /-0)	12.4
W2 (max)	18.4

1. All dimensions are in mm.
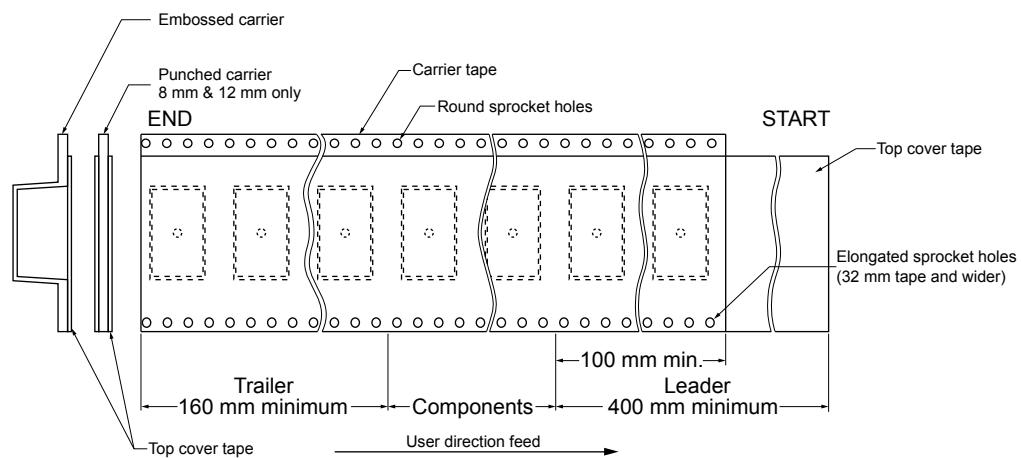
Figure 49. PowerSSO-16 carrier tape

Table 19. PowerSSO-16 carrier tape dimensions

Description	Value[1]
A_0	6.50 ± 0.1
B_0	5.25 ± 0.1
K_0	2.10 ± 0.1
K_1	1.80 ± 0.1
F	5.50 ± 0.1
P_1	8.00 ± 0.1
W	12.00 ± 0.3
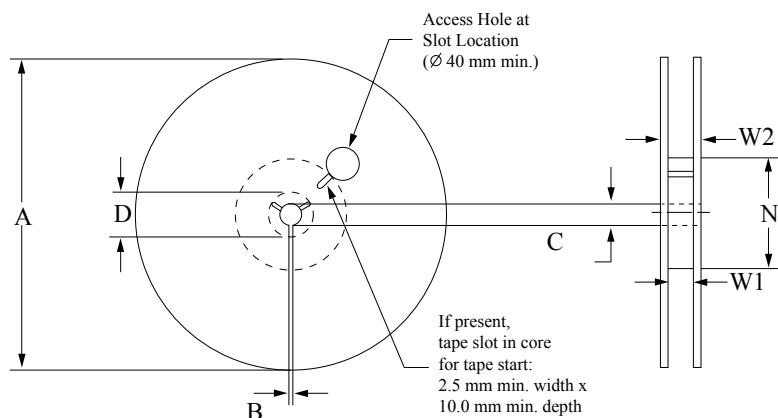
1. All dimensions are in mm.

Figure 50. PowerSSO-16 schematic drawing of leader and trailer tape

6.4 SO-8 packing information

Figure 51. Reel for SO-8

Access Hole at
Slot Location
(∅ 40 mm min.)

If present,
tape slot in core
for tape start:
2.5 mm min. width x
10.0 mm min. depth
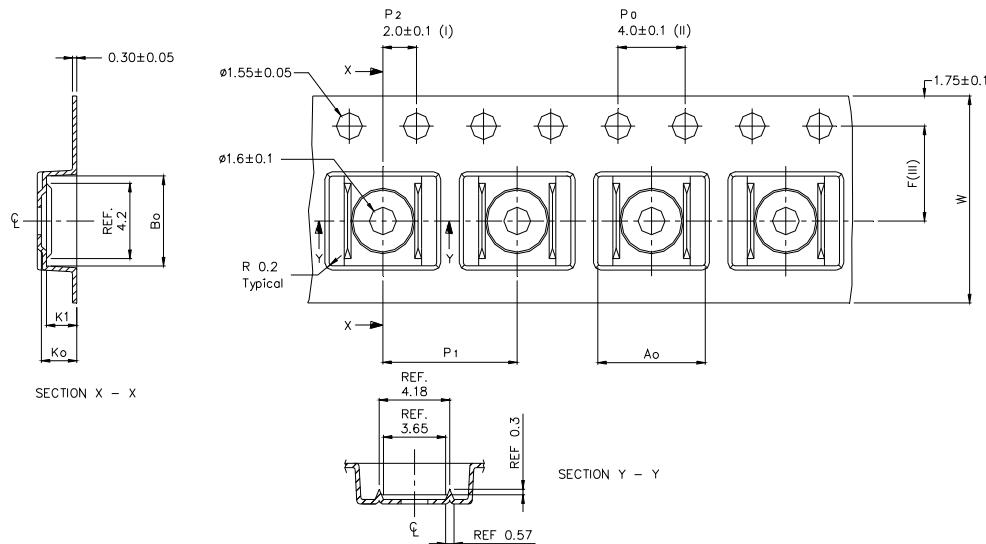
TAPG2004151655CFT

Table 20. Reel dimensions

Description	Value[1]
Base quantity	2500
Bulk quantity	2500
A (max)	330
B (min)	1.5
C (+0.5, -0.2)	13
D (min)	20.2
N	100
W1 (+2/ -0)	12.4
W2 (max)	18.4

1.   All dimensions are in mm.

Figure 52. SO-8 carrier tape
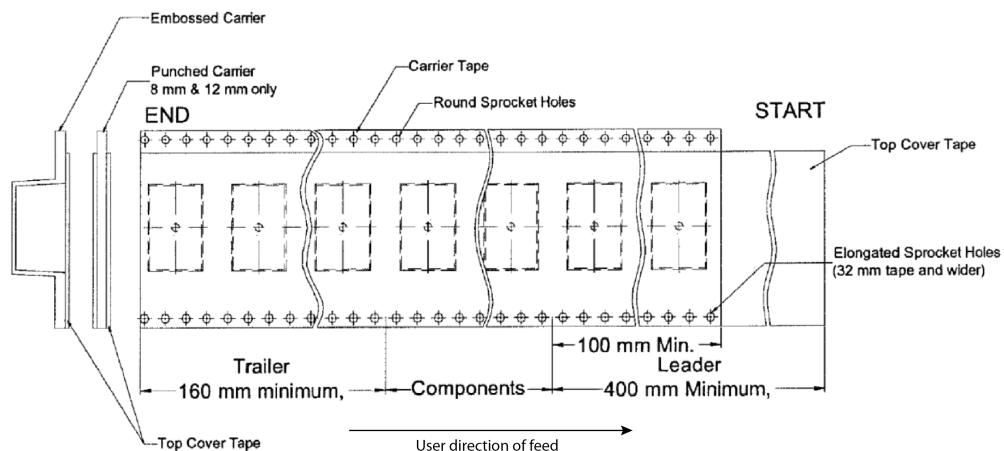
GAPG2105151447CFT

Table 21. SO-8 carrier tape dimensions

Description	Value[1]
A_0	6.50 ± 0.1
B_0	5.30 ± 0.1
K_0	2.20 ± 0.1
K_1	1.90 ± 0.1
F	5.50 ± 0.1
P_1	8.00 ± 0.1
W	12.00 ± 0.3

1.   All dimensions are in mm.
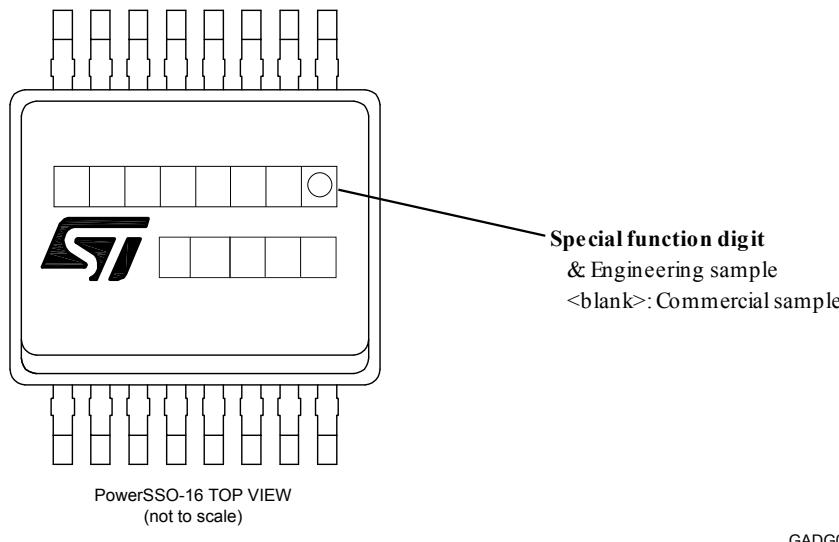
Figure 53. SO-8 schematic drawing of leader and trailer tape

GAPG2004151511CFT

6.5 PowerSSO-16 marking information
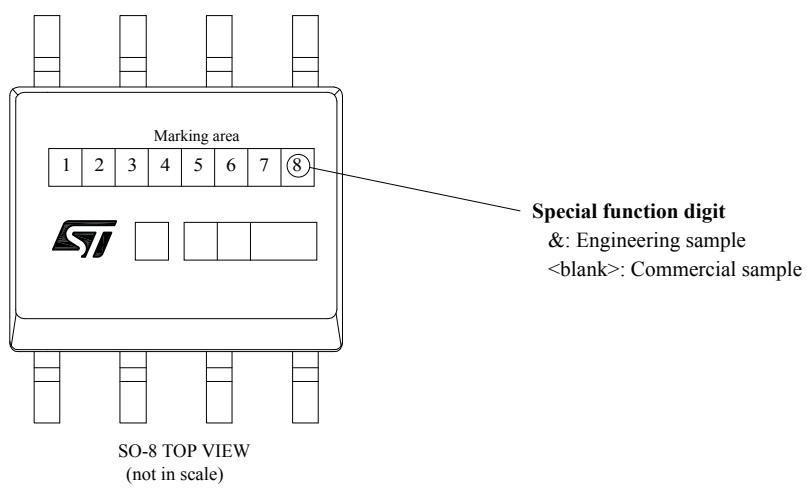
Figure 54. PowerSSO-16 marking information

PowerSSO-16 TOP VIEW
(not to scale)

GADG0310161234SMD

Parts marked as '&' are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

6.6 SO-8 marking information

Figure 55. SO-8 marking information

SO-8 TOP VIEW
(not in scale)

GAPG2705151558CFT

Note: *Engineering Samples: these samples can be clearly identified by a dedicated special symbol in the marking of each unit. These samples are intended to be used for electrical compatibility evaluation only; usage for any other purpose may be agreed only upon written authorization by ST. ST is not liable for any customer usage in production and/or in reliability qualification trials.*

Commercial Samples: fully qualified parts from ST standard production with no usage restrictions

7 Order codes

Table 22. **Device summary**

Package	Order codes
	Tape and reel
PowerSSO-16	VN7140AJTR
SO-8	VN7140ASTR

Revision history

Table 23. Document revision history

Date	Revision	Changes
03-Jun-2015	1	Initial release.
22-Jul-2015	2	Updated cover image. Updated *Table 4: "Thermal data"* Updated following sections: • *Section 6.1: "PowerSSO-16 thermal data"* • *Section 6.2: "SO-8 thermal data"*
13-Oct-2016	3	• Added AEC Q100 qualified in Features section • Updated *Figure 61: "PowerSSO-16 marking information"*
28-Jun-2018	4	Minor text changes in TCASE and VCC monitor.
04-Apr-2019	5	Updated Table 16. PowerSSO-16 mechanical data

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