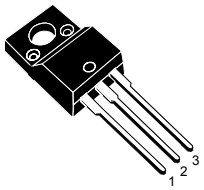
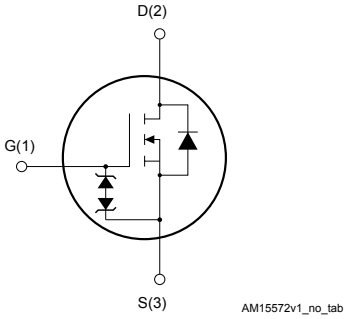
N-channel 800 V, 0.400 Ω typ., 12 A MDmesh™ K5 Power MOSFET in a TO-220FP ultra narrow leads package



TO-220FP
ultra narrow leads



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STFU14N80K5	800 V	0.445 Ω	12 A

- Industry's lowest $R_{DS(on)}$ x area
- Industry's best FoM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This very high voltage N-channel Power MOSFET is designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Product status link
STFU14N80K5

Product summary	
Order code	STFU14N80K5
Marking	14N80K5
Package	TO-220FP ultra narrow leads
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 30	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	12	A
I_D (1)	Drain current (continuous) at T_C = 100 °C	7.4	A
I_D (2)	Drain current (pulsed)	48	A
P_{TOT}	Total power dissipation at T_C = 25 °C	30	W
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s; T_C=25 °C)	2500	V
dv/dt (3)	Peak diode recovery voltage slope	4.5	V/ns
dv/dt (4)	MOSFET dv/dt ruggedness	50	
T_{stg}	Storage temperature range	- 55 to 150	°C
T_J	Operating junction temperature range		

1. *Limited by maximum junction temperature.*
2. *Pulse width limited by safe operating area.*
3. *I_{SD} ≤ 12 A, di/dt = 100 A/µs; V_{DS} (peak) < $V_{(BR)DSS}$, V_{DD}= 640 V*
4. *V_{DS} ≤ 640 V*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	4.2	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	62.5	°C/W

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	4	A
E_{AS}	Single pulse avalanche energy (starting Tj = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	270	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 4. On/off-state

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	800			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 800 V			1	µA
		V_{GS} = 0 V, V_{DS} = 800 V T_C = 125 °C(1)			50	µA
I_{GSS}	Gate body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 6 A		0.400	0.445	Ω

1. *Defined by design, not subject to production test.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	620	-	pF
C_{oss}	Output capacitance		-	60	-	pF
C_{rss}	Reverse transfer capacitance		-	0.8	-	pF
$C_{o(tr)}$ (1)	Equivalent capacitance time related	V_{DS} = 0 to 640 V, V_{GS} = 0 V	-	107	-	pF
$C_{o(er)}$ (2)	Equivalent capacitance energy related		-	39	-	pF
R_g	Intrinsic gate resistance	f = 1 MHz , I_D= 0 A	-	6.5	-	Ω
Q_g	Total gate charge	V_{DD} = 640 V, I_D = 12 A V_{GS}= 0 to 10 V (see Figure 15. Test circuit for gate charge behavior	-	22	-	nC
Q_{gs}	Gate-source charge		-	4.3	-	nC
Q_{gd}	Gate-drain charge		-	16.5	-	nC

1. *Time related is defined as a constant equivalent capacitance giving the same charging time as Coss when V_{DS} increases from 0 to 80% V_{DSS}*
2. *Energy related is defined as a constant equivalent capacitance giving the same stored energy as Coss when V_{DS} increases from 0 to 80% V_{DSS}*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD}= 400 V, I_D =6 A, R_G = 4.7 Ω	-	12.5	-	ns
t_r	Rise time	V_{GS} = 10 V	-	8	-	ns
$t_{d(off)}$	Turn-off delay time	see (Figure 14. Test circuit for resistive load switching times and	-	33	-	ns
t_f	Fall time	Figure 19. Switching time waveform)	-	10	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		12	A
I_{SDM} (1)	Source-drain current (pulsed)		-		48	A
V_{SD} (2)	Forward on voltage	I_{SD} = 12 A, V_{GS} = 0 V	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 12 A, di/dt = 100 A/µs,V_{DD} = 60 V (see)Figure 16. Test circuit for inductive load switching and diode recovery times	-	365		ns
Q_{rr}	Reverse recovery charge		-	4.77		µC
I_{RRM}	Reverse recovery current		-	26		A
t_{rr}	Reverse recovery time	I_{SD} = 12 A, di/dt = 100 A/µs V_{DD} = 60 V, T_j = 150 °C (see)Figure 16. Test circuit for inductive load switching and diode recovery times	-	485		ns
Q_{rr}	Reverse recovery charge		-	5.85		µC
I_{RRM}	Reverse recovery current		-	24		A

1. *Pulse width limited by safe operating area*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%*

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	I_{GS}= ± 1mA, I_D= 0 A	30	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection,thus eliminating the need for additional external componentry.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

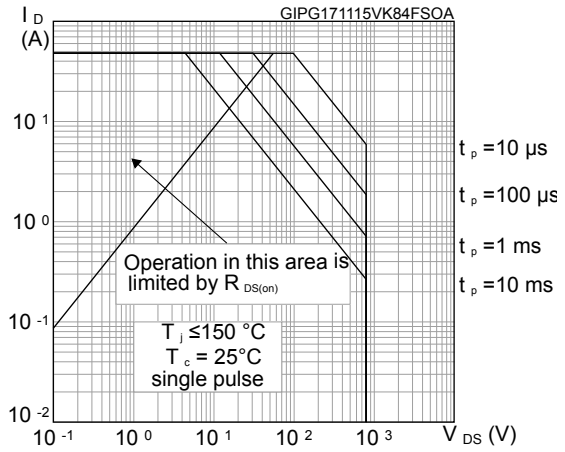


Figure 2. Thermal impedance

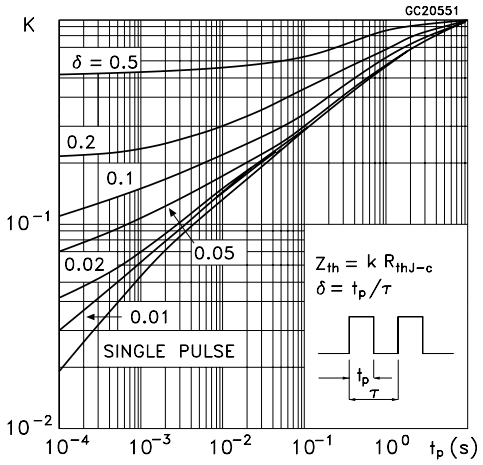


Figure 3. Output characteristics

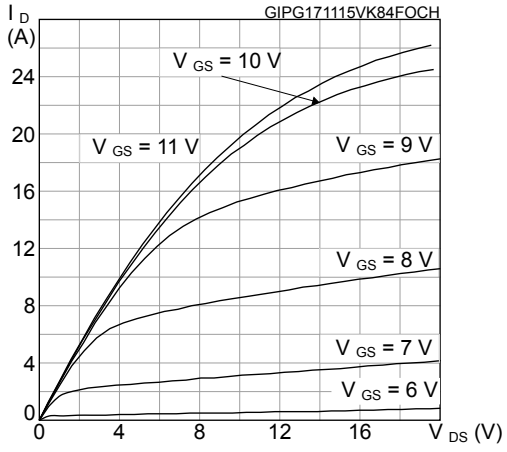


Figure 4. Transfer characteristics

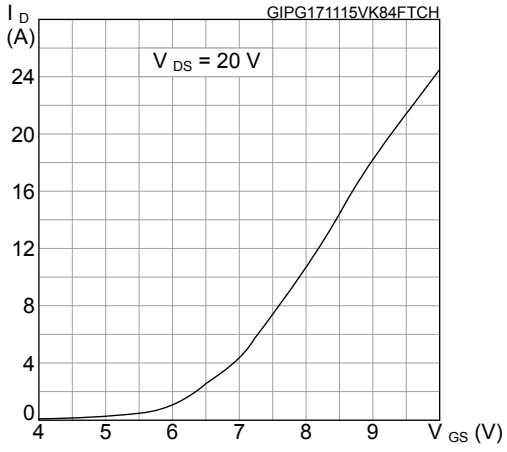


Figure 5. Gate charge vs gate-source voltage

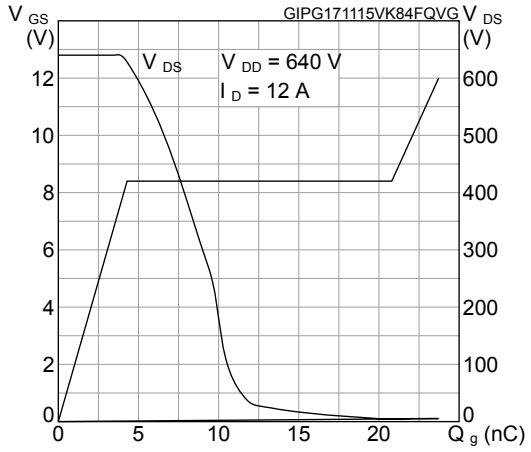


Figure 6. Static drain-source on-resistance

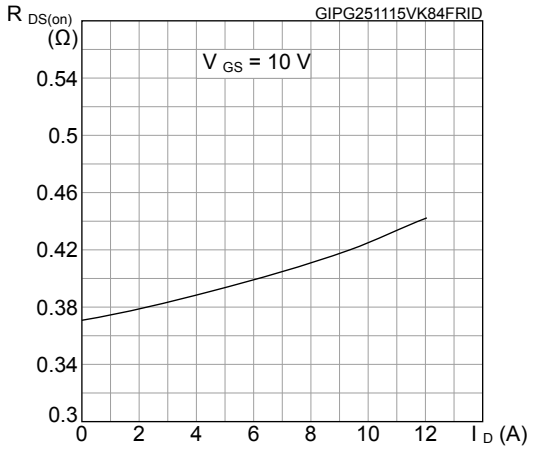


Figure 7. Capacitance variations

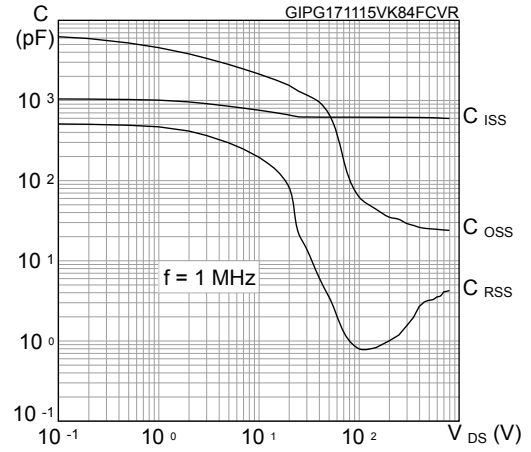


Figure 8. Normalized gate threshold voltage vs temperature

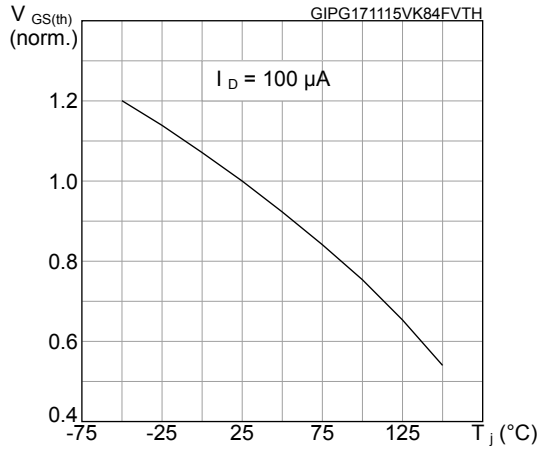


Figure 9. Normalized on-resistance vs temperature

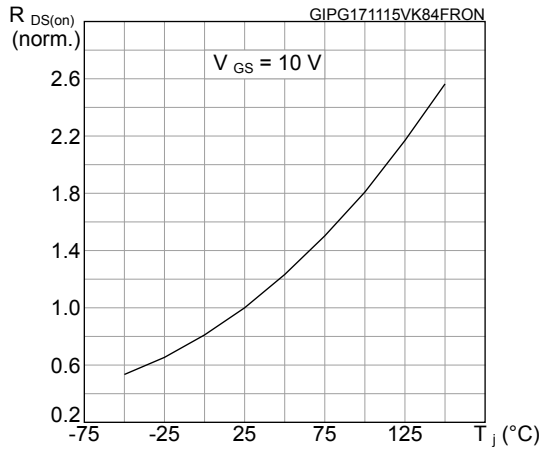


Figure 10. Normalized $V_{(BR)DSS}$ vs temperature

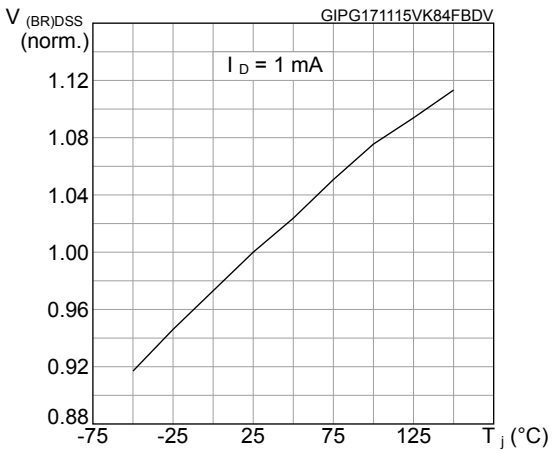


Figure 11. Maximum avalanche energy vs starting T_J

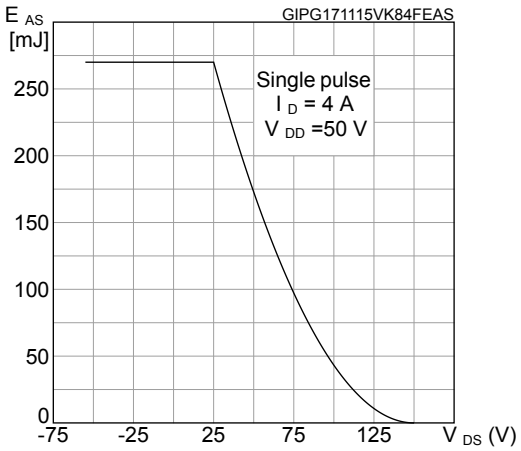


Figure 12. Source-drain diode forward characteristics

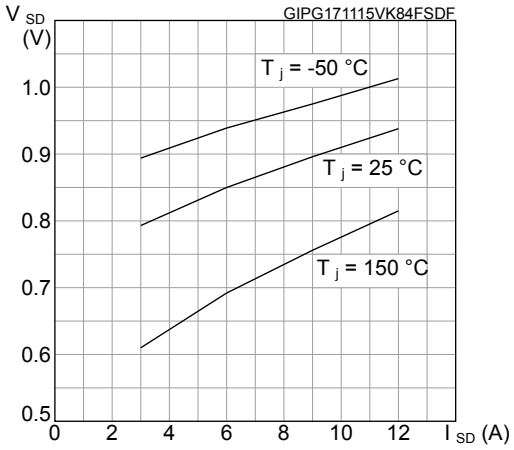
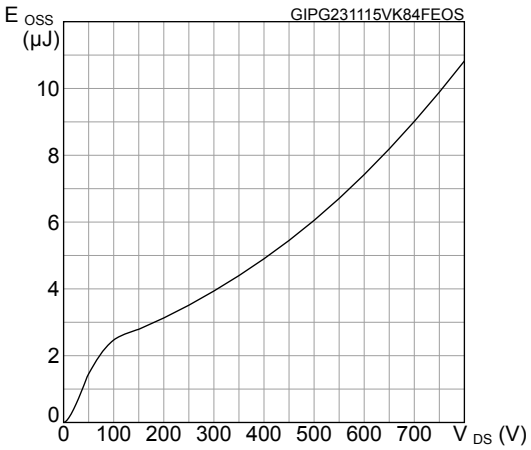


Figure 13. Maximum avalanche energy vs starting T_J



3 Test circuits

Figure 14. Test circuit for resistive load switching times

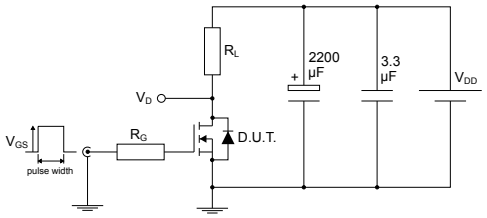


Figure 15. Test circuit for gate charge behavior

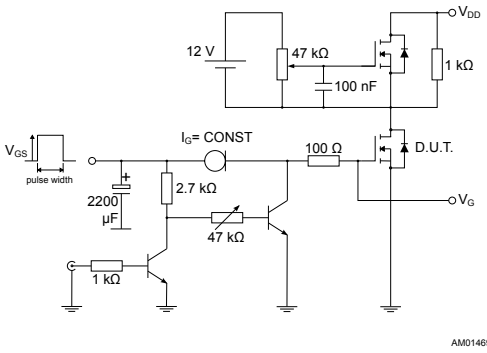


Figure 16. Test circuit for inductive load switching and diode recovery times

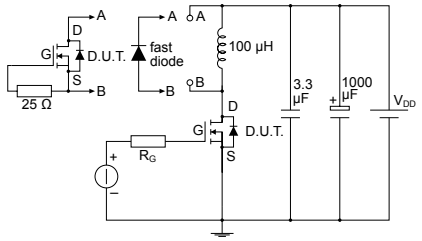


Figure 17. Unclamped inductive load test circuit

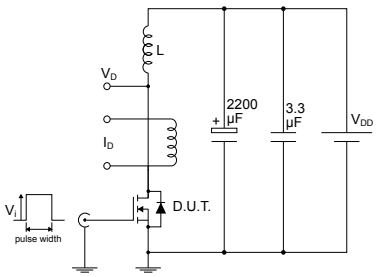


Figure 18. Unclamped inductive waveform

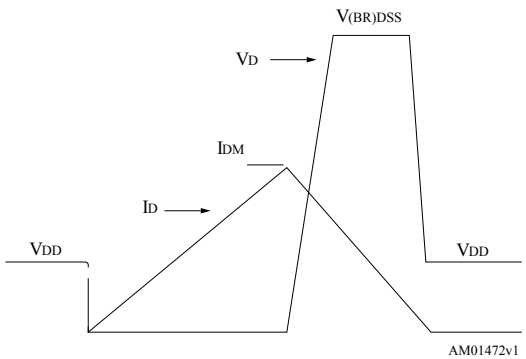
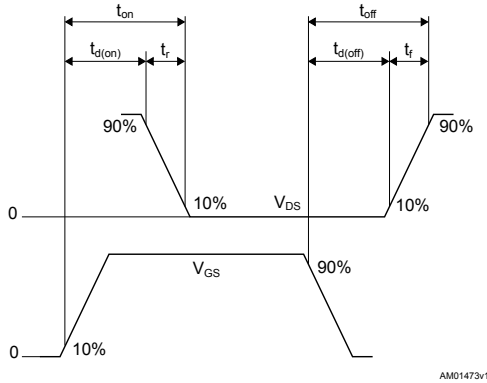


Figure 19. Switching time waveform

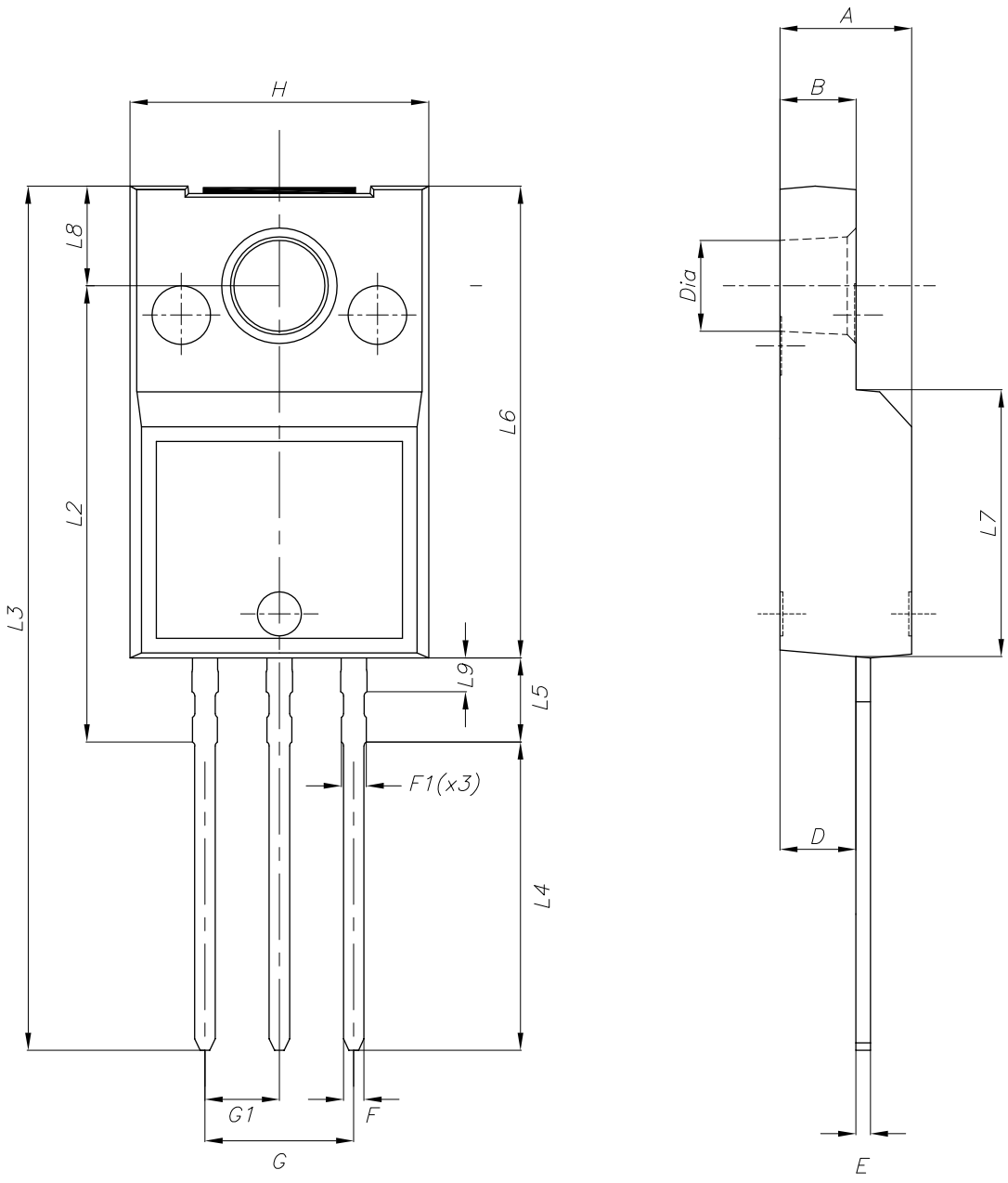


4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 TO-220FP ultra narrow leads package information

Figure 20. TO-220FP ultra narrow leads package outline



8576148_2

Table 9. **TO-220FP ultra narrow leads mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
E	0.45		0.60
F	0.65		0.75
F1	-		0.90
G	4.95		5.20
G1	2.40	2.54	2.70
H	10.00		10.40
L2	15.10		15.90
L3	28.50		30.50
L4	10.20		11.00
L5	2.50		3.10
L6	15.60		16.40
L7	9.00		9.30
L8	3.20		3.60
L9	-		1.30
Dia.	3.00		3.20

Revision history

Table 10. **Document revision history**

Date	Revision	Changes
10-Jan-2019	1	First release.

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

单击下面可查看定价，库存，交付和生命周期等信息

>>STMicro(意法半导体)