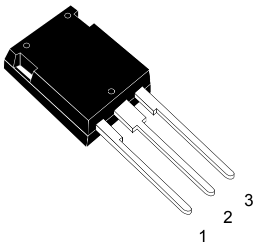
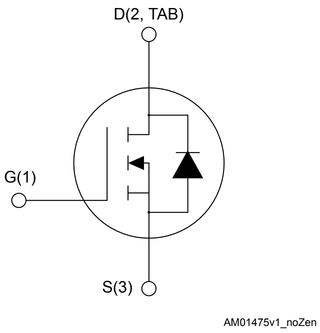
STY139N65M5

Datasheet

N-channel 650 V, 14 mΩ typ., 130 A MDmesh M5 Power MOSFET in a Max247 package



Max247



Product status link
STY139N65M5

Product summary	
Order code	STY139N65M5
Marking	139N65M5
Package	Max247
Packing	Tube

Features

Order code	V_{DS} at T_J max.	$R_{DS(on)}$ max.	I_D
STY139N65M5	710 V	17 mΩ	130 A

- Extremely low $R_{DS(on)}$
- Low gate charge and input capacitance
- Excellent switching performance
- 100% avalanche tested

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET based on the MDmesh M5 innovative vertical process technology combined with the well-known PowerMESH horizontal layout. The resulting product offers extremely low on-resistance, making it particularly suitable for applications requiring high power and superior efficiency.

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±25	V
I_D	Drain current (continuous) at T_C = 25 °C	130	A
	Drain current (continuous) at T_C = 100 °C	78	
I_{DM}(1)	Drain current (pulsed)	520	A
P_{TOT}	Total power dissipation at T_C = 25 °C	625	W
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_J max.)	12	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	2400	mJ
dv/dt(2)	Peak diode recovery voltage slope	15	V/ns
T_{stg}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range		°C

1. *Pulse width is limited by safe operating area.*
2. *I_{SD} ≤ 130 A, di/dt ≤ 400 A/μs, V_{DS} (peak) < $V_{(BR)DSS}$, V_{DD} = 400 V.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.2	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	30	°C/W

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	650			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 650 V			10	µA
		V_{GS} = 0 V, V_{DS} = 650 V, T_C = 125 °C(1)			100	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 65 A		14	17	mΩ

1. *Specified by design, not tested in production.*

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	15600	-	pF
C_{oss}	Output capacitance		-	365	-	pF
C_{rss}	Reverse transfer capacitance		-	9	-	pF
$C_{o(tr)}$(1)	Equivalent capacitance time related	V_{DS} = 0 to 520 V, V_{GS} = 0 V	-	1559	-	pF
$C_{o(er)}$(2)	Equivalent capacitance energy related		-	360	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	-	1.2	-	Ω
Q_g	Total gate charge	V_{DD} = 520 V, I_D = 65 A	-	363	-	nC
Q_{gs}	Gate-source charge	V_{GS} = 0 to 10 V	-	88	-	nC
Q_{gd}	Gate-drain charge	(see Figure 14. Test circuit for gate charge behavior)	-	164	-	nC

1. *$C_{o(tr)}$ is an equivalent capacitance that provides the same charging time as C_{oss} while V_{DS} is rising from 0 V to the stated value.*
2. *$C_{o(er)}$ is an equivalent capacitance that provides the same stored energy as C_{oss} while V_{DS} is rising from 0 V to the stated value.*

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(v)}$	Voltage delay time	V_{DD} = 400 V, I_D = 80 A,	-	295	-	ns
$t_{r(v)}$	Voltage rise time	R_G = 4.7 Ω, V_{GS} = 10 V	-	56	-	ns
$t_{f(i)}$	Current fall time	(see Figure 15. Test circuit for inductive load switching and diode recovery times	-	37	-	ns
$t_{c(off)}$	Crossing time	and Figure 18. Switching time waveform)	-	84	-	ns

Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		130	A
I_{SDM}[1]	Source-drain current (pulsed)		-		520	A
V_{SD}[2]	Forward on voltage	I_{SD} = 130 A, V_{GS} = 0 V	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 130 A, di/dt = 100 A/µs, V_{DD} = 100 V (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	570		ns
Q_{rr}	Reverse recovery charge		-	15		µC
I_{RRM}	Reverse recovery current		-	53		A
t_{rr}	Reverse recovery time	I_{SD} = 130 A, di/dt = 100 A/µs, V_{DD} = 100 V, T_J = 150 °C (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	720		ns
Q_{rr}	Reverse recovery charge		-	24		µC
I_{RRM}	Reverse recovery current		-	68		A

1. *Pulse width is limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

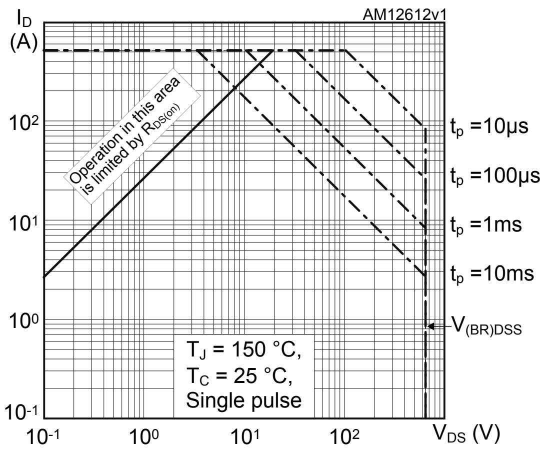


Figure 2. Normalized transient thermal impedance

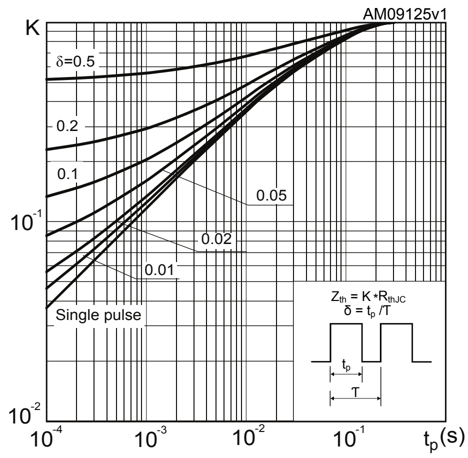


Figure 3. Typical output characteristics

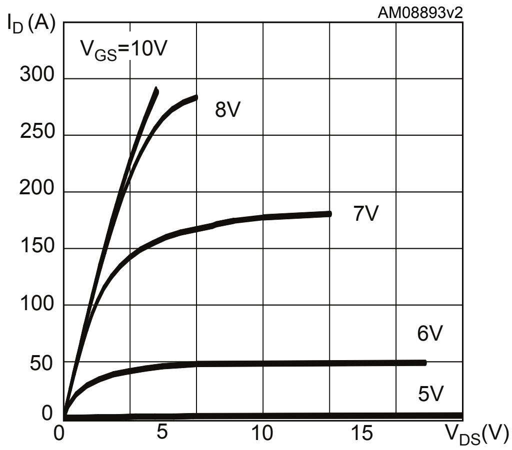


Figure 4. Typical transfer characteristics

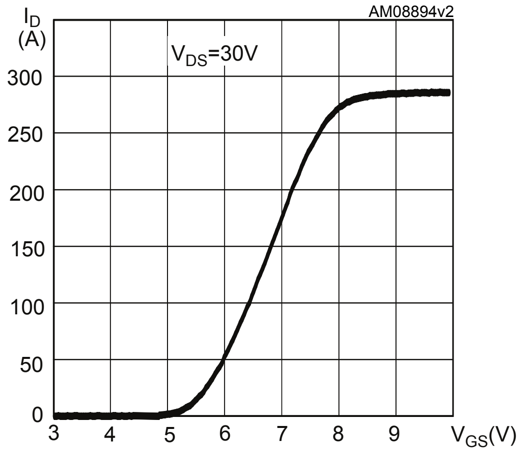


Figure 5. Normalized breakdown voltage vs temperature

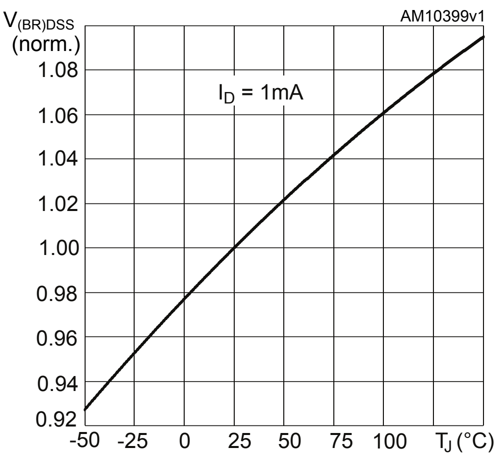


Figure 6. Typical drain-source on-resistance

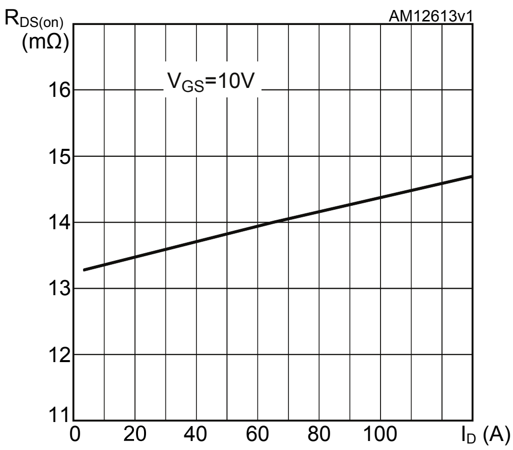


Figure 7. **Typical gate charge characteristics**

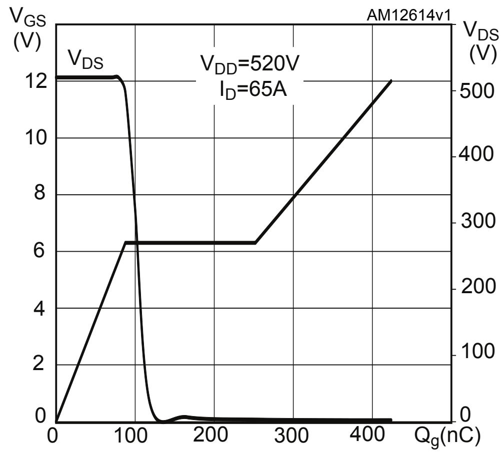


Figure 8. **Typical capacitance characteristics**

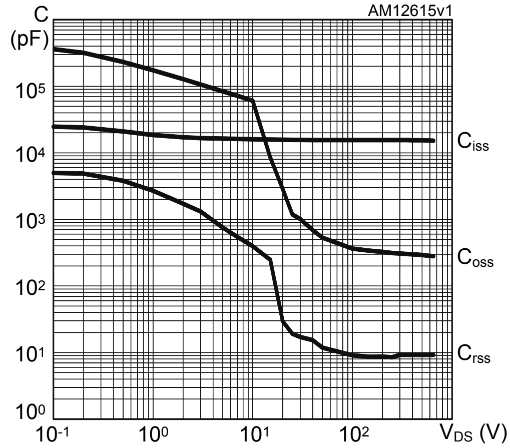


Figure 9. **Normalized gate threshold vs temperature**

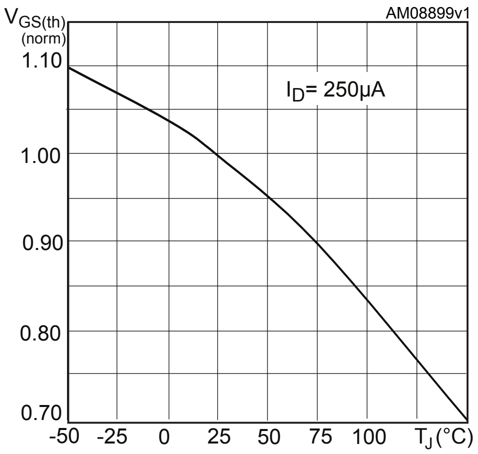


Figure 10. **Normalized on-resistance vs temperature**

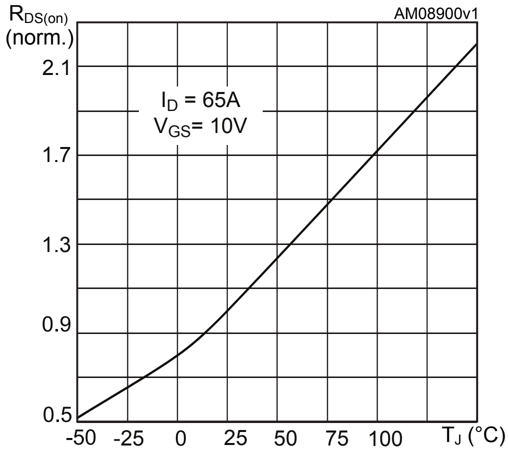


Figure 11. **Typical output capacitance stored energy**

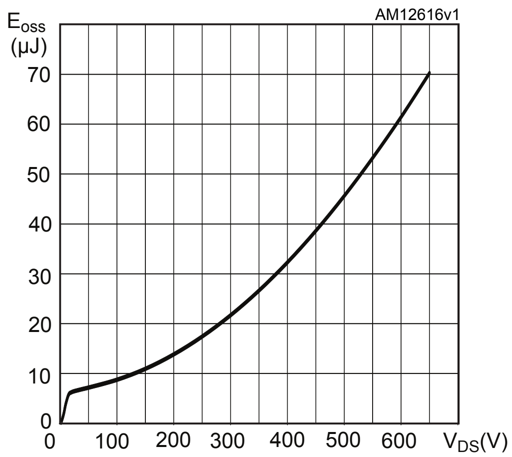
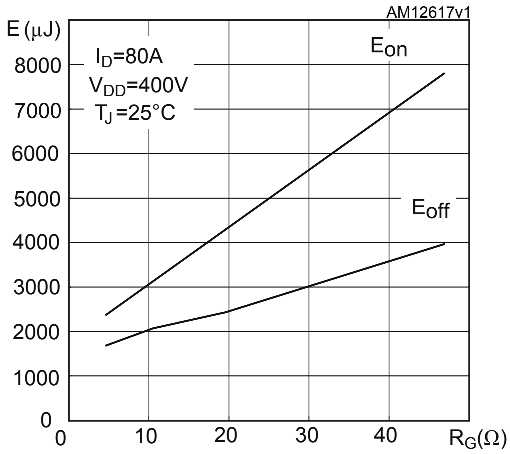


Figure 12. **Typical switching energy vs gate resistance**



Note: *E_{on} including reverse recovery of a SiC diode.*

3 Test circuits

Figure 13. Test circuit for resistive load switching times

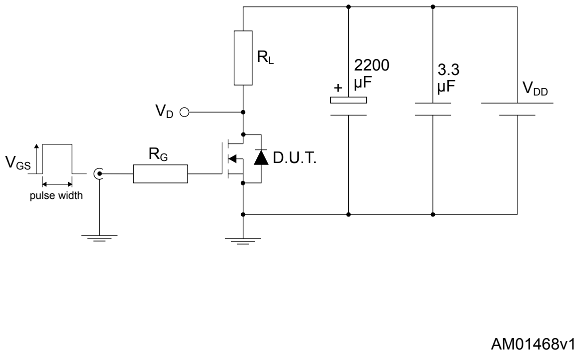


Figure 14. Test circuit for gate charge behavior

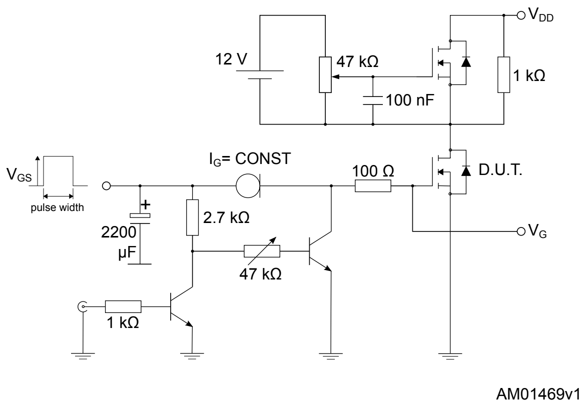


Figure 15. Test circuit for inductive load switching and diode recovery times

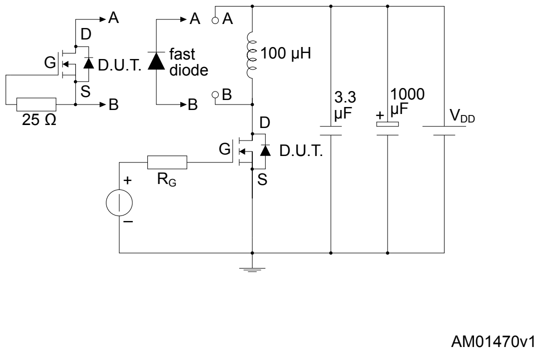


Figure 16. Unclamped inductive load test circuit

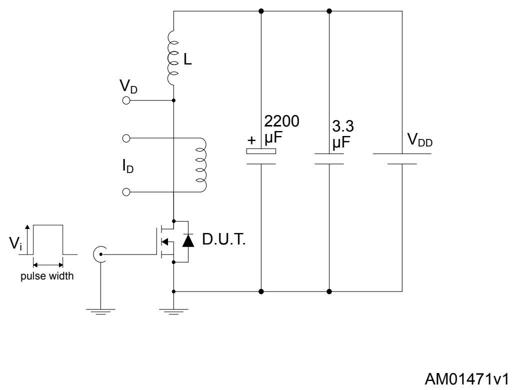


Figure 17. Unclamped inductive waveform

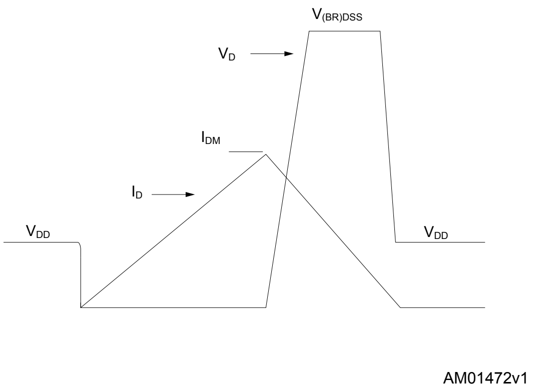
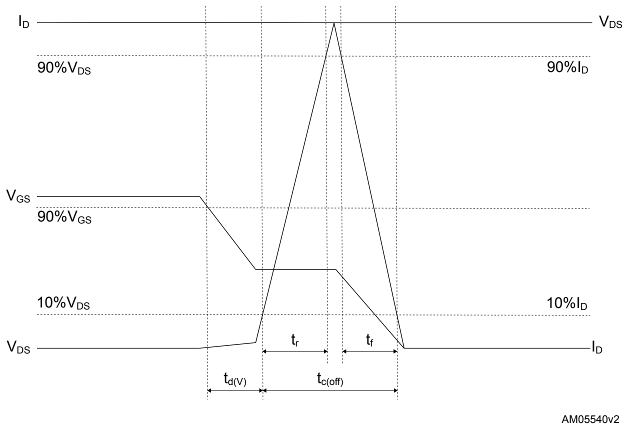


Figure 18. Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 Max247 package information

Figure 19. **Max247 package outline**

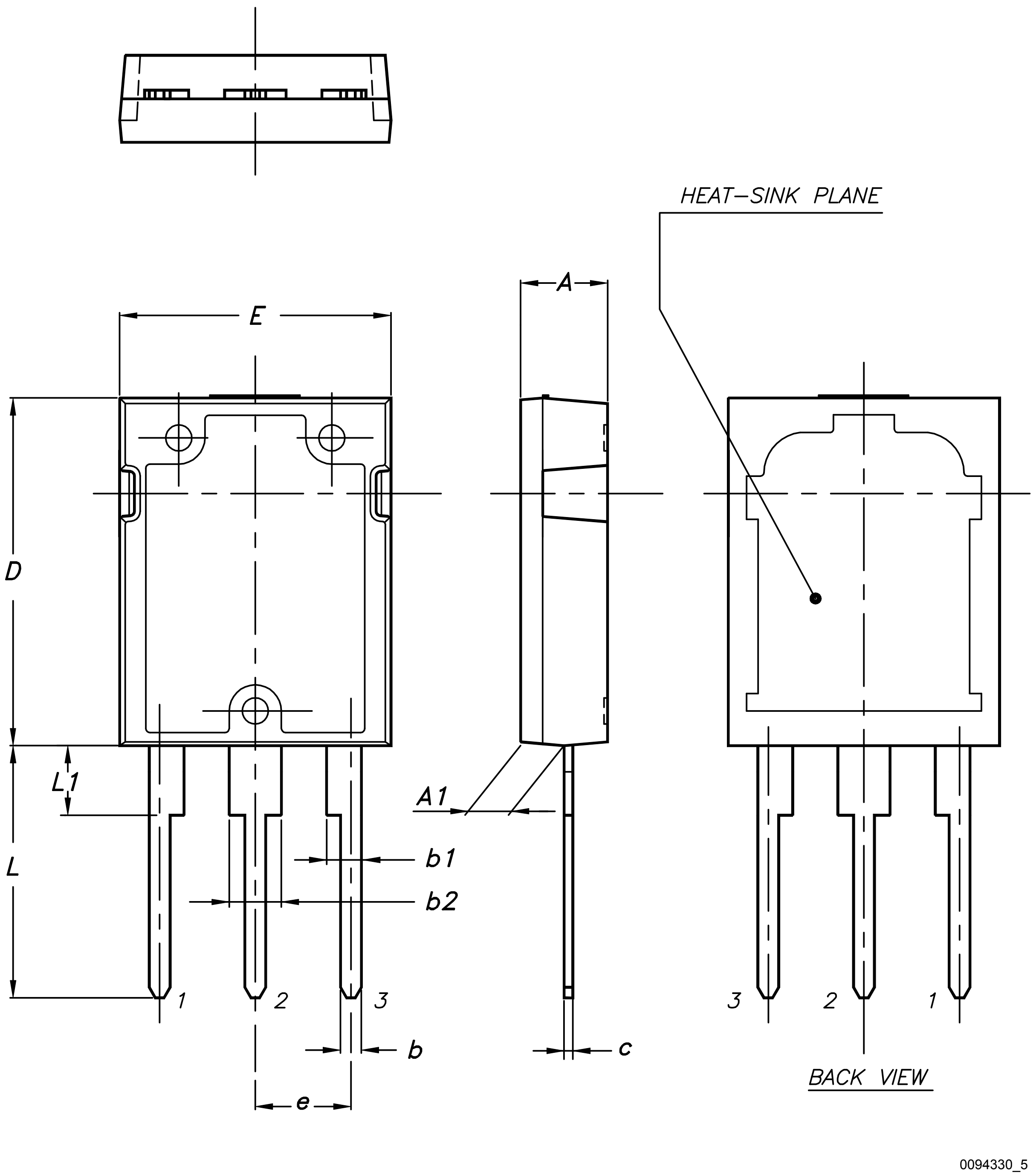


Table 7. Max247 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.70	-	5.30
A1	2.20	-	2.60
b	1.00	-	1.40
b1	2.00	-	2.40
b2	3.00	-	3.40
c	0.40	-	0.80
D	19.70	-	20.30
e	5.35	-	5.55
E	15.30	-	15.90
L	14.20	-	15.20
L1	3.70	-	4.30

Revision history

Table 8. Document revision history

Date	Revision	Changes
09-Mar-2012	1	First release.
04-Apr-2012	2	Inserted new *Section 2.1: Electrical characteristics (curves)*. Updated *Section 4: Package mechanical data*.
19-Apr-2012	3	Document promoted from preliminary data to production data. Updated *Section 4: Package mechanical data*.
24-Jan-2013	4	– Minor text changes – Modified: I_{AR} E_{AS} values on *Table 2*
18-Jul-2022	5	Updated title, Internal schematic, Features and Description on cover page. Updated I_{AR} value in Table 1. Absolute maximum ratings and updated Table 2. Thermal data. Minor text changes.

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