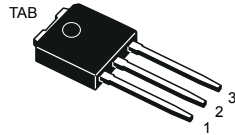
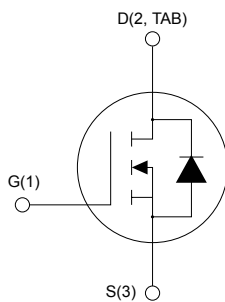


N-channel 600 V, 7.3 Ω typ., 1 A SuperMESH Power MOSFET in an IPAK package


IPAK


AM01475v1_noZen


Product status link
[STD1NK60-1](#)
Product summary

Order code	STD1NK60-1
Marking	D1NK60
Package	IPAK
Packing	Tube

Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STD1NK60-1	600 V	8.5 Ω	1 A

- Extremely high dv/dt capability
- ESD improved capability
- 100% avalanche tested
- Gate charge minimized

Applications

- Low power battery chargers
- Switch mode low power supplies (SMPS)
- Low power, ballast, CFL (compact fluorescent lamps)

Description

This high-voltage device is a Zener-protected N-channel Power MOSFET developed using the SuperMESH technology by STMicroelectronics, an optimization of the well-established PowerMESH. In addition to a significant reduction in on-resistance, this device is designed to ensure a high level of dv/dt capability for the most demanding applications.

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	600	V
V_{GS}	Gate-source voltage	± 30	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	1	A
	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	0.63	
$I_{DM}^{(1)}$	Drain current (pulsed)	4	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	30	W
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J max.)	1	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	25	mJ
$dv/dt^{(2)}$	Peak diode recovery voltage slope	3	V/ns
T_{stg}	Storage temperature range	-55 to 150	$^\circ\text{C}$
T_J	Operating junction temperature range		$^\circ\text{C}$

1. Pulse width limited by safe operating area.

2. $I_{SD} \leq 1\text{ A}$, $di/dt \leq 100\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq T_J$ max.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	4.2	$^\circ\text{C}/\text{W}$
R_{thJA}	Thermal resistance, junction-to-ambient	100	$^\circ\text{C}/\text{W}$

2 Electrical characteristics

$T_C = 25\text{ °C}$ unless otherwise specified.

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	600			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$, $T_C = 125\text{ °C}$ ⁽¹⁾			50	
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 30\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2.25	3	3.7	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$, $I_D = 0.5\text{ A}$		7.3	8.5	Ω

1. Specified by design, not tested in production.

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	156	-	pF
C_{oss}	Output capacitance		-	23.5	-	pF
C_{rss}	Reverse transfer capacitance		-	3.8	-	pF
Q_g	Total gate charge	$V_{DD} = 480\text{ V}$, $I_D = 1\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 14. Test circuit for gate charge behavior)	-	7	-	nC
Q_{gs}	Gate-source charge		-	1.1	-	nC
Q_{gd}	Gate-drain charge		-	3.7	-	nC

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$, $I_D = 0.5\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	6.5	-	ns
t_r	Rise time		-	5	-	ns
$t_{d(off)}$	Turn-off delay time	(see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	19	-	ns
t_f	Fall time		-	25	-	ns

Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		1	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		4	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 1.0 \text{ A}$, $V_{GS} = 0 \text{ V}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 1 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$,	-	140		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 25 \text{ V}$	-	240		nC
I_{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	3.3		A
t_{rr}	Reverse recovery time	$I_{SD} = 1 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$	-	229		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 25 \text{ V}$, $T_J = 150 \text{ }^\circ\text{C}$	-	377		nC
I_{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	3.3		A

1. Pulse width is limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics curves

Figure 1. Safe operating area

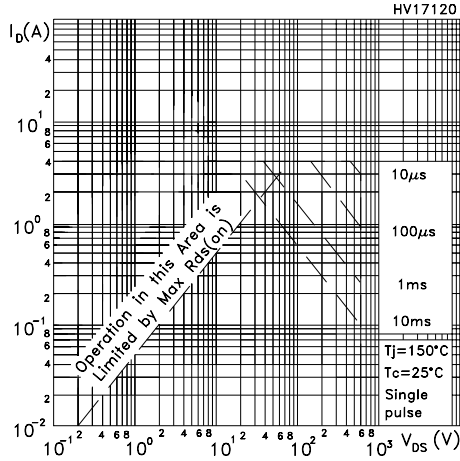


Figure 2. Thermal impedance

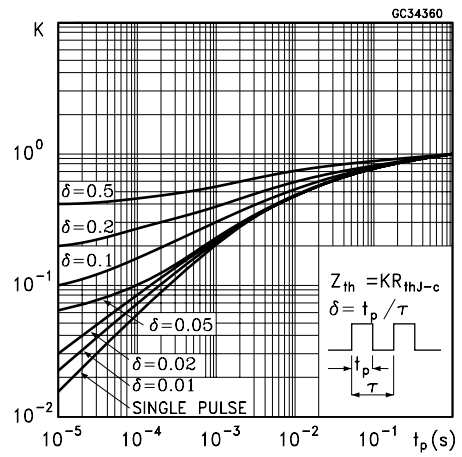


Figure 3. Output characteristics

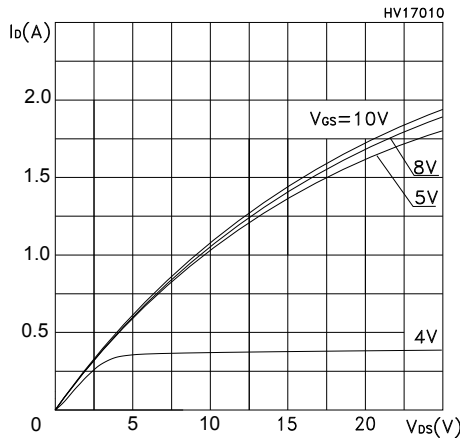


Figure 4. Transfer characteristics

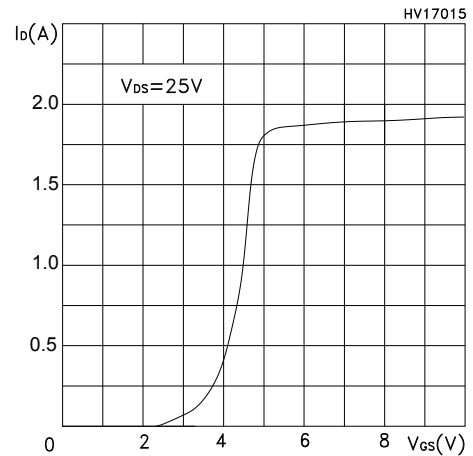


Figure 5. Gate charge vs gate-source voltage

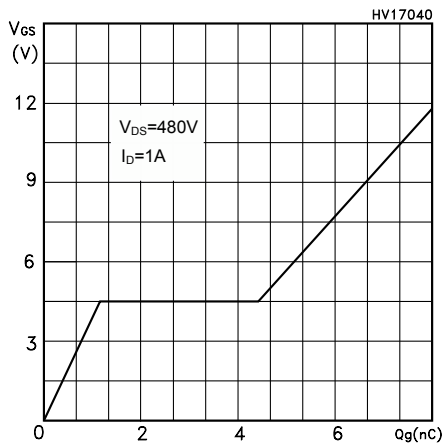


Figure 6. Capacitance variations

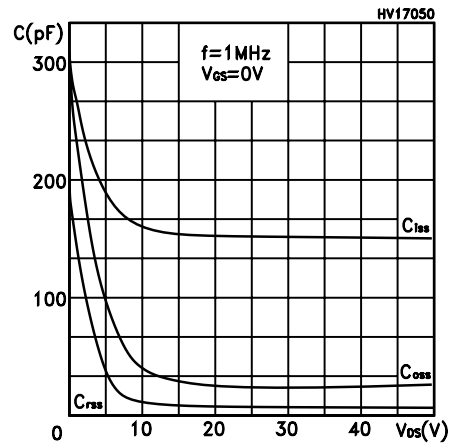


Figure 7. Static drain-source on-resistance

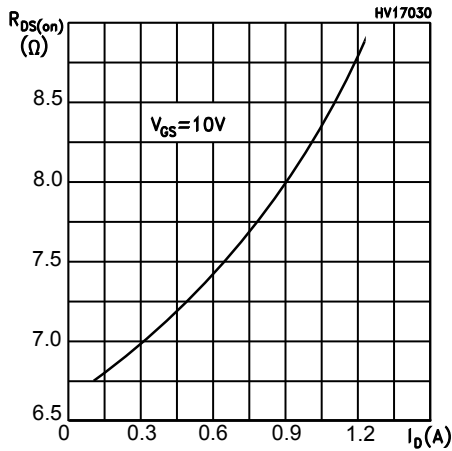


Figure 8. Normalized gate threshold voltage vs temperature

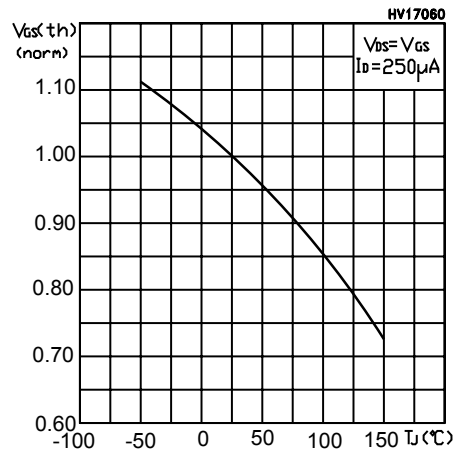


Figure 9. Normalized on-resistance vs temperature

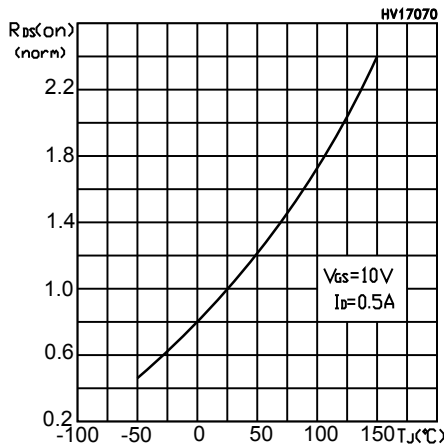


Figure 10. Source-drain forward characteristics

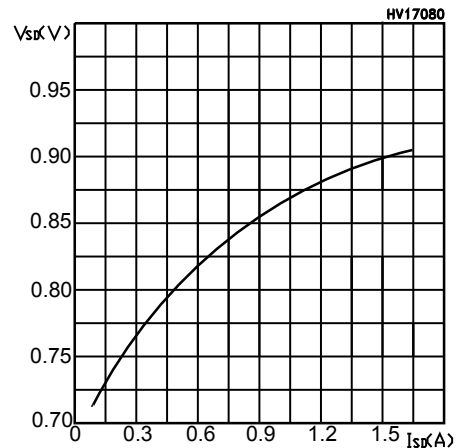


Figure 11. Normalized $V_{(BR)DSS}$ vs temperature

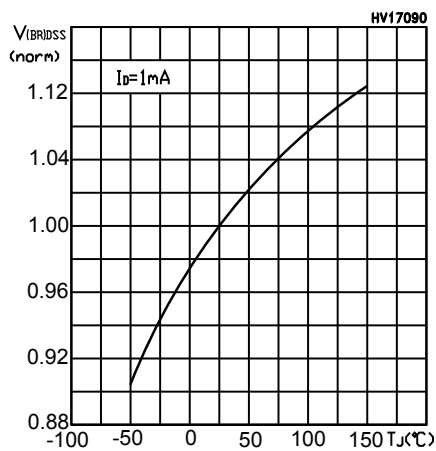
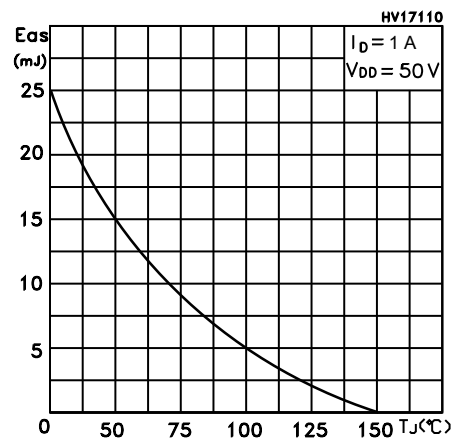


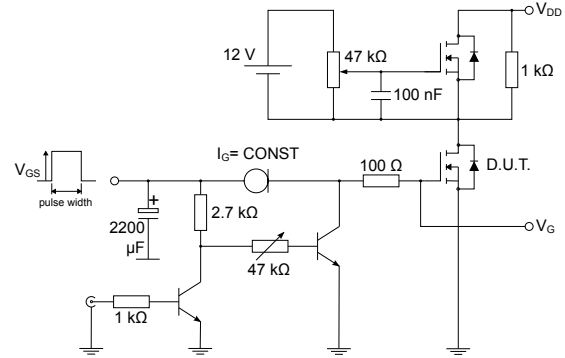
Figure 12. Maximum avalanche energy vs temperature



3 Test circuits

Figure 13. Test circuit for resistive load switching times


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Figure 14. Test circuit for gate charge behavior


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Figure 15. Test circuit for inductive load switching and diode recovery times

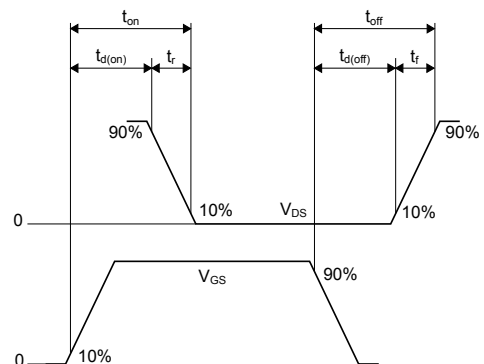

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Figure 16. Unclamped inductive load test circuit


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Figure 17. Unclamped inductive waveform


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Figure 18. Switching time waveform


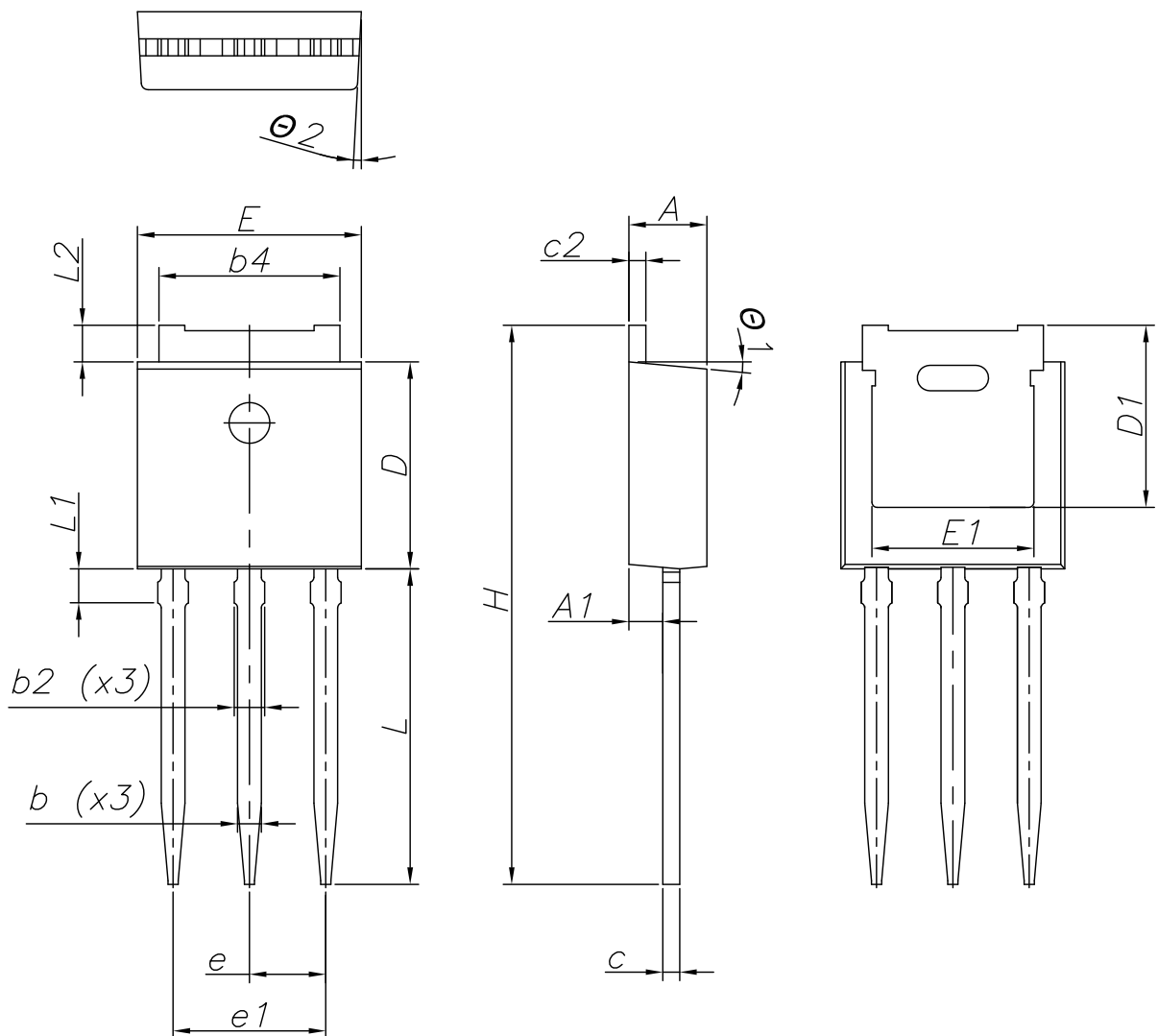
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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 IPAK (TO-251) type C package information

Figure 19. IPAK (TO-251) type C package outline



0068771_IK_typeC_rev16

Table 7. IPAK (TO-251) type C package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.35
A1	0.90	1.00	1.10
b	0.66		0.79
b2			0.90
b4	5.23	5.33	5.43
c	0.46		0.59
c2	0.46		0.59
D	6.00	6.10	6.20
D1	5.20	5.37	5.55
E	6.50	6.60	6.70
E1	4.60	4.78	4.95
e	2.20	2.25	2.30
e1	4.40	4.50	4.60
H	16.18	16.48	16.78
L	9.00	9.30	9.60
L1	0.80	1.00	1.20
L2	0.90	1.08	1.25
θ1	3°	5°	7°
θ2	1°	3°	5°

Revision history

Table 8. Document revision history

Date	Revision	Changes
09-Feb-2017	1	First release.
17-Oct-2023	2	Updated Section 4.1 IPAK (TO-251) type C package information. Minor text changes.

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