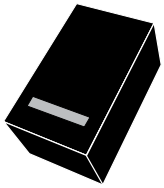
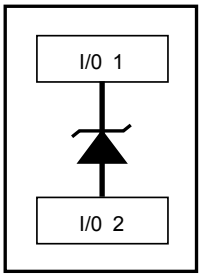
ESDAXLC6-1MY2

Datasheet

Extra low capacitance single line transient voltage surge suppressor (TVS)



SOD882 (µQFN-2L)



GND

Product status link
ESDAXLC6-1MY2

Features

- Extra low capacitance 0.6 pF max on a wide frequency spectrum (200 MHz - 3000 MHz)
- Unidirectional device
- Low clamping factor V_{CL} / V_{BR}
- Fast response time
- Very thin package: 0.55 mm max
- Low leakage current
- High ESD protection level
- High integration
- Suitable for high density boards
- Complies with the following standards
  - IEC 61000-4-2 level 4
  - MIL STD 883G-Method 3015-7: class 3B

Applications

Where transient overvoltage protection in ESD sensitive equipment is required, such as:

- Computers
- Printers
- Communication systems
- Cellular phone handsets and accessories
- Video equipment Portable equipment

Description

The ESDAXLC6-1MY2 is a single line Transil diode designed specifically for the protection of integrated circuits in portable equipment and miniaturized electronics devices subject to ESD transient over voltages.

Packaged in SOD882 (µQFN-2L), it minimizes PCB consumption.

1 Characteristics

Table 1. Absolute maximum ratings (T_{amb} = 25 °C)

Symbol	Parameter		Value	Unit
V_{PP}	Peak pulse voltage	IEC 61000-4-2, level 4 : contact discharge	8	kV
P_{PP}	Peak pulse power	8/20µs(1), T_j initial = T_{amb}	12	W
I_{PP}	Peak pulse current typical value (8/20 µs)		2.8	A
T_{stg}	Storage temperature range		-55 to +150	°C
T_{op}	Operating temperature range		-40 to +125	

1. *For a surge greater than the maximum values, the diode will fail in short-circuit.*

Figure 1. Electrical characteristics (definitions)

Symbol — Parameter
V_{BR} = Breakdown voltage
I_{RM} = Leakage current at V_{RM}
V_{RM} = Stand-off voltage
I_R = Breakdown current

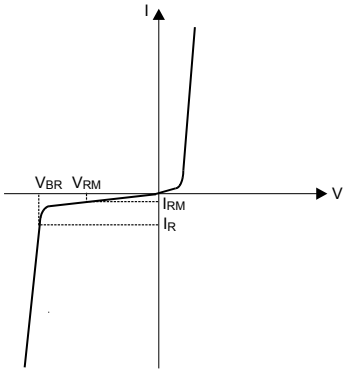


Table 2. Electrical characteristics (values) (T_{amb} = 25° C)

Symbol	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	I_R = 1 mA	6	-		V
I_{RM}	V_{RM} = 3 V		-	100	nA
C_{LINE}	V_R = 0 V, F = (200 MHz - 3000 MHz), V_{OSC} = 30 mV		-	0.6	pF

1.1 Characteristics (curves)

Figure 2. Junction capacitance versus reverse voltage applied (typical values)

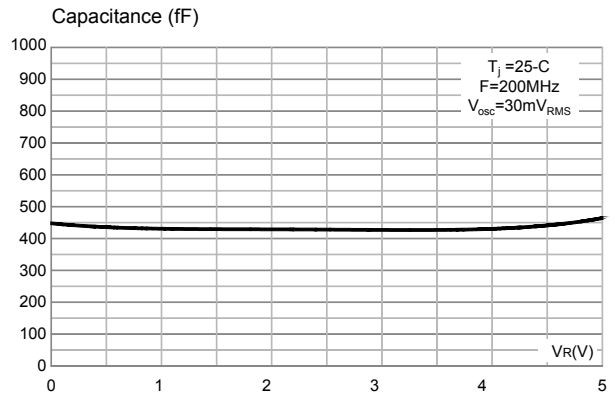


Figure 3. Junction capacitance versus frequency (typical values)

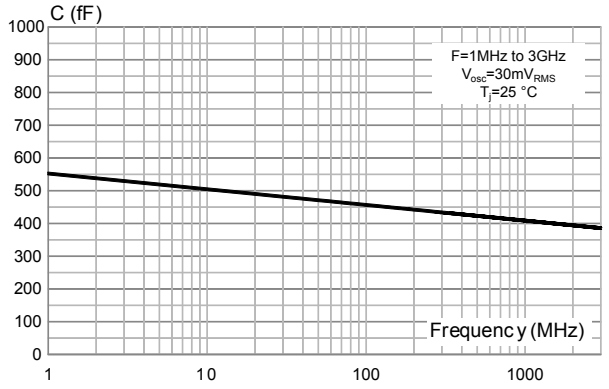


Figure 4. S21 (dB) attenuation

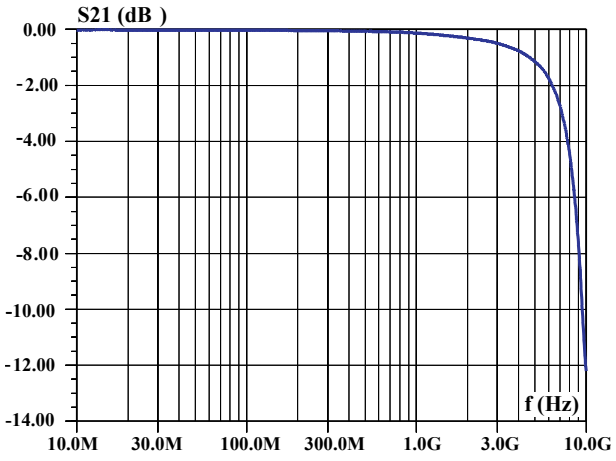


Figure 5. Leakage current versus junction temperature (typical values)

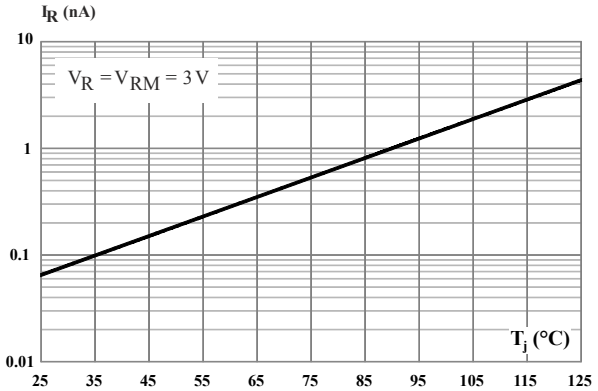


Figure 6. ESD response to IEC 61000-4-2 (+ 8 kV contact discharge

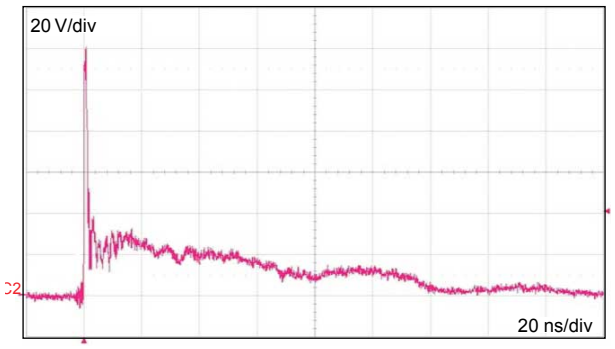
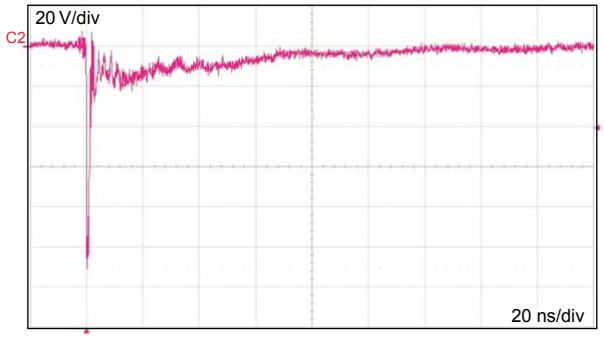


Figure 7. ESD response to IEC 61000-4-2 (-8 kV contact discharge)



2 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

2.1 SOD882 package information

- Epoxy meets UL 94, V0
- Lead-free package

Figure 8. SOD882 package outline

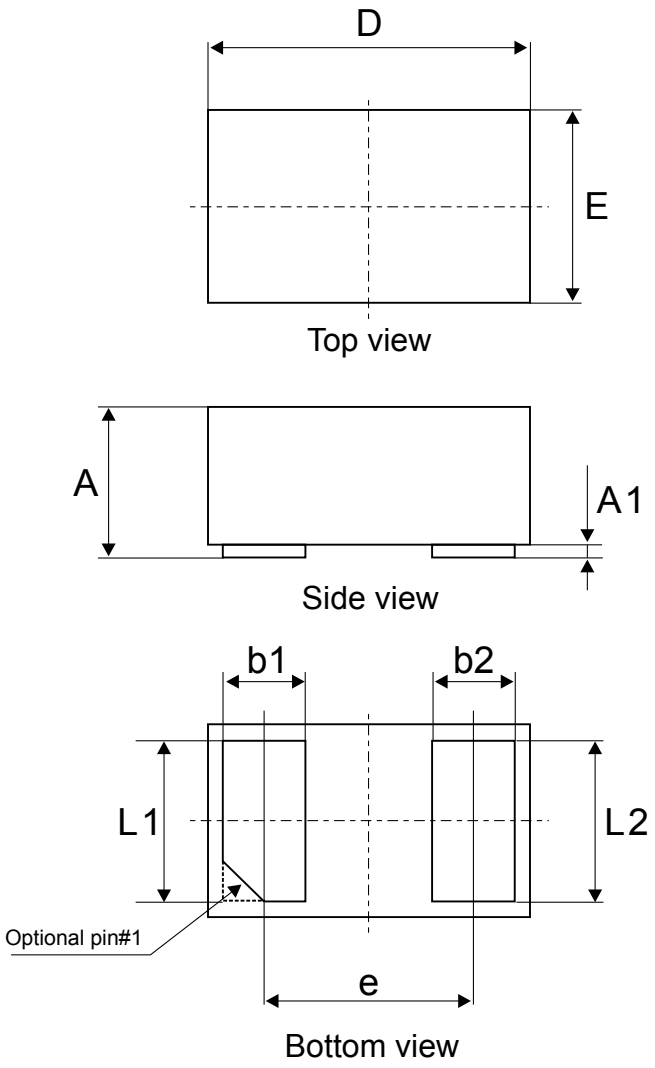


Table 3. **SOD882 package mechanical data**

Ref.	Dimensions					
	Millimeters			inches (dimension in inches are given for reference only)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.45	0.50	0.55	0.018	0.020	0.022
A1	0.00		0.05	0.000	0.000	0.002
b1	0.20	0.25	0.30	0.008	0.010	0.012
b2	0.20	0.25	0.30	0.008	0.010	0.012
D	0.95	1.00	1.05	0.037	0.039	0.041
E	0.55	0.60	0.65	0.022	0.024	0.026
e		0.65			0.026	
L1	0.45	0.50	0.55	0.018	0.020	0.022
L2	0.45	0.50	0.55	0.018	0.020	0.022

Figure 9. **SOD882 recommended footprint**

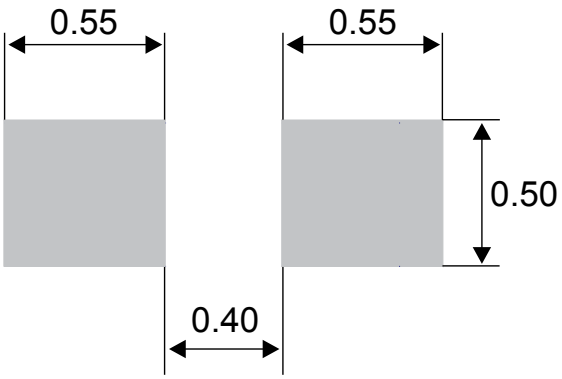


Figure 10. **Marking**

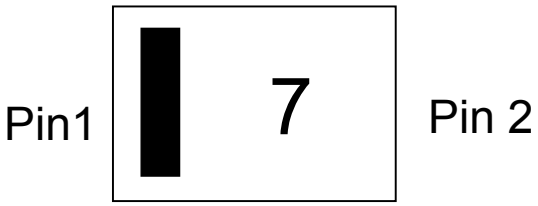
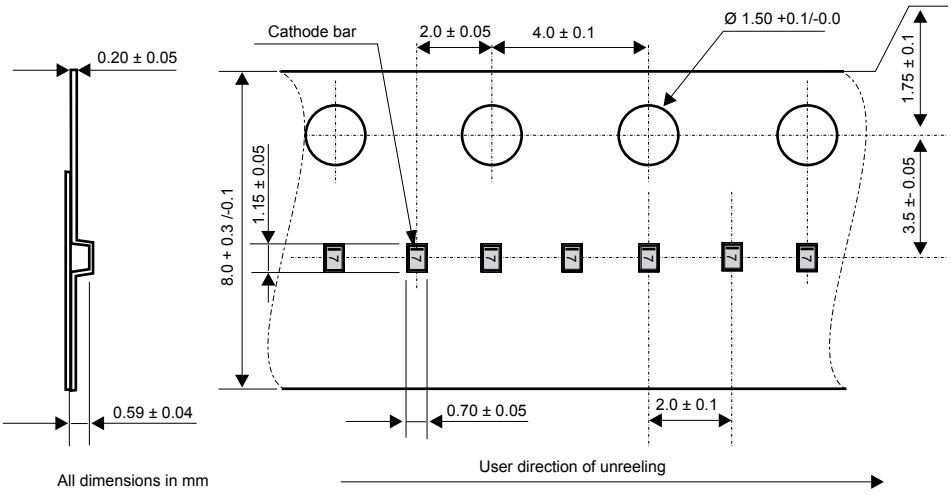


Figure 11. Tape and reel specification

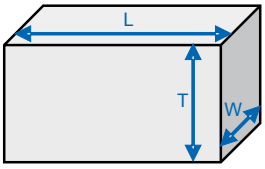


3 Recommendation on PCB assembly

3.1 Stencil opening design

1. General recommendation on stencil opening design
   a. Stencil opening dimensions: L (Length), W (Width), T (Thickness).

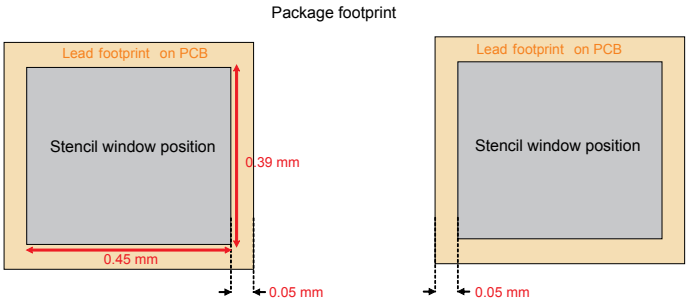
Figure 12. Stencil opening recommendation



   b. General design rule
      - Stencil thickness (T) = 75 ~ 125 µm
      - $\frac{W}{T} \geq 1.5$
      - $\frac{L \times W}{2T(L+W)} \geq 0.66$

1. Reference design
   a. Stencil opening thickness: 100 µm
   b. Stencil opening for leads: Opening to footprint ratio is 90%

Figure 13. Recommended stencil window position in mm



3.2 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed.
4. Use solder paste with fine particles: powder particle size 20-45 µm.

3.3 Placement

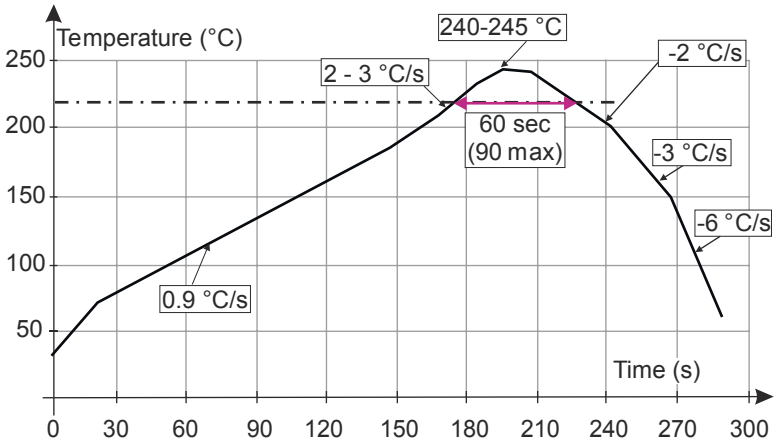
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering
3. Standard tolerance of ±0.05 mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

3.4 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. A symmetrical layout is recommended, to avoid any tilt phenomena caused by asymmetrical solder paste due to solder flow away.

3.5 Reflow profile

Figure 14. ST ECOPACK® recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement.

4 Ordering information

Figure 15. **Ordering information scheme**

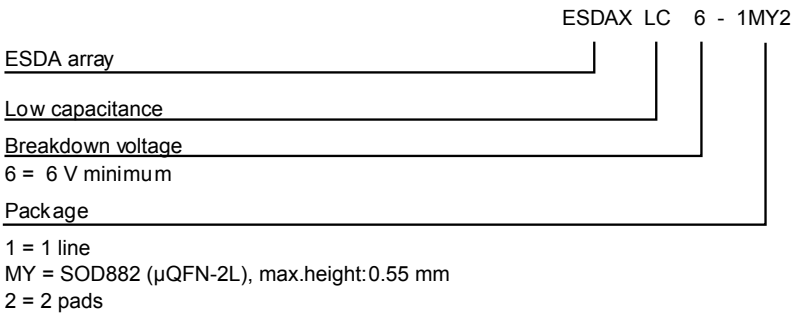


Table 4. **Ordering information**

Order code	Marking	Package	Weight	Base qty.	Delivery mode
ESDAXLC6-1MY2	7	SOD882 (µQFN-2L)	0.942 mg	12000	Tape and reel

Revision history

Table 5. **Document revision history**

Date	Revision	Changes
18-Jan-2010	1	Initial release.
23-Sep-2011	2	Updated package name.
31-Mar-2014	3	Updated operating junction temperature range in Table 2. Updated Figure 3, Figure 4, and Figure 6. Updated graphic and dimension names in Table 3, Updated Figure 15.
19-Sep-2019	4	Updated Section 2.1 SOD882 package information.

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