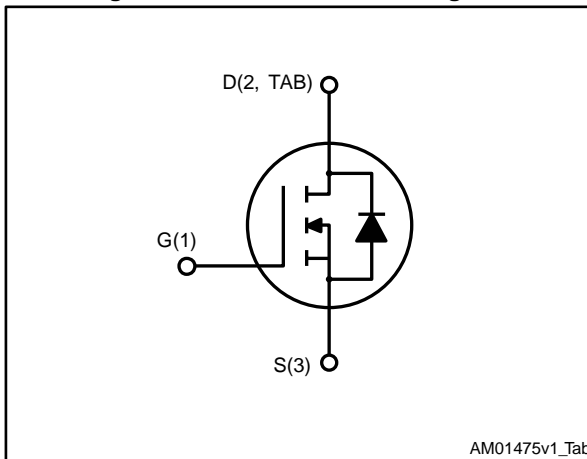


N-channel 30 V, 4 mΩ typ., 80 A Power MOSFET in a DPAK package

Datasheet - production data



Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D	P _{TOT}
STD80N3LL	30 V	5.2 mΩ	80 A	75 W

- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET with very low R_{DS(on)} in all packages.

Table 1: Device summary

Order code	Marking	Package	Packaging
STD80N3LL	80N3LL	DPAK	Tape and reel

Contents

- 1 Electrical ratings 3**
- 2 Electrical characteristics 4**
 - 2.1 Electrical characteristics (curves)..... 5
- 3 Test circuits 7**
- 4 Package information 8**
 - 4.1 DPAK package information 9
 - 4.2 DPAK (TO-252) packing information..... 12
- 5 Revision history 14**



1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	30	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	80	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	60	A
$I_{DM}^{(1)(2)}$	Drain current (pulsed)	320	A
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	75	W
T_j	Operating junction temperature range	-55 to 175	$^\circ\text{C}$
T_{stg}	Storage temperature range		

Notes:

⁽¹⁾This value is limited by package

⁽²⁾Pulse width limited by safe operating area

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max.	50	$^\circ\text{C}/\text{W}$
$R_{thj-case}$	Thermal resistance junction-case max.	2	$^\circ\text{C}/\text{W}$

Notes:

⁽¹⁾When mounted on FR-4 board of 1 inch², 2oz Cu

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4: On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 1 mA, V _{GS} = 0 V	30			V
I _{DSS}	Zero gate voltage drain current	V _{GS} = 0 V V _{DS} = 30 V			1	μA
I _{GSS}	Gate-body leakage current	V _{GS} = 20 V, V _{DS} = 0 V			100	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	1		2.5	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 40 A		4	5.2	mΩ
		V _{GS} = 4.5 V, I _D = 40 A		5.5	6.5	mΩ

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{ISS}	Input capacitance	V _{DS} = 25 V, f = 1 MHz, V _{GS} = 0 V	-	1640	-	pF
C _{OSS}	Output capacitance		-	207	-	
C _{RSS}	Reverse transfer capacitance		-	160	-	
Q _g	Total gate charge	V _{DD} = 15 V, I _D = 80 A, V _{GS} = 4.5 V (see Figure 14: "Test circuit for gate charge behavior")	-	18	-	nC
Q _{gs}	Gate-source charge	-	5.3	-		
Q _{gd}	Gate-drain charge	-	8.8	-		

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 15 V, I _D = 40 A, R _G = 4.7 Ω, V _{GS} = 10 V (see Figure 13: "Test circuit for resistive load switching times")	-	6.4	-	ns
t _r	Rise time		-	8	-	ns
t _{d(off)}	Turn-off delay time		-	36	-	ns
t _f	Fall time		-	12	-	ns

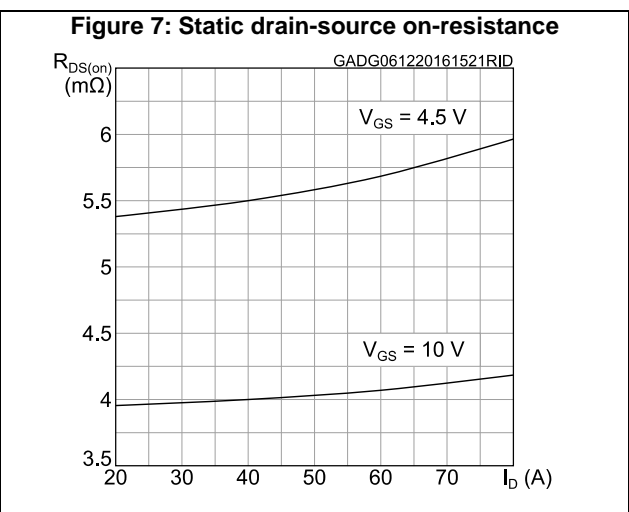
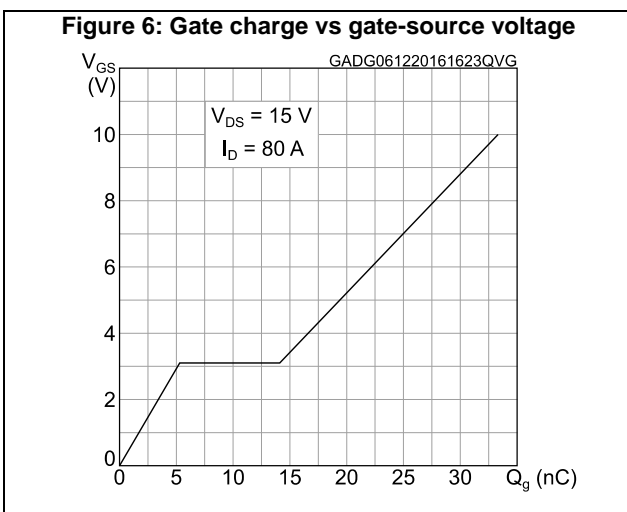
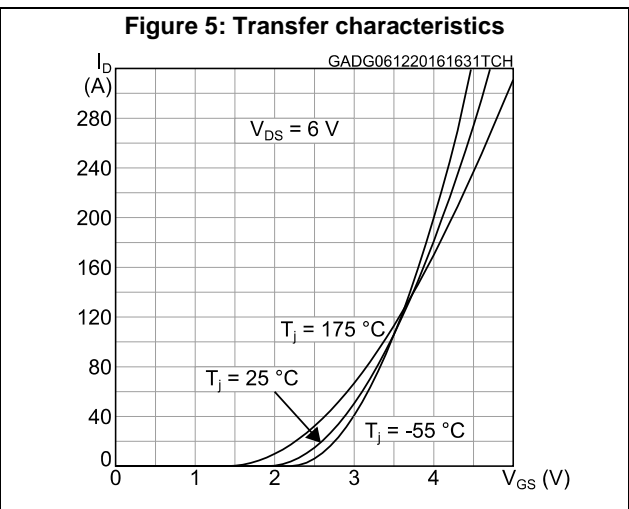
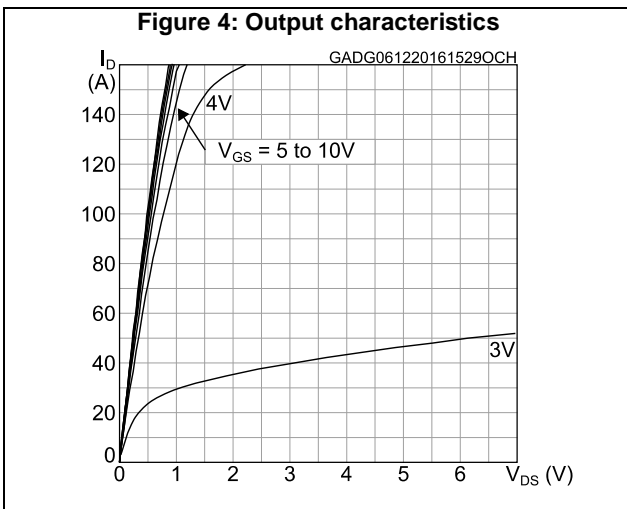
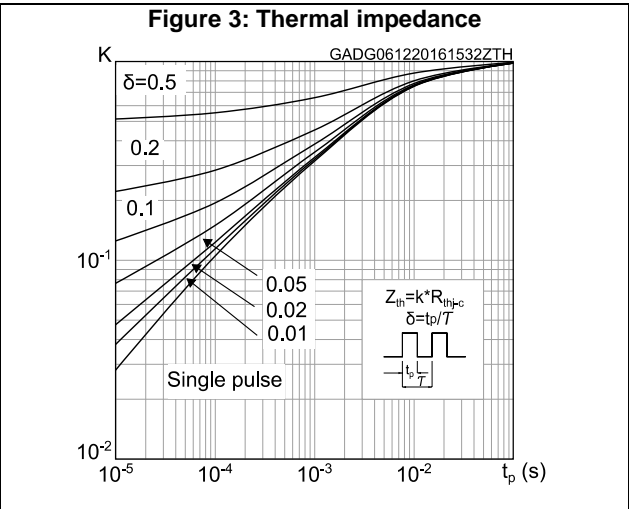
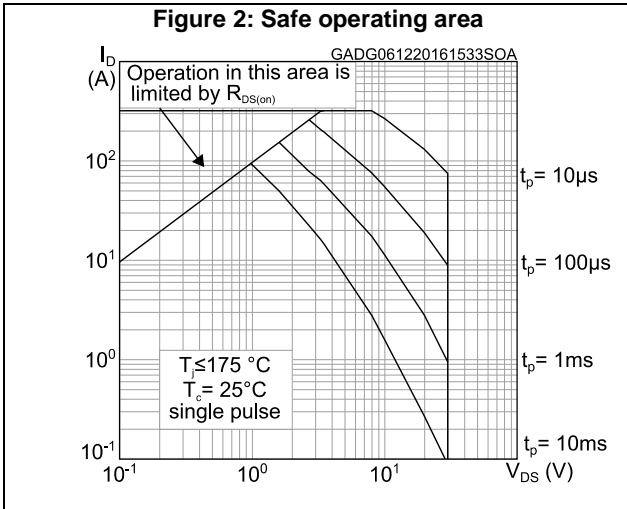
Table 7: Source-drain diode

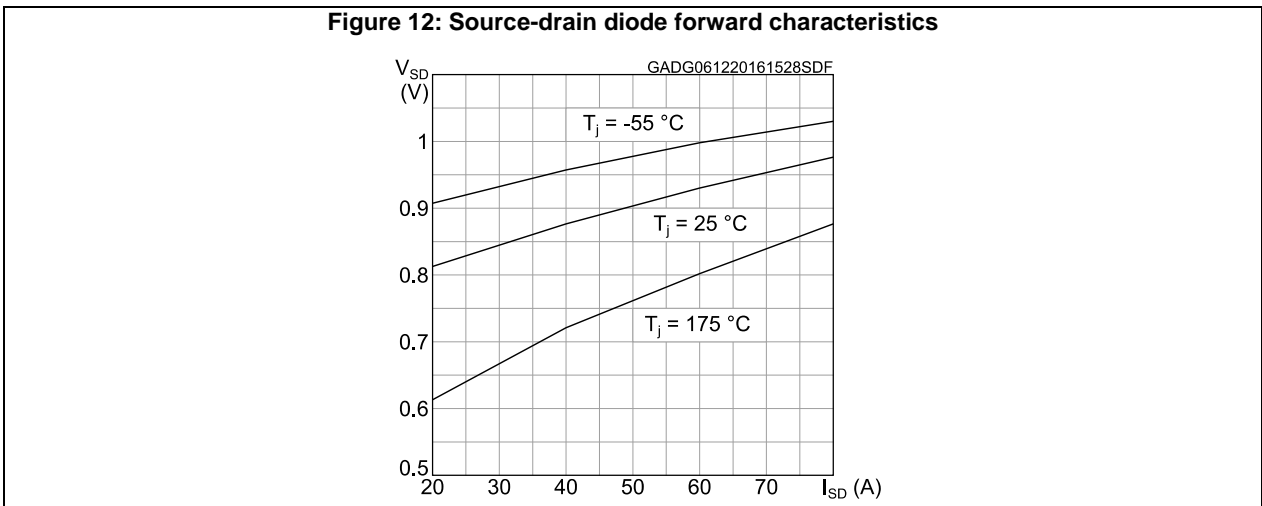
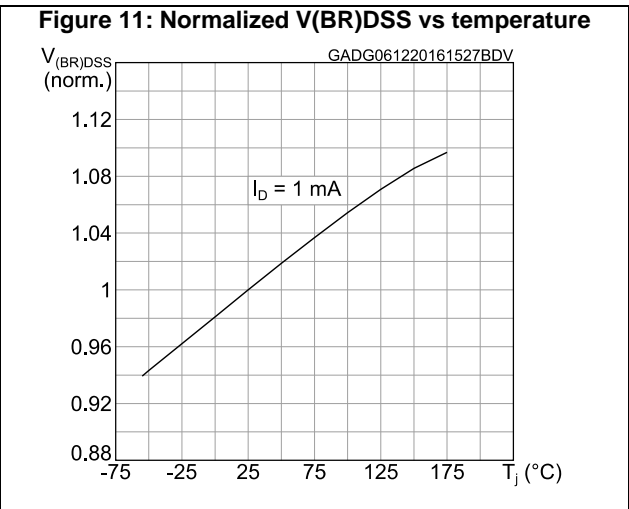
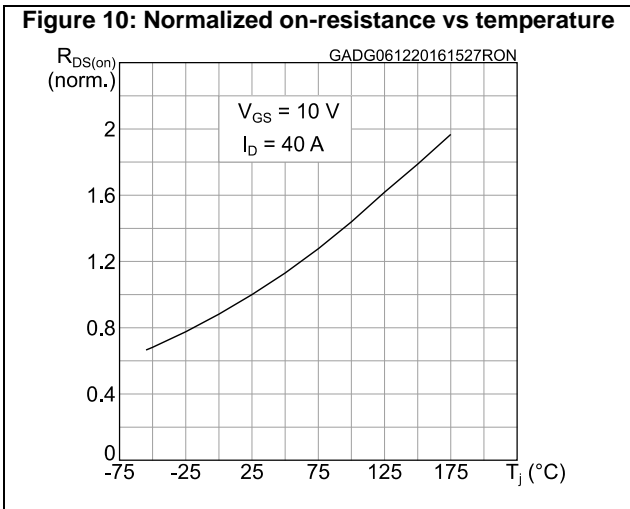
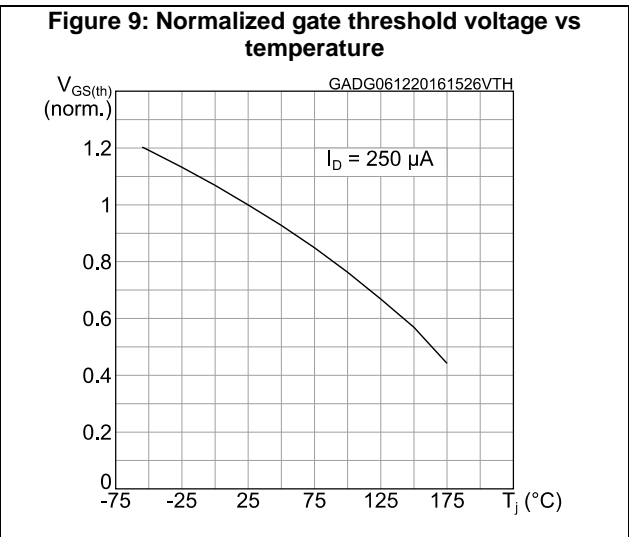
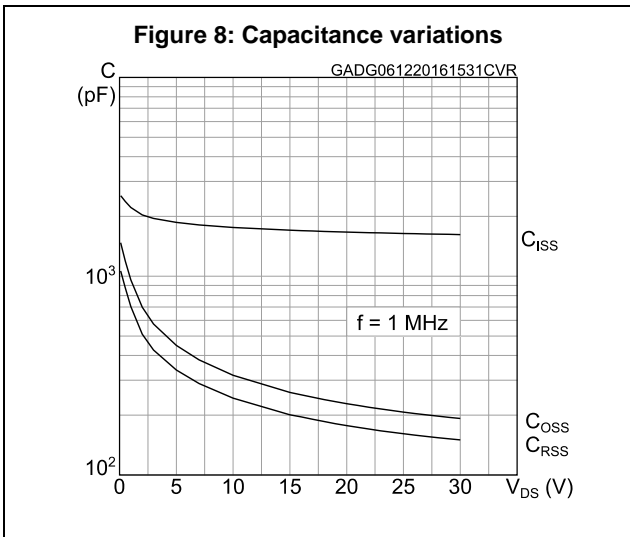
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{SD} ⁽¹⁾	Forward on voltage	I _{SD} = 80 A, V _{GS} = 0 V	-		1.2	V
t _{rr}	Reverse recovery time	I _D = 80 A, di/dt = 100 A/μs	-	21		ns
Q _{rr}	Reverse recovery charge	V _{DD} = 24 V (see Figure 15: "Test circuit for inductive load switching and diode recovery times")	-	14		nC
I _R RM	Reverse recovery current		-	1.3		A

Notes:

⁽¹⁾Pulsed: pulse duration = 300 μs, duty cycle 1.5%

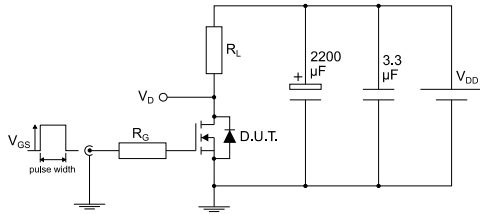
2.1 Electrical characteristics (curves)





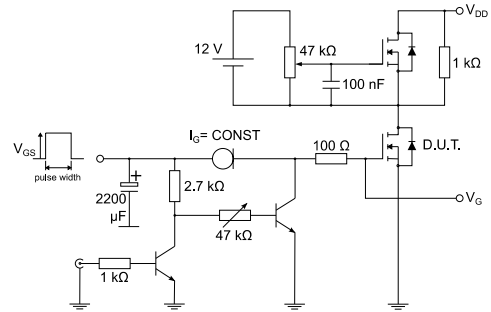
3 Test circuits

Figure 13: Test circuit for resistive load switching times



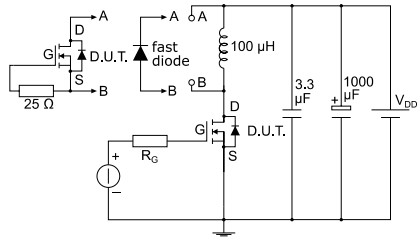
AM01468v1

Figure 14: Test circuit for gate charge behavior



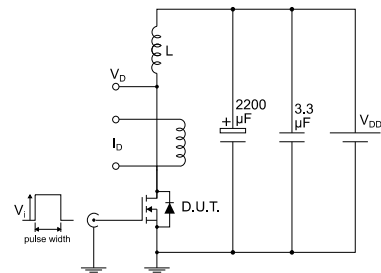
AM01469v1

Figure 15: Test circuit for inductive load switching and diode recovery times



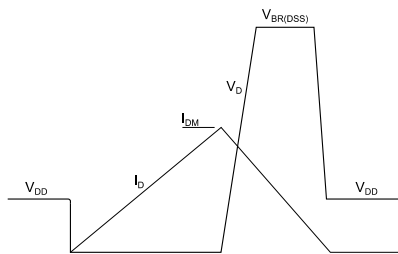
AM01470v1

Figure 16: Unclamped inductive load test circuit



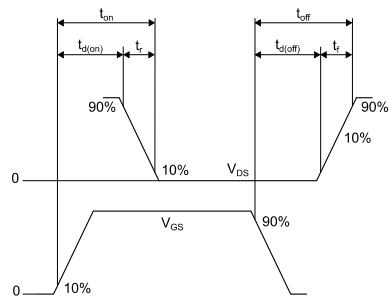
AM01471v1

Figure 17: Unclamped inductive waveform



AM01472v1

Figure 18: Switching time waveform



AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 DPAK package information

Figure 19: DPAK (TO-252) type A2 package outline

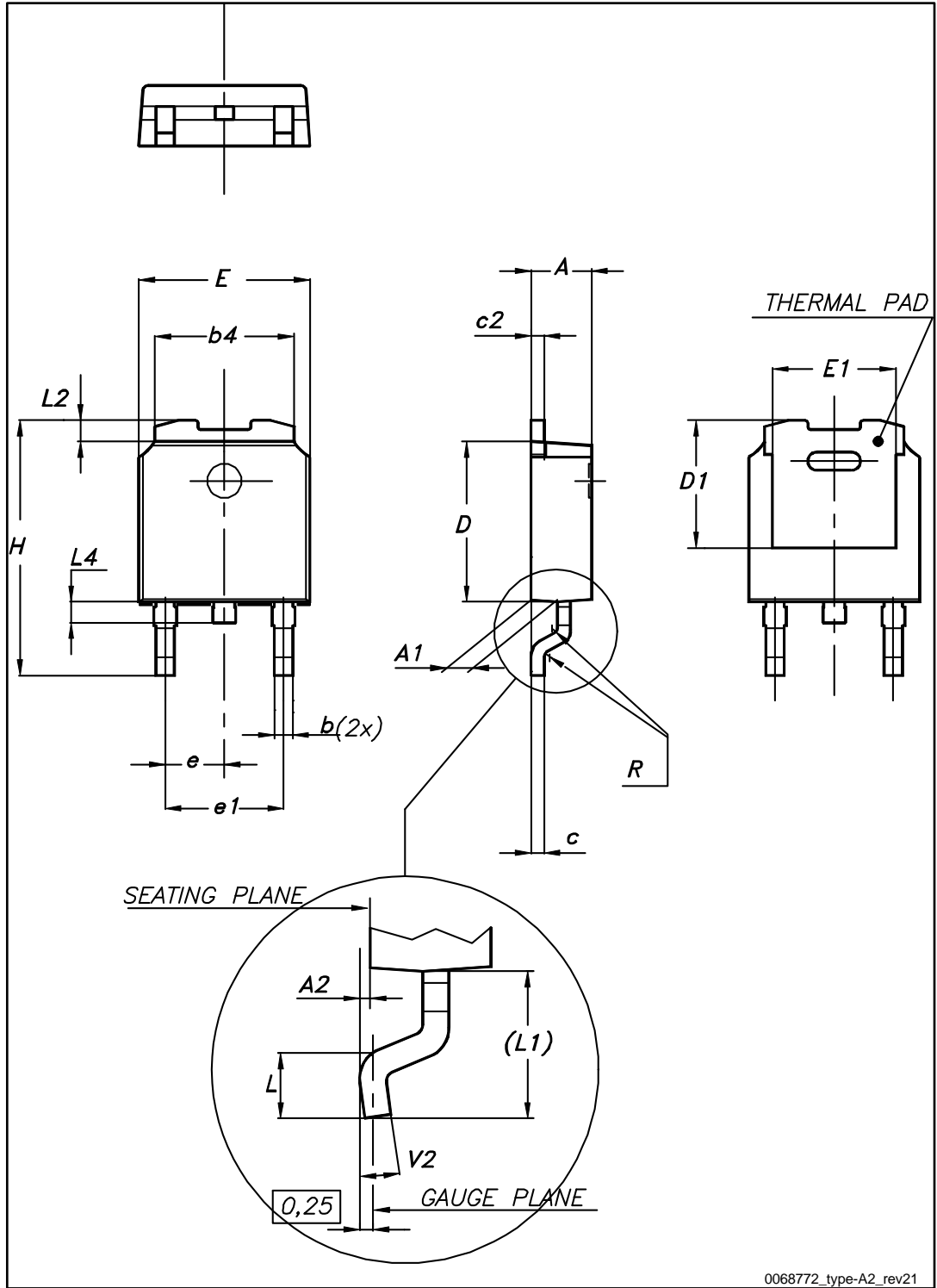
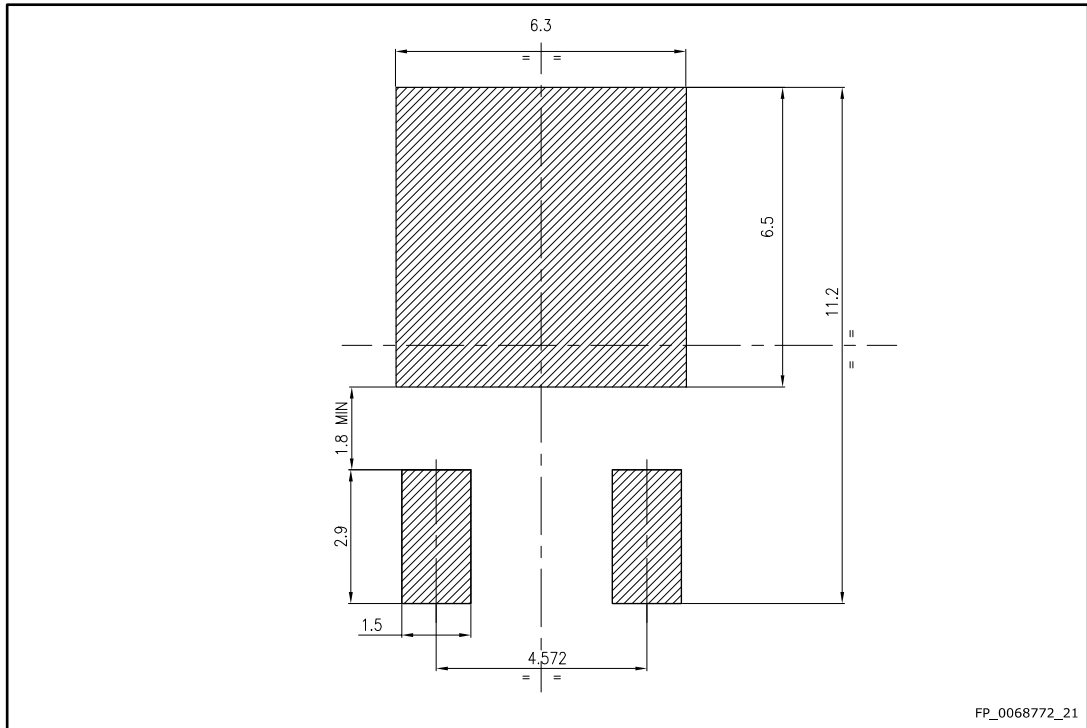


Table 8: DPAK (TO-252) type A2 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	5.10	5.20	5.30
e	2.16	2.28	2.40
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
L1	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 20: DPAK (TO-252) type A2 recommended footprint (dimensions are in mm)



4.2 DPAK (TO-252) packing information

Figure 21: DPAK (TO-252) tape outline

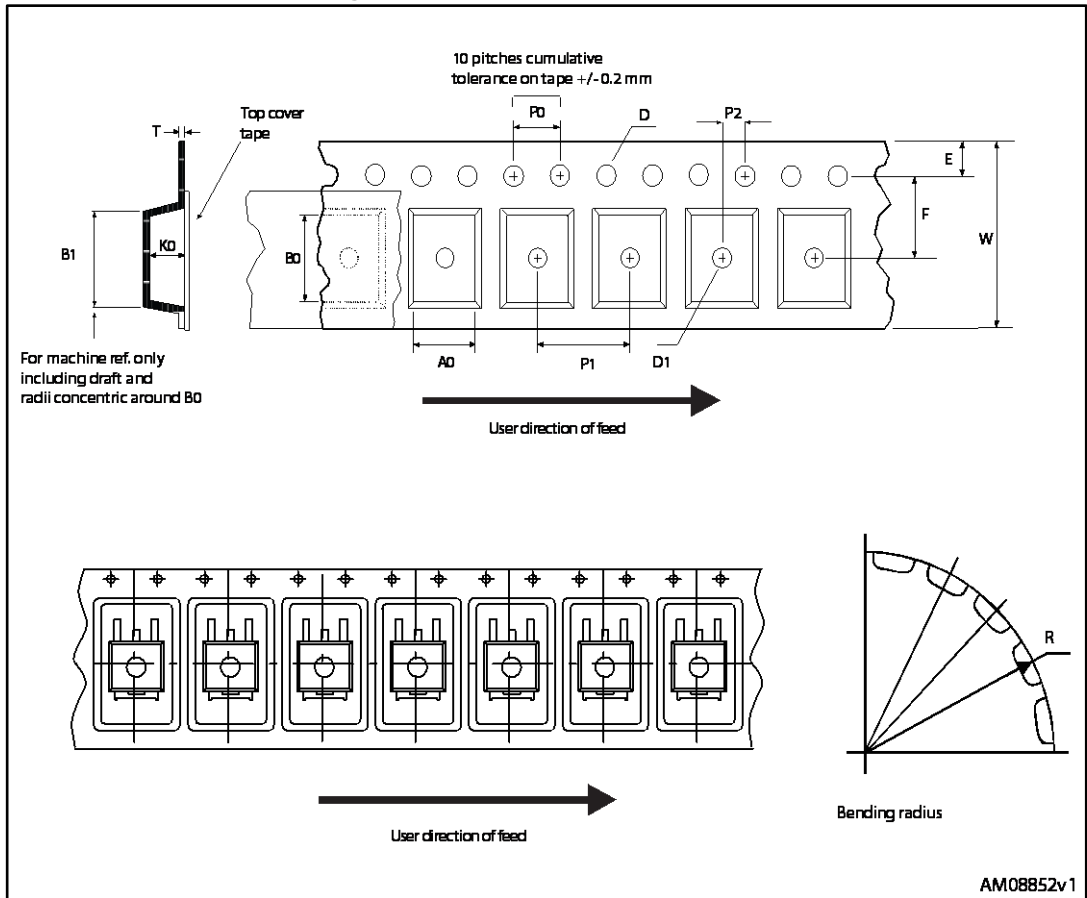


Figure 22: DPAK (TO-252) reel outline

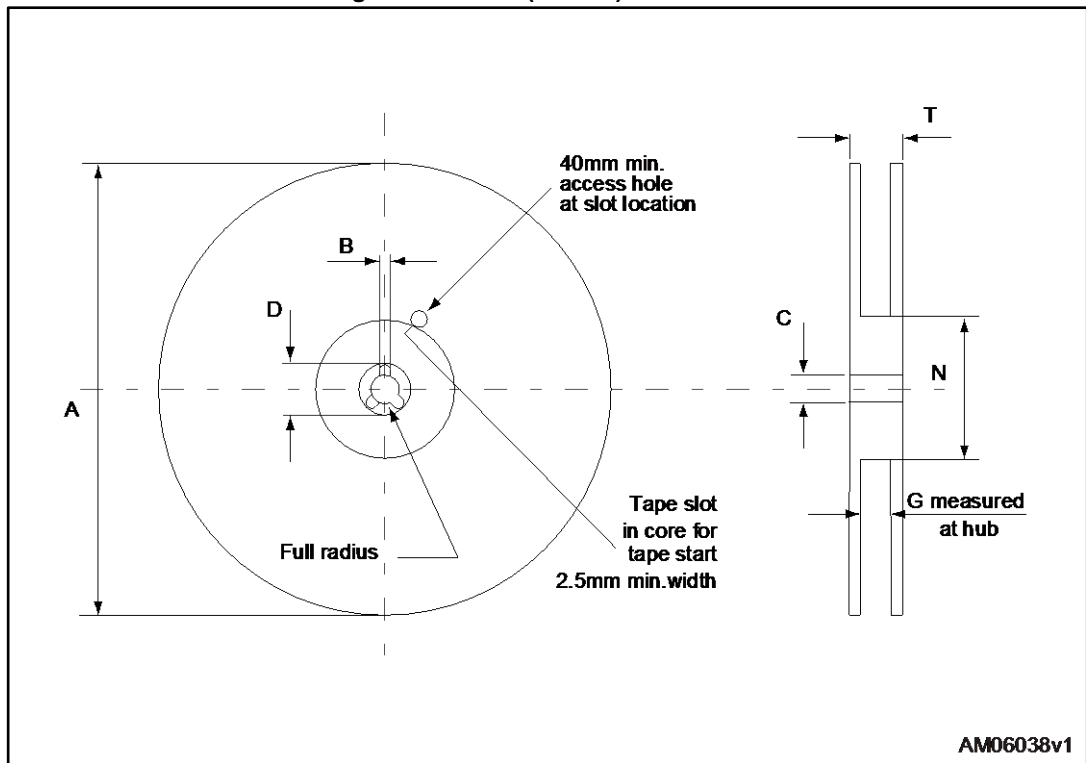


Table 9: DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

5 Revision history

Table 10: Document revision history

Date	Revision	Changes
26-Jul-2016	1	First release.
06-Dec-2016	2	Document status promoted from preliminary to production data. Updated <i>Section 2: "Electrical characteristics"</i> and added <i>Section 2.1: "Electrical characteristics (curves)"</i> . Minor text changes.

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2016 STMicroelectronics – All rights reserved

单击下面可查看定价，库存，交付和生命周期等信息

[>>STMicro\(意法半导体\)](#)