



# STD30PF03LT4 STD30PF03L-1

P-channel 30 V - 0.025  $\Omega$  - 24 A - DPAK / IPAK  
STripFET™ II Power MOSFET

## Features

Type	V <sub>DSS</sub>	R <sub>DS(on) max</sub>	I <sub>D</sub>
STD30PF03LT4	30 V	< 0.028 $\Omega$	24 A
STD30PF03L-1	30 V	< 0.028 $\Omega$	24 A

- Standard outline for easy automated surface mount assembly
- Low threshold device
- Low gate charge

## Application

- Switching applications

## Description

This Power MOSFET is the latest development of STMicroelectronics unique “single feature size” strip-based process. The resulting transistor shows extremely high packing density for low on-resistance and low gate charge.

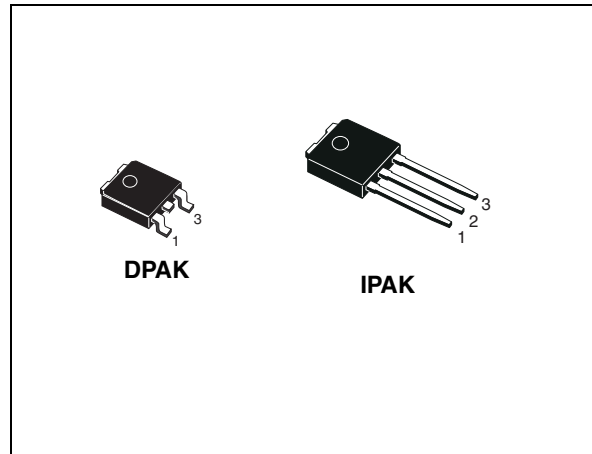


Figure 1. Internal schematic diagram

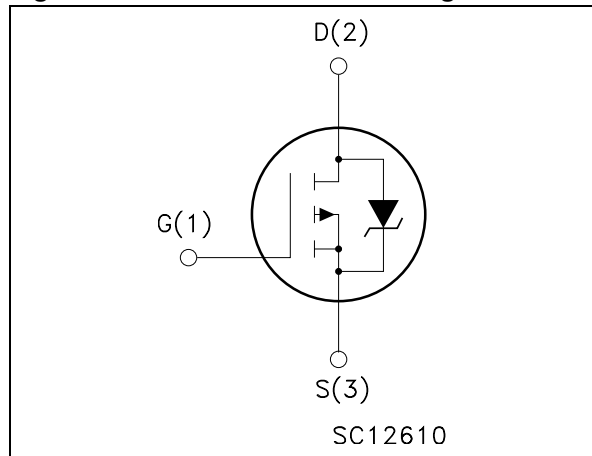


Table 1. Device summary

Order codes	Marking	Package	Packaging
STD30PF03LT4	D30PF03L	DPAK	Tape & reel
STD30PF03L-1	D30PF03L	IPAK	Tube

# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS}=0$ )	30	V
$V_{GS}$	Gate-source voltage	$\pm 16$	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	24	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	24	A
$I_{DM}^{(2)}$	Drain current (pulsed)	96	A
$P_{TOT}$	Total dissipation at $T_C=25\text{ }^\circ\text{C}$	70	W
	Derating factor	0.47	W/ $^\circ\text{C}$
$E_{AS}^{(3)}$	Single pulse avalanche energy	850	mJ
$T_{stg}$	Storage temperature	-55 to 175	$^\circ\text{C}$
$T_j$	Max. operating junction temperature	175	$^\circ\text{C}$

1. Current limited by wire bonding
2. Pulse width limited by safe operating area
3. Starting  $T_j = 25\text{ }^\circ\text{C}$ ,  $I_D = 12\text{ A}$ ,  $V_{DD} = 15\text{ V}$

**Table 3. Thermal data**

Symbol	Parameter	Max value		Unit
		DPAK	IPAK	
$R_{thj-case}$	Thermal resistance junction-case max	2.14		$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	--	100	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}$	Thermal resistance junction-pcb max	50 <sup>(1)</sup>	--	$^\circ\text{C}/\text{W}$
$T_l$	Maximum lead temperature for soldering purpose	--	275	$^\circ\text{C}/\text{W}$

1. When mounted on FR-4 board of 1 inch<sup>2</sup>.

*Note: For the p-channel Power MOSFET actual polarity of voltages and current has to be reversed*

## 2 Electrical characteristics

(T<sub>CASE</sub>=25 °C unless otherwise specified)

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0	30			V
I <sub>DSS</sub>	Zero gate voltage drain current (V <sub>GS</sub> = 0)	V <sub>DS</sub> =Max rating V <sub>DS</sub> =Max rating, T <sub>c</sub> =100 °C			1 10	μA μA
I <sub>GSS</sub>	Gate body leakage current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ±16 V			±100	nA
V <sub>GS(th)</sub>	Gate threshold voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1			V
R <sub>DS(on)</sub>	Static drain-source on resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 12 A V <sub>GS</sub> = 5 V, I <sub>D</sub> = 12 A		0.025 0.032	0.028 0.040	Ω Ω

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g <sub>fs</sub> <sup>(1)</sup>	Forward transconductance	V <sub>DS</sub> =15 V, I <sub>D</sub> = 12 A		23		S
C <sub>iss</sub> C <sub>oss</sub> C <sub>rss</sub>	Input capacitance Output capacitance Reverse transfer capacitance	V <sub>DS</sub> =25 V, f=1MHz, V <sub>GS</sub> =0		1670 345 120		pF pF pF
Q <sub>g</sub> Q <sub>gs</sub> Q <sub>gd</sub>	Total gate charge Gate-source charge Gate-drain charge	V <sub>DD</sub> =15 V, I <sub>D</sub> = 24 A V <sub>GS</sub> =5 V <i>Figure 15</i>		18.6 5.5 11	28	nC nC nC

1. Pulsed: pulse duration = 300 μs, duty cycle 1.5%

Note: For the p-channel Power MOSFET actual polarity of voltages and current has to be reversed



**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD}=25\text{ V}$ , $I_D=24\text{ A}$ , $R_G=4.7\ \Omega$ , $V_{GS}=5\text{ V}$ <i>Figure 14</i>		64		ns
$t_r$	Rise time			122		ns
$t_{d(off)}$	Turn-off delay time				36	ns
$t_f$	Fall time				26	ns

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$I_{SD}$	Source-drain current				24	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				96	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 12\text{ A}$ , $V_{GS}=0$			1.3	V
$t_{rr}$	Reverse recovery time	$I_{SD}=24\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD}=50\text{ V}$ , $T_j=150\text{ }^\circ\text{C}$ <i>Figure 16</i>		40		ns
$Q_{rr}$	Reverse recovery charge				52	$\mu\text{C}$
$I_{RRM}$	Reverse recovery current				2.6	A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

Note: For the p-channel Power MOSFET actual polarity of voltages and current has to be reversed

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

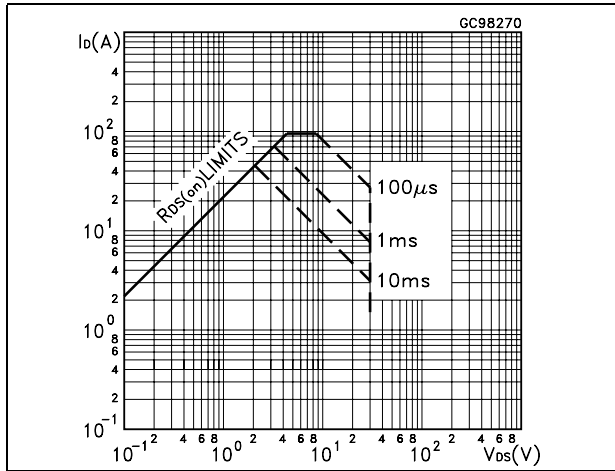


Figure 3. Thermal impedance

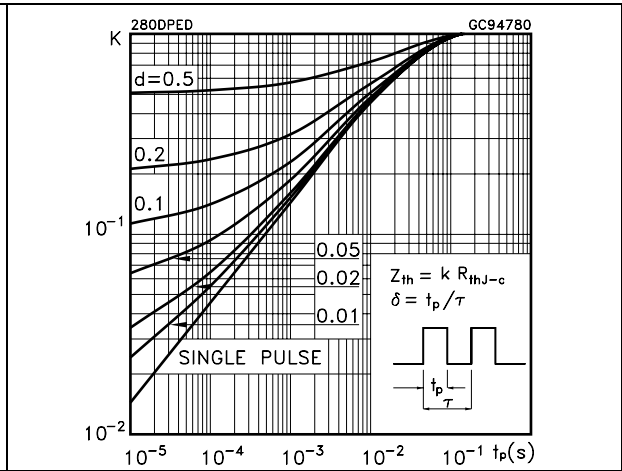


Figure 4. Output characteristics

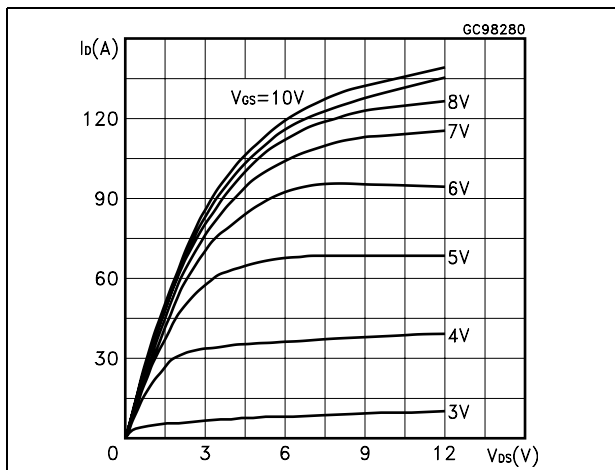


Figure 5. Transfer characteristics

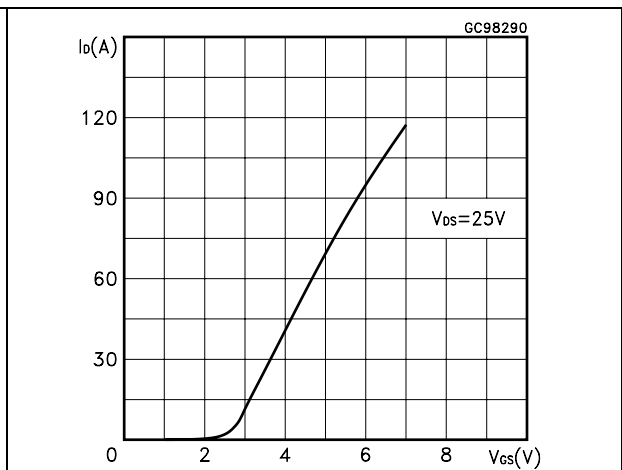


Figure 6. Transconductance

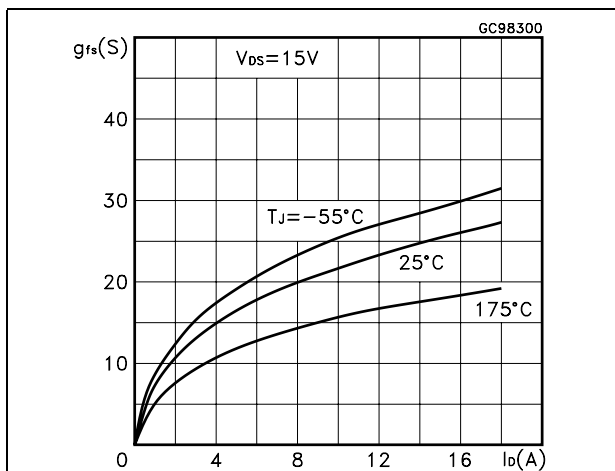


Figure 7. Static drain-source on resistance

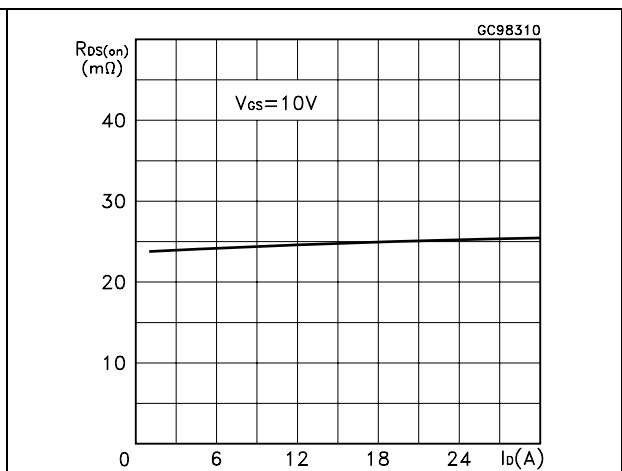


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

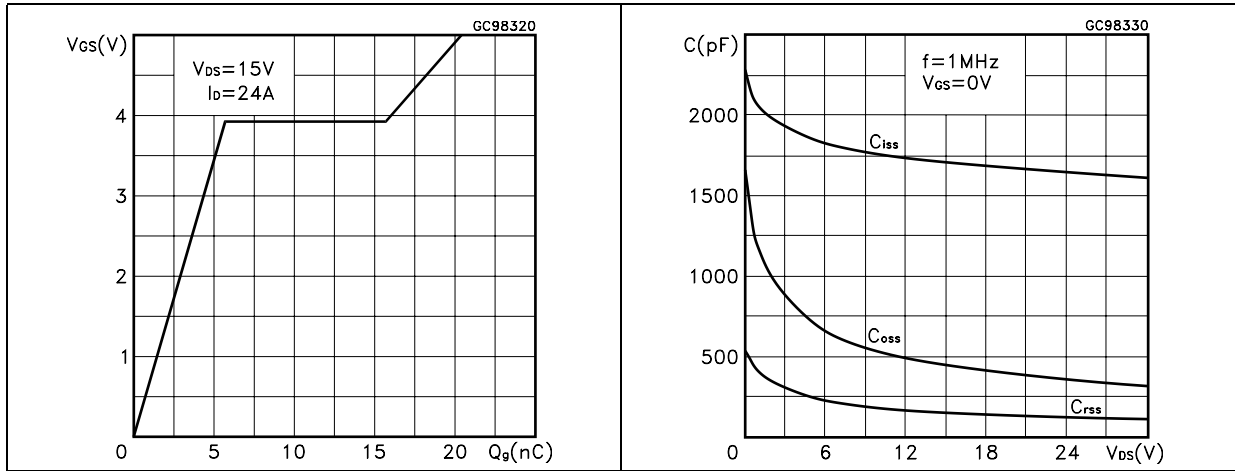


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on resistance vs temperature

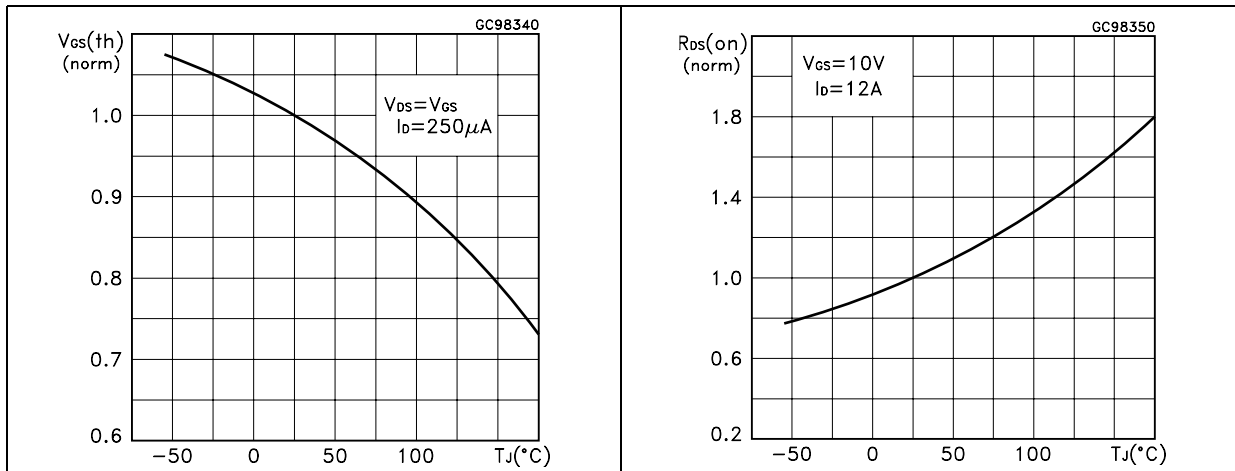
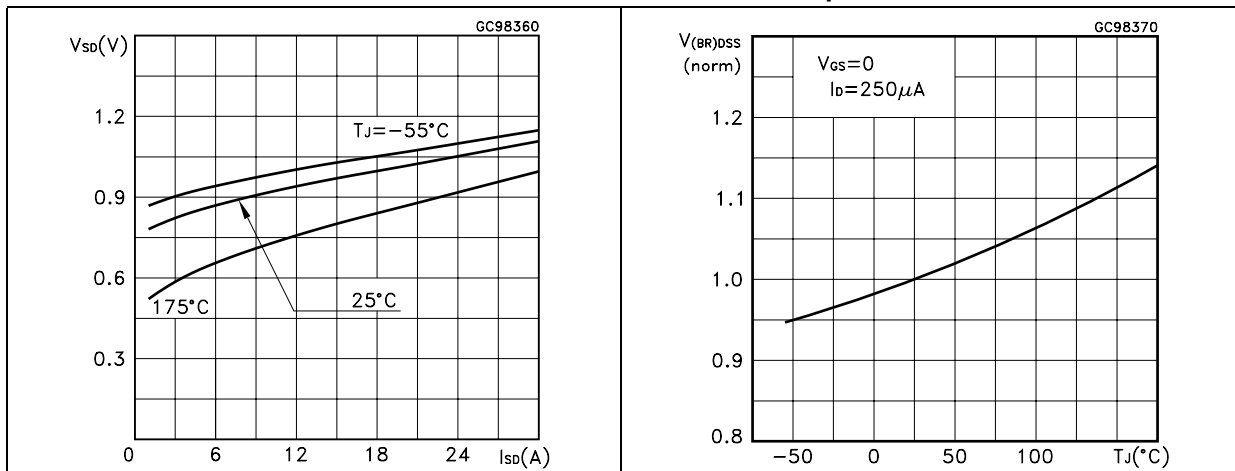


Figure 12. Source-drain diode forward characteristics Figure 13. Normalized breakdown voltage vs temperature



### 3 Test circuit

Figure 14. Switching times test circuit for resistive load

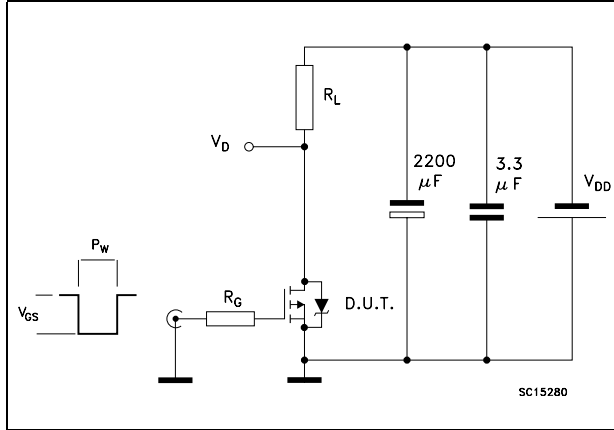


Figure 15. Gate charge test circuit

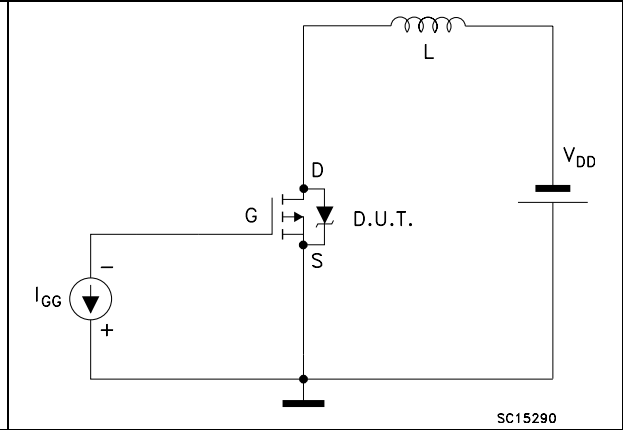
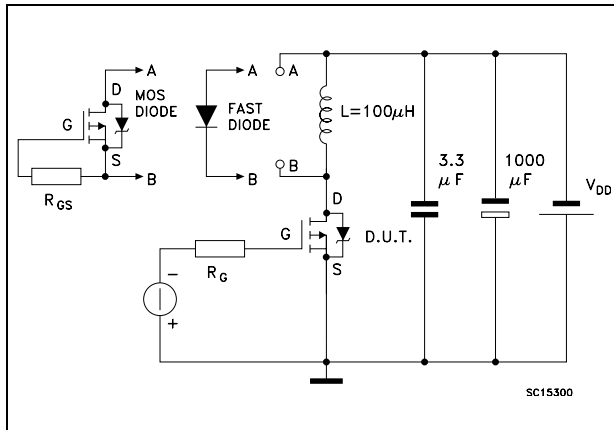


Figure 16. Test circuit for diode recovery behavior



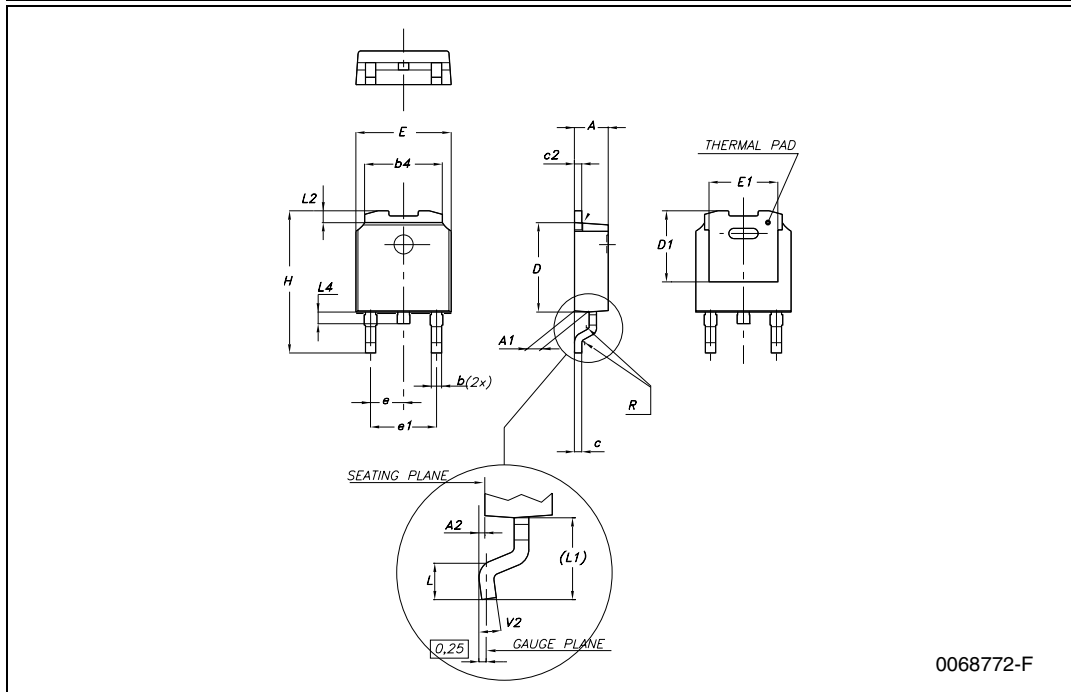
## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)



**DPAK MECHANICAL DATA**

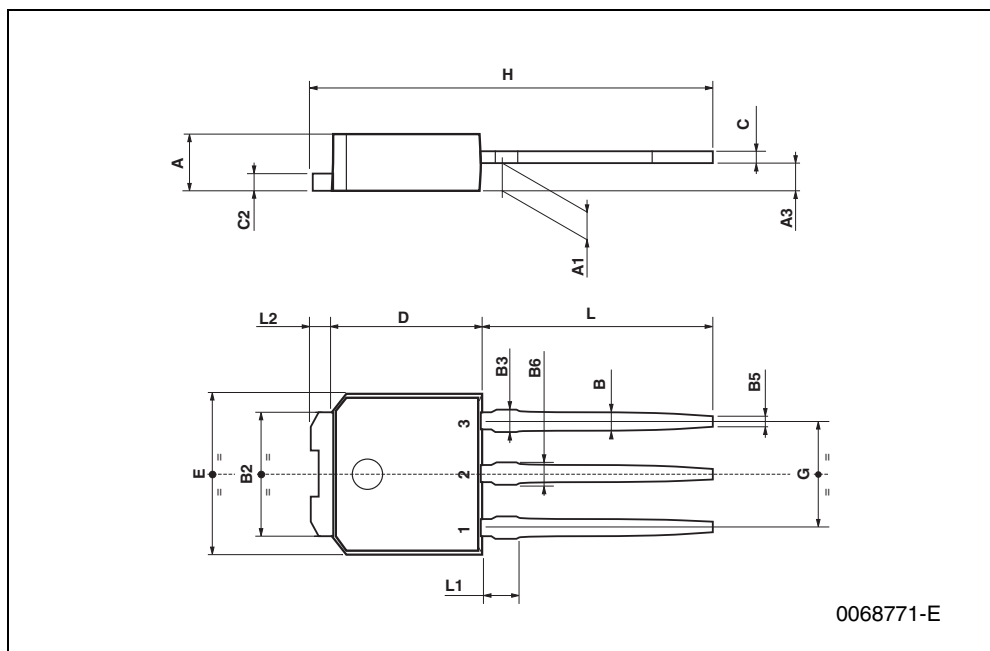
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.9	0.025		0.035
b4	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
D1		5.1			0.200	
E	6.4		6.6	0.252		0.260
E1		4.7			0.185	
e		2.28			0.090	
e1	4.4		4.6	0.173		0.181
H	9.35		10.1	0.368		0.397
L	1			0.039		
(L1)		2.8			0.110	
L2		0.8			0.031	
L4	0.6		1	0.023		0.039
R		0.2			0.008	
V2	0°		8°	0°		8°



0068772-F

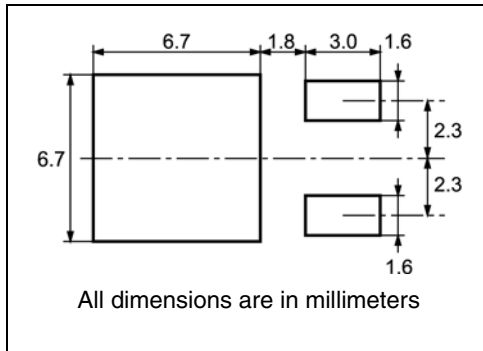
**TO-251 (IPAK) MECHANICAL DATA**

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A3	0.7		1.3	0.027		0.051
B	0.64		0.9	0.025		0.031
B2	5.2		5.4	0.204		0.212
B3			0.85			0.033
B5		0.3			0.012	
B6			0.95			0.037
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	15.9		16.3	0.626		0.641
L	9		9.4	0.354		0.370
L1	0.8		1.2	0.031		0.047
L2		0.8	1		0.031	0.039



## 5 Packaging mechanical data

### DPAK FOOTPRINT



### TAPE AND REEL SHIPMENT

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	16.4	18.4	0.645	0.724
N	50		1.968	
T		22.4		0.881

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	6.8	7	0.267	0.275
B0	10.4	10.6	0.409	0.417
B1		12.1		0.476
D	1.5	1.6	0.059	0.063
D1	1.5		0.059	
E	1.65	1.85	0.065	0.073
F	7.4	7.6	0.291	0.299
K0	2.55	2.75	0.100	0.108
P0	3.9	4.1	0.153	0.161
P1	7.9	8.1	0.311	0.319
P2	1.9	2.1	0.075	0.082
R	40		1.574	
W	15.7	16.3	0.618	0.641

## 6 Revision history

**Table 8. Document revision history**

Date	Revision	Changes
14-Jan-2008	2	– Document reformatted – Corrected marking on <a href="#">Table 1: Device summary</a>

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