

STFU23N80K5

N-channel 800 V, 0.23 Ω typ., 16 A MDmesh™ K5 Power MOSFET in a TO-220FP ultra narrow leads package

Datasheet - production data

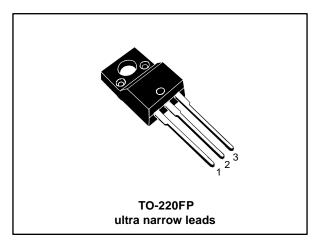
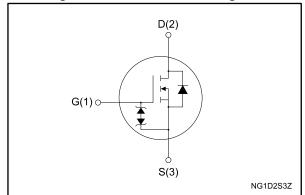


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	ΙD	Ртот
STFU23N80K5	800 V	0.28 Ω	16 A	35 W

- Industry's lowest R_{DS(on)} x area
- Industry's best FoM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

Applications

• Switching applications

Description

This very high voltage N-channel Power MOSFET is designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Table 1: Device summary

Order code	Marking	Package	Packing
STFU23N80K5	23N80K5	TO-220FP ultra narrow leads	Tube

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STFU23N80K5 Electrical ratings

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter		Unit
V _G s	Gate-source voltage	±30	V
1-	Drain current (continuous) at T _{case} = 25 °C	16	
l _D	Drain current (continuous) at T _{case} = 100 °C	10	Α
I _{DM} ⁽¹⁾	Drain current (pulsed)	64	Α
Ртот	Total dissipation at T _{case} = 25 °C 35		W
dv/dt ⁽²⁾	Peak diode recovery voltage slope		V/ns
dv/dt ⁽³⁾	MOSFET dv/dt ruggedness	50	V/IIS
V _{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t= 1 s, Tc= 25 °C)		V
T _{stg}	Storage temperature range		°C
Tj	Operating junction temperature range	-55 to 150	C

Notes:

Table 3: Thermal data

Symbol	Symbol Parameter		Unit
R _{thj-case}	Thermal resistance junction-case	3.6	°C/W
R _{thj-amb}	Thermal resistance junction-ambient	50	C/VV

Table 4: Avalanche characteristics

	Symbol	Parameter	Value	Unit
Ī	I _{AR} ⁽¹⁾	Avalanche current, repetitive or not repetitive	5	Α
	E _{AS} ⁽²⁾	Single pulse avalanche energy	400	mJ

Notes:

⁽¹⁾Pulse width is limited by safe operating area.

 $^{^{(2)}}I_{SD} \leq$ 16 A, di/dt=100 A/ μs , VDs peak < V(BR)DSS, VDD = 80% V(BR)DSS

 $^{^{(3)}}V_{DS} \le 640 \ V$

 $[\]ensuremath{^{(1)}}\xspace Pulse$ width limited by $T_{jmax}.$

 $^{^{(2)}}Starting~T_j=25~^{\circ}C,~I_D=I_{AR},~V_{DD}=50~V.$

Electrical characteristics STFU23N80K5

2 Electrical characteristics

(T_{case} = 25 °C unless otherwise specified)

Table 5: Static

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	$V_{GS} = 0 \text{ V}, I_D = 1 \text{ mA}$	800			V
	Zara gata valtaga drain	$V_{GS} = 0 \text{ V}, V_{DS} = 800 \text{ V}$			1	
IDSS	Zero gate voltage drain current	$V_{GS} = 0 \text{ V}, V_{DS} = 800 \text{ V},$ $T_{case} = 125 \text{ °C}^{(1)}$			50	μΑ
I _{GSS}	Gate-body leakage current	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			±10	μΑ
V _{GS(th)}	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 100 \mu A$	3	4	5	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 8 A		0.23	0.28	Ω

Notes:

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
Ciss	Input capacitance		ı	1000	ı	
Coss	Output capacitance	$V_{DS} = 100 \text{ V}, f = 1 \text{ MHz},$ $V_{GS} = 0 \text{ V}$	1	65	1	pF
Crss	Reverse transfer capacitance	VG3 - V	ı	1.5	ı	
$C_{O(tr)}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0$ to 640 V, $V_{GS} = 0$ V	-	165	-	~ F
C _{O(er)} (2)	Equivalent output capacitance	$V_{DS} = 0$ to 640 V, $V_{GS} = 0$ V	ı	59	ı	pF
R _G	Intrinsic gate resistance	$f = 1 \text{ MHz}, I_D = 0 \text{ A}$	ı	4.7	ı	Ω
Qg	Total gate charge	V _{DD} = 640 V, I _D = 16 A,	ı	33	1	
Qgs	Gate-source charge	V _{GS} = 0 to 10 V (see Figure 14: "Test circuit	-	6	1	nC
Q_{gd}	Gate-drain charge	for gate charge behavior")	-	25	-	

Notes:

 $^{^{(1)}}$ Defined by design, not subject to production test.

 $^{^{(1)}}$ Time related is defined as a constant equivalent capacitance giving the same charging time as Coss when V_{DS} increases from 0 to 80% V_{DSS}.

 $^{^{(2)}}$ Energy related is defined as a constant equivalent capacitance giving the same stored energy as Coss when V_{DS} increases from 0 to 80% V_{DSS}.

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 400 V, I _D = 8 A	-	14	-	
tr	Rise time	$R_G = 4.7 \Omega$, $V_{GS} = 10 V$ (see Figure 13: "Test circuit for	ı	9	1	
t _{d(off)}	Turn-off delay time	resistive load switching times"	-	48	-	ns
t _f	Fall time	and Figure 18: "Switching time waveform")	-	9	-	

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I _{SD}	Source-drain current		-		16	Α
I _{SDM} ⁽¹⁾	Source-drain current (pulsed)		1		64	Α
V _{SD} ⁽²⁾	Forward on voltage	V _{GS} = 0 V, I _{SD} = 16 A	-		1.5	V
t _{rr}	Reverse recovery time	$I_{SD} = 16 \text{ A, di/dt} = 100 \text{ A/}\mu\text{s,}$	-	410		ns
Qrr	Reverse recovery charge	V _{DD} = 60 V (see Figure 15: "Test circuit for	-	7		μC
I _{RRM}	Reverse recovery current	inductive load switching and diode recovery times")	-	34		А
t _{rr}	Reverse recovery time	$I_{SD} = 16 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s},$	-	650		ns
Qrr	Reverse recovery charge	$V_{DD} = 60 \text{ V}, T_j = 150 \text{ °C}$ (see Figure 15: "Test circuit for	-	10		μC
I _{RRM}	Reverse recovery current	inductive load switching and diode recovery times")	-	32		Α

Notes:

Table 9: Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
$V_{(BR)GSO} \\$	Gate-source breakdown voltage	$I_{GS} = \pm 1 \text{ mA}, I_D = 0 \text{ A}$	±30	-	-	V

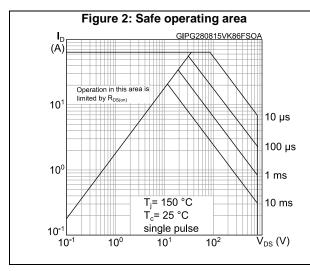
The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.



⁽¹⁾ Pulse width is limited by safe operating area.

 $^{^{(2)}}$ Pulse test: pulse duration = 300 μ s, duty cycle 1.5%.

2.1 Electrical characteristics (curves)



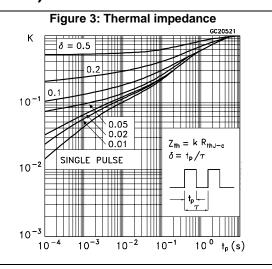
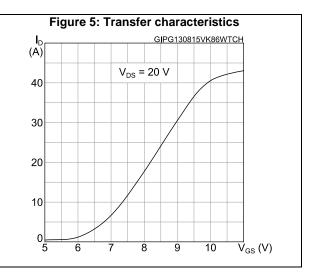
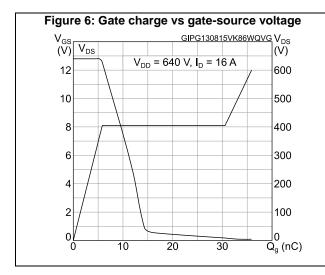
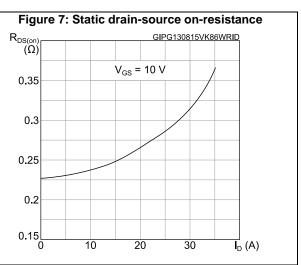


Figure 4: Output characteristics GIPG130815VK86WOCH (A)40 V_{GS}= 11 V V_{GS}= 10 V 30 V_{GS} = 9 V 20 V_{GS}= 8 V 10 V_{GS} = 7 V V_{GS} = 6 V0 12 16 $\overline{\mathsf{V}}_{\mathsf{DS}}(\mathsf{V})$







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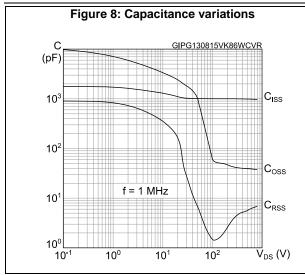


Figure 9: Normalized gate threshold voltage vs temperature

V_{GS(th)}
(norm.)

1.2

1.0

0.8

0.6

0.4

0.2

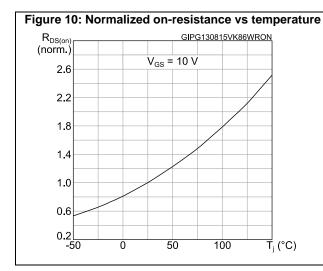
-50

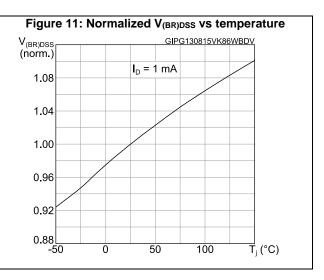
0

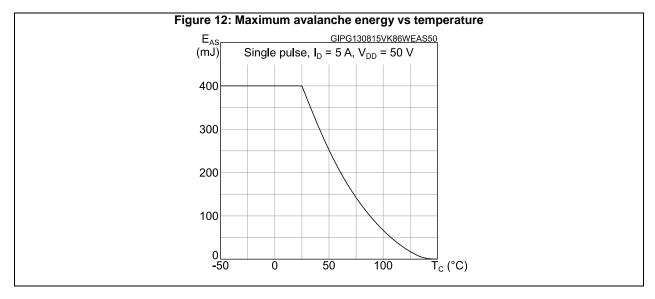
50

100

T_j(°C)







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Test circuits STFU23N80K5

3 Test circuits

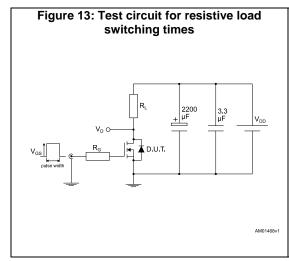


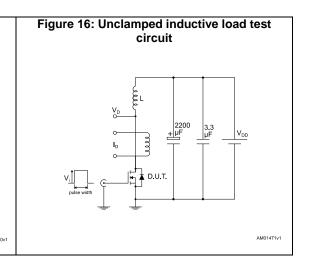
Figure 14: Test circuit for gate charge behavior

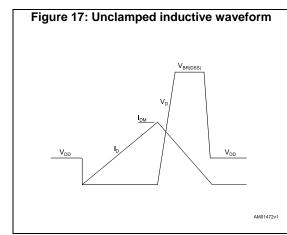
12 V 47 KΩ 100 NF D.U.T.

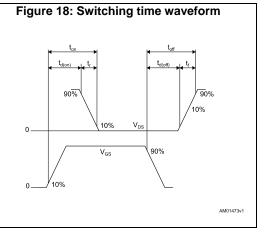
VGS 1 KΩ 100 NF D.U.T.

AM01469v1

Figure 15: Test circuit for inductive load switching and diode recovery times







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Package information 4

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

TO-220FP ultra narrow leads package information 4.1

В F1(x3)D G1 Ε 8576148_1

Figure 19: TO-220FP ultra narrow leads package outline

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Table 10: TO-220FP ultra narrow leads mechanical data

Dim		mm	
Dim.	Min.	Тур.	Max.
А	4.40		4.60
В	2.50		2.70
D	2.50		2.75
Е	0.45		0.60
F	0.65		0.75
F1	-		0.90
G	4.95		5.20
G1	2.40	2.54	2.70
Н	10.00		10.40
L2	15.10		15.90
L3	28.50		30.50
L4	10.20		11.00
L5	2.50		3.10
L6	15.60		16.40
L7	9.00		9.30
L8	3.20		3.60
L9	-		1.30
Dia.	3.00		3.20

STFU23N80K5 Revision history

5 Revision history

Table 11: Document revision history

Date	Revision	Changes
21-Feb-2017	1	First release

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