# H3LIS331DL

Datasheet

## High-*g*, low-power 3-axis digital accelerometer


**TFLGA-16L**
**3 x 3 x 1.0 mm³**

| Product status link |
|---|
| H3LIS331DL |

| Product summary | | |
|---|---|---|
| **Order code** | H3LIS331DL | H3LIS331DLTR |
| **Temp. range [°C]** | -40 to +85 | |
| **Package** | TFLGA-16L<br>3 x 3 x 1.0 mm³ | |
| **Packing** | Tray | Tape and reel |

| Product resources |
|---|
| TN0018 (design and soldering) |

| Product label |
|---|
| SUSTAINABLE TECHNOLOGY |

## Features

- 3-axis digital accelerometer
- ±100*g*/±200*g*/±400*g* dynamically selectable full scales
- Output data rate (ODR) from 0.5 Hz up to 1 kHz
- Low power consumption down to 7 µA in low-power mode
- Power savings and sleep-to-wake-up functions
- Programmable interrupts
- I²C/SPI digital output interface
- Supply voltage, 2.16 V to 3.6 V
- Low-voltage compatible IOs, 1.8 V
- 10000 *g* high-shock survivability
- ECOPACK and RoHS compliant

## Applications

- Car crash detection in wearables and personal electronics
- Shock detection
- Impact recognition and logging
- Concussion detection in impact sports
- Asset tracking
- Augmented sports equipment

## Description

The H3LIS331DL is a high-*g*, low-power, high-performance 3-axis linear accelerometer with digital I²C/SPI serial interface standard output.

The device features ultralow-power operational modes that allow advanced power saving and smart sleep-to-wake-up functions.

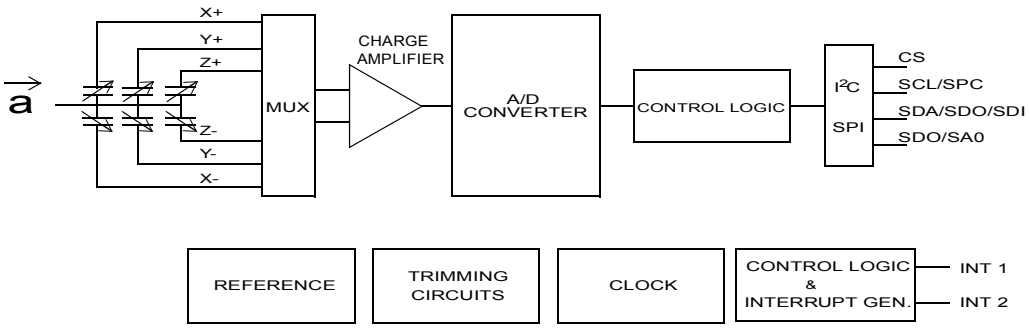
The H3LIS331DL has dynamically user-selectable full scales of ±100*g*/±200*g*/±400*g* and it is capable of measuring accelerations with output data rates from 0.5 Hz to 1 kHz.

The H3LIS331DL is available in a small thin plastic land grid array package (LGA) and it is guaranteed to operate over an extended temperature range from -40 °C to +85 °C.

# 1 Block diagram and pin description

## 1.1 Block diagram

Figure 1. **Block diagram**



## 1.2 Pin description

Figure 2. **Pin connections**

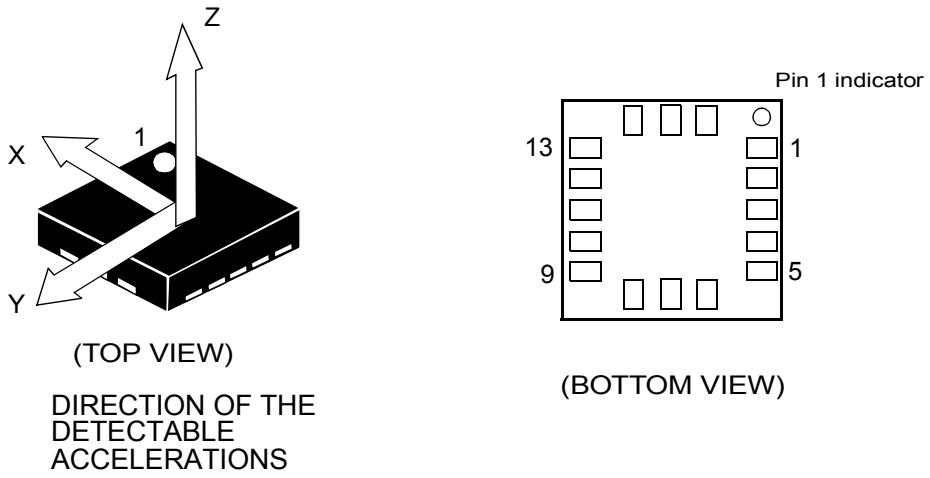



Table 1. **Pin description**

| Pin # | Name | Function |
|---|---|---|
| 1 | Vdd_IO | Power supply for I/O pins |
| 2 | NC | Not connected |
| 3 | NC | Not connected |
| 4 | SCL<br>SPC | I²C serial clock (SCL)<br>SPI serial port clock (SPC) |
| 5 | GND | 0 V supply |
| 6 | SDA<br>SDI<br>SDO | I²C serial data (SDA)<br>SPI serial data input (SDI)<br>3-wire interface serial data output (SDO) |
| 7 | SDO<br>SA0 | SPI serial data output (SDO)<br>I²C less significant bit of the device address (SA0) |
| 8 | CS | SPI enable<br>I²C/SPI mode selection (1: I²C mode; 0: SPI enabled) |
| 9 | INT 2 | Inertial interrupt 2 |
| 10 | Reserved | Connect to GND |
| 11 | INT 1 | Inertial interrupt 1 |
| 12 | GND | 0 V supply |
| 13 | GND | 0 V supply |
| 14 | Vdd | Power supply |
| 15 | Reserved | Connect to Vdd |
| 16 | GND | 0 V supply |

# 2 Mechanical and electrical specifications

## 2.1 Mechanical characteristics

@ Vdd = 2.5 V, T = 25 °C unless otherwise noted. The product is factory calibrated at 2.5 V. The operational power supply range is from 2.16 V to 3.6 V. The product calibration is done at ±1 *g*.

**Table 2. Mechanical characteristics**

| Symbol | Parameter | Test conditions | Min. | Typ.(1) | Max. | Unit |
|---|---|---|---|---|---|---|
| FS | Measurement range(2) | FS bit set to 00 | | ±100 | | *g* |
| | | FS bit set to 01 | | ±200 | | |
| | | FS bit set to 11 | | ±400 | | |
| So | Sensitivity(3) | FS bit set to 00<br>12-bit representation | | 49 | | mg/digit |
| | | FS bit set to 01 mg/digit<br>12-bit representation | | 98 | | |
| | | FS bit set to 11<br>12-bit representation | | 195 | | |
| TCSo | Sensitivity change vs. temperature | FS bit set to 00 | | ±0.01 | | %/°C |
| TyOff | Typical zero-*g* level offset accuracy(4) | FS bit set to 00 | | ±1 | | *g* |
| TCOff | Zero-*g* level change vs. temperature | Max. delta from 25 °C | | ±5 | | mg/°C |
| An | Acceleration noise density | FS bit set to 00 | | 15 | | mg/√Hz |
| NL | Nonlinearity | FS bit set to 00<br>Range -70 *g* .. +70 *g* | | 2 | | %FS |
| Top | Operating temperature range | | -40 | | +85 | °C |
| Wh | Product weight | | | 20 | | mgram |

1. *Typical specifications are not guaranteed.*
2. *Verified by wafer level test and measurement of initial offset and sensitivity*
3. *Factory calibrated at ±1 g*
4. *Offset can be eliminated by enabling the built-in high-pass filter.*

## 2.2 Electrical characteristics

@ Vdd = 2.5 V, T = 25 °C unless otherwise noted. The product is factory calibrated at 2.5 V. The operational power supply range is from 2.16 V to 3.6 V.

**Table 3. Electrical characteristics**

| Symbol | Parameter | Test conditions | Min. | Typ.(1) | Max. | Unit |
|---|---|---|---|---|---|---|
| Vdd | Supply voltage | | 2.16 | 2.5 | 3.6 | V |
| Vdd_IO | I/O pins supply voltage(2) | | 1.71 | | Vdd+0.1 | V |
| Idd | Current consumption in normal mode | ODR 50 Hz<br>ODR 400 Hz<br>ODR 1000 Hz | | 260<br>300<br>370 | | µA |
| IddLP | Current consumption in low-power mode(3) | ODR 0.5 Hz<br>ODR 1 Hz<br>ODR 5 Hz<br>ODR 10 Hz | | 7<br>10<br>38<br>75 | | µA |
| IddPdn | Current consumption in power-down mode | | | 1 | | µA |
| VIH | Digital high-level input voltage | | 0.8*Vdd_IO | | | V |
| VIL | Digital low-level input voltage | | | | 0.2*Vdd_IO | V |
| VOH | High-level output voltage | | 0.9*Vdd_IO | | | V |
| VOL | Low-level output voltage | | | | 0.1*Vdd_IO | V |
| ODR | Output data rate in normal mode | DR bit set to 00 | | 50 | | Hz |
| | | DR bit set to 01 | | 100 | | |
| | | DR bit set to 10 | | 400 | | |
| | | DR bit set to 11 | | 1000 | | |
| $ODR_{LP}$ | Output data rate in low-power mode | PM bit set to 010 | | 0.5 | | Hz |
| | | PM bit set to 011 | | 1 | | |
| | | PM bit set to 100 | | 2 | | |
| | | PM bit set to 101 | | 5 | | |
| | | PM bit set to 110 | | 10 | | |
| BW | System bandwidth(4) | | | ODR/2 | | Hz |
| Ton | Turn-on time(5) | ODR = 100 Hz | | 1/ODR+1ms | | s |
| Top | Operating temperature range | | -40 | | +85 | °C |

1. *Typical specifications are not guaranteed.*
2. *It is possible to remove Vdd maintaining Vdd_IO without blocking the communication busses; in this condition the measurement chain is powered off.*
3. *Based on characterization data on a limited number of samples. Not measured in production.*
4. *Refer to Table 16 for filter cutoff frequency.*
5. *Time to obtain valid data after exiting power-down mode.*

## 2.3 Communication interface characteristics

### 2.3.1 SPI - serial peripheral interface

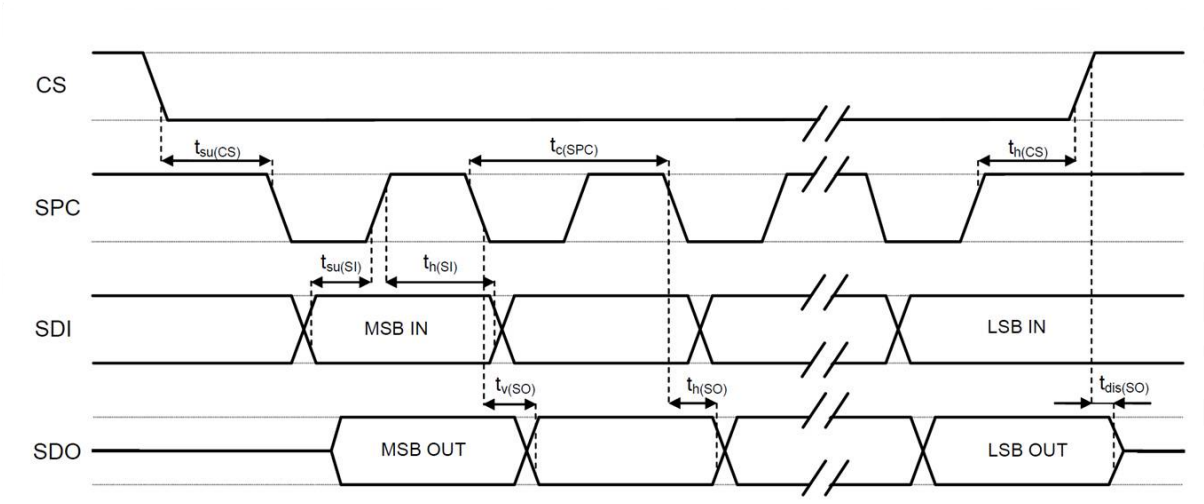
Subject to general operating conditions for Vdd and Top.

**Table 4. SPI slave timing values**

| Symbol | Parameter | Value(1) | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(SPC)}$ | SPI clock cycle | 100 | | ns |
| $f_{c(SPC)}$ | SPI clock frequency | | 10 | MHz |
| $t_{su(CS)}$ | CS setup time | 6 | | ns |
| $t_{h(CS)}$ | CS hold time | 8 | | |
| $t_{su(SI)}$ | SDI input setup time | 5 | | |
| $t_{h(SI)}$ | SDI input hold time | 15 | | |
| $t_{v(SO)}$ | SDO valid output time | | 50 | |
| $t_{h(SO)}$ | SDO output hold time | 9 | | |
| $t_{dis(SO)}$ | SDO output disable time | | 50 | |

1. *Values are guaranteed at 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results, not tested in production.*

**Figure 3. SPI slave timing diagram**




*Note: Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO for both input and output ports.*
*When no communication is ongoing, data on CS, SPC, SDI and SDO are driven by internal pull-up resistors.*

### 2.3.2 I²C - inter-IC control interface

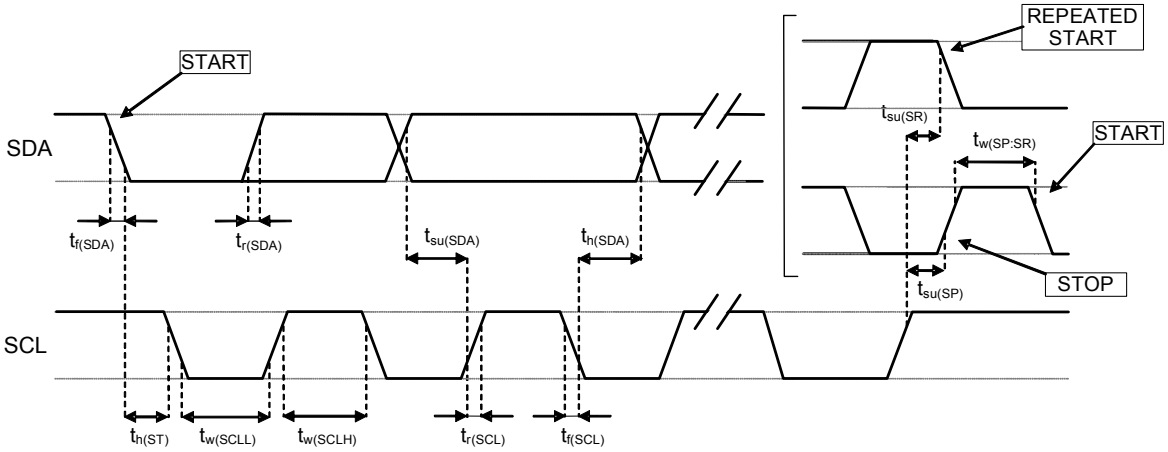
Subject to general operating conditions for Vdd and Top.

**Table 5. I²C slave timing values**

| Symbol | Parameter | I²C standard mode(1) | | I²C fast mode(1) | | Unit |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| $f_{(SCL)}$ | SCL clock frequency | 0 | 100 | 0 | 400 | kHz |
| $t_{w(SCLL)}$ | SCL clock low time | 4.7 | | 1.3 | | µs |
| $t_{w(SCLH)}$ | SCL clock high time | 4.0 | | 0.6 | | |
| $t_{su(SDA)}$ | SDA setup time | 250 | | 100 | | ns |
| $t_{h(SDA)}$ | SDA data hold time | 0.01 | 3.45 | 0.01 | 0.9 | µs |
| $t_{r(SDA)}$ $t_{r(SCL)}$ | SDA and SCL rise time | | 1000 | $20 + 0.1C_b$(2) | 300 | ns |
| $t_{f(SDA)}$ $t_{f(SCL)}$ | SDA and SCL fall time | | 300 | $20 + 0.1C_b$(2) | 300 | |
| $t_{h(ST)}$ | START condition hold time | 4 | | 0.6 | | µs |
| $t_{su(SR)}$ | Repeated START condition setup time | 4.7 | | 0.6 | | |
| $t_{su(SP)}$ | STOP condition setup time | 4 | | 0.6 | | |
| $t_{w(SP:SR)}$ | Bus free time between STOP and START condition | 4.7 | | 1.3 | | |

1. *Data based on standard I2C protocol requirement, not tested in production.*
2. *$C_b$ = total capacitance of one bus line in pF.*

**Figure 4. I²C slave timing diagram**




*Note: Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO for both ports.*

## 2.4 Absolute maximum ratings

Stresses above those listed as absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Table 6. Absolute maximum ratings**

| Symbol | Ratings | Maximum value | Unit |
|---|---|---|---|
| Vdd | Supply voltage | -0.3 to 4.8 | V |
| Vdd_IO | I/O pins supply voltage | -0.3 to 4.8 | V |
| Vin | Input voltage on any control pin (CS, SCL/SPC, SDA/SDI/SDO, SDO/SA0) | -0.3 to Vdd_IO +0.3 | V |
| $A_{UNP}$ | Acceleration (any axis, unpowered) | 3000 *g* for 0.5 ms | |
| | | 10000 *g* for 0.1 ms | |
| $T_{OP}$ | Operating temperature range | -40 to +85 | °C |
| $T_{STG}$ | Storage temperature range | -40 to +125 | °C |
| ESD | Electrostatic discharge protection | 4 (HBM) | kV |
| | | 1.5 (CDM) | kV |
| | | 200 (MM) | V |

*Note: Supply voltage on any pin should never exceed 4.8 V.*

This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.

This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part.

# 3 Terminology

## 3.1 Sensitivity

Sensitivity describes the gain of the sensor and can be determined by applying 1 *g* acceleration to it. The sensor can measure DC accelerations, which can be done easily by pointing the axis of interest towards the center of the Earth, noting the output value, rotating the sensor by 180 degrees (pointing to the sky), and noting the output value again. By doing so, ±1 *g* acceleration is applied to the sensor. Subtracting the larger output value from the smaller one, and dividing the result by two, leads to the actual sensitivity of the sensor. This value changes very little over temperature and time. The sensitivity tolerance describes the range of sensitivities of a large population of sensors.

## 3.2 Zero-*g* level

The zero-*g* level offset (TyOff) describes the deviation of an actual output signal from the ideal output signal if no acceleration is present. A sensor in a steady-state on a horizontal surface measures 0 *g* for the X-axis and 0 *g* for the Y-axis whereas the Z-axis measures 1 *g*. The output is ideally in the middle of the dynamic range of the sensor (content of OUT registers 00h, data expressed as two's complement number). A deviation from the ideal value in this case is called zero-*g* offset. Offset is, to some extent, a result of stress to the MEMS sensor and therefore can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. Offset changes little over temperature, refer to "Zero-*g* level change vs. temperature" (see TCOff in Table 2). The zero-*g* level tolerance (TyOff) describes the standard deviation of the range of zero-*g* levels of a population of sensors.

## 3.3 Sleep-to-wake-up

The "sleep-to-wake-up" function, in conjunction with low-power mode, allows further reducing the system power consumption and developing new smart applications.

The H3LIS331DL may be set in a low-power operating mode, characterized by lower date rate refreshes. In this way the device, even if sleeping, continues to sense acceleration and generate interrupt requests.

When the sleep-to-wake-up function is activated, the H3LIS331DL is able to automatically wake up as soon as the interrupt event has been detected, increasing the output data rate and bandwidth.

With this feature the system may be efficiently switched from low-power mode to full performance, depending on user-selectable positioning and acceleration events, therefore ensuring power saving and flexibility.

# 4 Functionality

The H3LIS331DL is a “nano”, low-power, digital output 3-axis linear accelerometer housed in an LGA package. The complete device includes a sensing element and an IC interface able to take the information from the sensing element and provide a signal to the application over an I²C/SPI serial interface.

## 4.1 Sensing element

A proprietary process is used to create a surface micromachined accelerometer. The technology allows processing suspended silicon structures, which are attached to the substrate in a few points called anchors and are free to move in the direction of the sensed acceleration. To be compatible with traditional packaging techniques, a cap is placed on top of the sensing element to avoid blocking the moving parts during the molding phase of the plastic encapsulation.

When an acceleration is applied to the sensor, the proof mass displaces from its nominal position, causing an imbalance in the capacitive half bridge. This imbalance is measured using charge integration in response to a voltage pulse applied to the capacitor.

At steady-state, the nominal value of the capacitors is a few pF and when an acceleration is applied, the maximum variation of the capacitive load is in the fF range.

## 4.2 IC interface

The complete measurement chain is composed of a low-noise capacitive amplifier, which converts the capacitive unbalance of the MEMS sensor into an analog voltage that is available to the user through an analog-to-digital converter.

The acceleration data may be accessed through an I²C/SPI interface, making the device particularly suitable for direct interfacing with a microcontroller.

The H3LIS331DL features a data-ready signal (RDY), which indicates when a new set of measured acceleration data is available, therefore simplifying data synchronization in the digital system that uses the device.

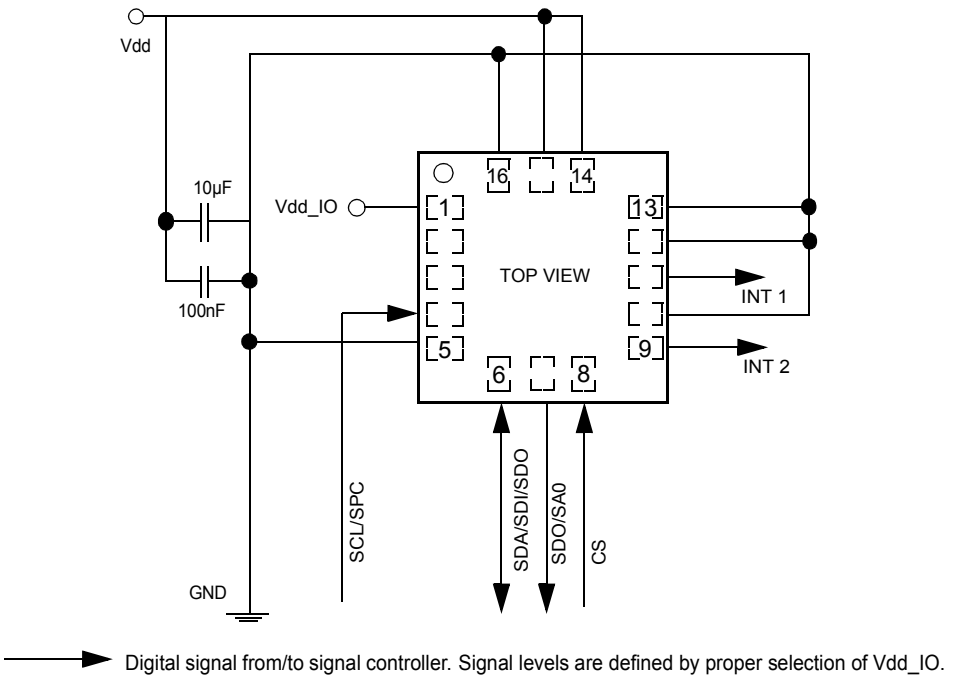
## 4.3 Factory calibration

The IC interface is factory calibrated for sensitivity (So) and zero-*g* level (TyOff).

The trim values are stored inside the device in nonvolatile memory. When the device is turned on, the trim parameters are downloaded into the registers to be used during active operation. This allows the device to be used without further calibration.

# 5 Application hints

Figure 5. **H3LIS331DL electrical connections**




The device core is supplied through the Vdd line while the I/O pins are supplied through the Vdd_IO line. Power supply decoupling capacitors (100 nF ceramic, 10 µF aluminum) should be placed as near as possible to pin 14 of the device (common design practice).

All the voltage and ground supplies must be present at the same time to have proper behavior of the IC (refer to Figure 5). It is possible to remove Vdd maintaining Vdd_IO without blocking the communication bus, in this condition the measurement chain is powered off.

The functionality of the device and the measured acceleration data are selectable and accessible through the I²C or SPI interfaces. When using the I²C, CS must be tied high.

The functions, the threshold, and the timing of the two interrupt pins (INT 1 and INT 2) can be completely programmed by the user through the I²C/SPI interface.

## 5.1 Soldering information

The LGA package is compliant with the ECOPACK and RoHS standards.

It is qualified for soldering heat resistance according to JEDEC J-STD-020C.

Leave “pin 1 indicator” unconnected during soldering.

For land pattern and soldering recommendations, consult technical note TN0018 available on www.st.com.

# 6 Digital interfaces

The registers embedded inside the H3LIS331DL may be accessed through both the I²C and SPI serial interfaces. The latter may be software configured to operate either in 3-wire or 4-wire interface mode.

The serial interfaces are mapped to the same pins. To select/exploit the I²C interface, the CS line must be tied high (that is, connected to Vdd_IO).

**Table 7. Serial interface pin description**

| Pin name | Pin description |
|---|---|
| CS | Enables SPI<br>I²C/SPI mode selection (1: I²C mode; 0: SPI enabled) |
| SCL<br>SPC | I²C serial clock (SCL)<br>SPI serial port clock (SPC) |
| SDA<br>SDI<br>SDO | I²C serial data (SDA)<br>SPI serial data input (SDI)<br>3-wire interface serial data output (SDO) |
| SA0<br>SDO | I²C less significant bit of the device address (SA0)<br>SPI serial data output (SDO) |

## 6.1 I²C serial interface

The H3LIS331DL I²C is a bus slave. The I²C is employed to write data into registers whose content can also be read back.

The relevant I²C terminology is given in the table below.

**Table 8. I²C terminology**

| Term | Description |
|---|---|
| Transmitter | The device that sends data to the bus |
| Receiver | The device that receives data from the bus |
| Master | The device that initiates a transfer, generates clock signals, and terminates a transfer |
| Slave | The device addressed by the master |

There are two signals associated with the I²C bus: the serial clock line (SCL) and the serial data line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. Both the lines are connected to Vdd_IO through a pull-up resistor embedded inside the H3LIS331DL. When the bus is free both lines are high.

The I²C interface is compliant with fast mode (400 kHz) I²C standards as well as with normal mode.

### 6.1.1 I²C operation

The transaction on the bus is started through a start (ST) signal. A start condition is defined as a high to low transition on the data line while the SCL line is held high. After this has been transmitted by the master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the master.

The slave address (SAD) associated to the H3LIS331DL is 001100x. The **SDO**/**SA0** pin can be used to modify the less significant bit of the device address. If the SA0 pin is connected to the voltage supply, LSB is 1 (address 0011001) or else, if the SA0 pin is connected to ground, the LSB value is 0 (address 0011000). This solution allows the connection and addressing of two different accelerometers to the same I²C lines.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line low so that it remains stable low during the high period of the acknowledge clock pulse. A receiver that has been addressed is obliged to generate an acknowledge after each byte of data received.

The I²C embedded inside the H3LIS331DL behaves like a slave device and the following protocol must be adhered to. After the start condition (ST) a slave address is sent, once a slave acknowledge (SAK) has been returned, an 8-bit subaddress (SUB) is transmitted: the 7 LSB represent the actual register address while the MSB enables address auto increment. If the MSB of the SUB field is 1, the SUB (register address) is automatically increased to allow multiple data read/write.

The slave address is completed with a read/write bit. If the bit is 1 (read), a repeated start (SR) condition must be issued after the two subaddress bytes; if the bit is 0 (write), the master transmits to the slave with the direction unchanged. Table 10 explains how the SAD+read/write bit pattern is composed, listing all the possible configurations.

**Table 9. SAD+read/write patterns**

| Command | SAD[6:1] | SAD[0] = SA0 | R/W | SAD+R/W |
|---|---|---|---|---|
| Read | 001100 | 0 | 1 | 00110001 (31h) |
| Write | 001100 | 0 | 0 | 00110000 (30h) |
| Read | 001100 | 1 | 1 | 00110011 (33h) |
| Write | 001100 | 1 | 0 | 00110010 (32h) |

**Table 10. Transfer when master is writing one byte to slave**

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Master | ST | SAD + W | | SUB | | DATA | | SP |
| Slave | | | SAK | | SAK | | SAK | |

**Table 11. Transfer when master is writing multiple bytes to slave**

| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Master | ST | SAD + W | | SUB | | DATA | | DATA | | SP |
| Slave | | | SAK | | SAK | | SAK | | SAK | |

**Table 12. Transfer when master is receiving (reading) one byte of data from slave**

| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Master | ST | SAD + W | | SUB | | SR | SAD + R | | | NMAK | SP |
| Slave | | | SAK | | SAK | | | SAK | DATA | | |

**Table 13. Transfer when master is receiving (reading) multiple bytes of data from slave**

| | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Master | ST | SAD+ W | | SUB | | SR | SAD+ R | | | MAK | | MAK | | NMAK | SP |
| Slave | | | SAK | | SAK | | | SAK | DATA | | DATA | | DATA | | |

Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the most significant bit (MSB) first. If a slave receiver does not acknowledge the slave address (that is, it is not able to receive because it is performing some real-time function) the data line must be left high by the slave. The master can then abort the transfer. A low-to-high transition on the SDA line while the SCL line is high is defined as a stop condition. Each data transfer must be terminated by the generation of a stop (SP) condition.

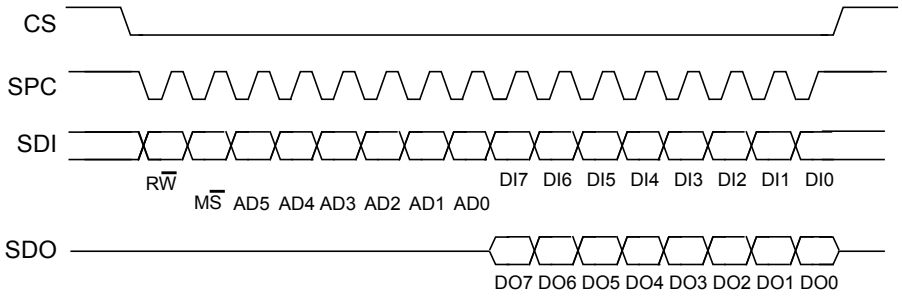
In order to read multiple bytes, it is necessary to assert the most significant bit of the subaddress field. In other words, SUB(7) must be equal to 1 while SUB(6-0) represents the address of the first register to be read.

In the presented communication format MAK is master acknowledge and NMAK is no master acknowledge.

## 6.2 SPI bus interface

The H3LIS331DL SPI is a bus slave. The SPI allows the writing and reading the device registers.
The serial interface interacts with the application using four wires: **CS**, **SPC**, **SDI**, and **SDO**.

**Figure 6. Read and write protocol**




**CS** enables the serial port and it is controlled by the SPI master. It goes low at the start of the transmission and goes back high at the end. **SPC** is the serial port clock and it is controlled by the SPI master. It is stopped high when **CS** is high (no transmission). **SDI** and **SDO** are respectively the serial port data input and output. Those lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**.

Both the read register and write register commands are completed in 16 clock pulses or in multiples of 8 in the case of multiple read/write bytes. Bit duration is the time between the two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of **SPC** after the falling edge of **CS** while the last bit (bit 15, bit 23, ...) starts at the last falling edge of **SPC** just before the rising edge of **CS**.

***bit 0***: R$\overline{W}$ bit. When 0, the data DI(7:0) is written into the device. When 1, the data DO(7:0) from the device is read. In the latter case, the chip drives **SDO** at the start of bit 8.

***bit 1***: M$\overline{S}$ bit. When 0, the address remains unchanged in multiple read/write commands. When 1, the address is auto-incremented in multiple read/write commands.

***bit 2-7***: address AD(5:0). This is the address field of the indexed register.

***bit 8-15***: data DI(7:0) (write mode). This is the data that is written into the device (MSB first).

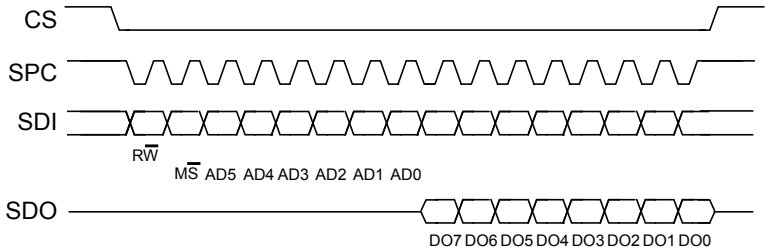
***bit 8-15***: data DO(7:0) (read mode). This is the data that is read from the device (MSB first).

In multiple read/write commands, further blocks of 8 clock periods are added. When the M$\overline{S}$ bit is 0, the address used to read/write data remains the same for every block. When the M$\overline{S}$ bit is 1 the address used to read/write data is increased at every block.

The function and the behavior of **SDI** and **SDO** remain unchanged.

### 6.2.1 SPI read

Figure 7. **SPI read protocol**




The SPI read command is performed with 16 clock pulses. A multiple byte read command is performed by adding blocks of 8 clock pulses to the previous one.

***bit 0***: READ bit. The value is 1.

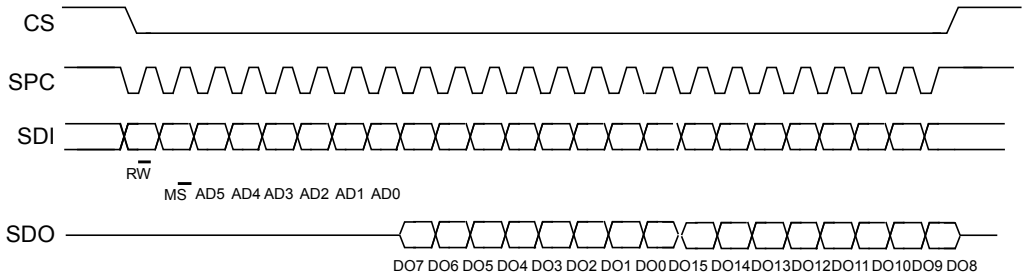
***bit 1***: MS bit. When 0, does not increment the address. When 1, increments the address in multiple reads.

***bit 2-7***: address AD(5:0). This is the address field of the indexed register.

***bit 8-15***: data DO(7:0) (read mode). This is the data that is read from the device (MSB first).

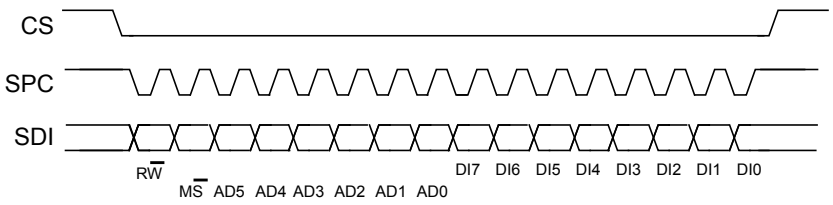
***bit 16-...*** : data DO(...-8). Further data in multiple byte reads.

Figure 8. **Multiple byte SPI read protocol (2-byte example)**



### 6.2.2 SPI write

Figure 9. **SPI write protocol**




The SPI write command is performed with 16 clock pulses. A multiple byte write command is performed by adding blocks of 8 clock pulses to the previous one.

***bit 0***: WRITE bit. The value is 0.

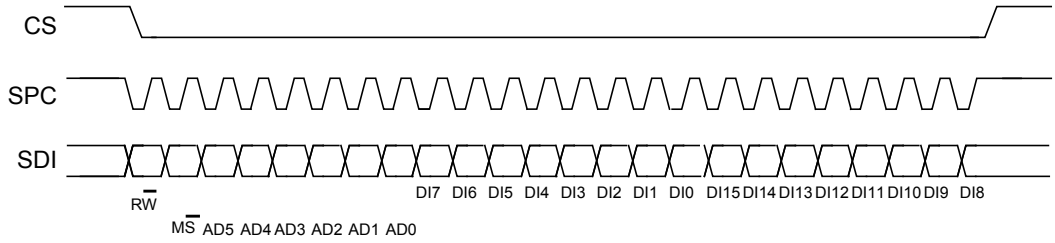
***bit 1***: MS bit. When 0, does not increment the address. When 1, increments the address in multiple writes.

***bit 2 -7***: address AD(5:0). This is the address field of the indexed register.

***bit 8-15***: data DI(7:0) (write mode). This is the data that is written inside the device (MSB first).

***bit 16-...***: data DI(...-8). Further data in multiple byte writes.

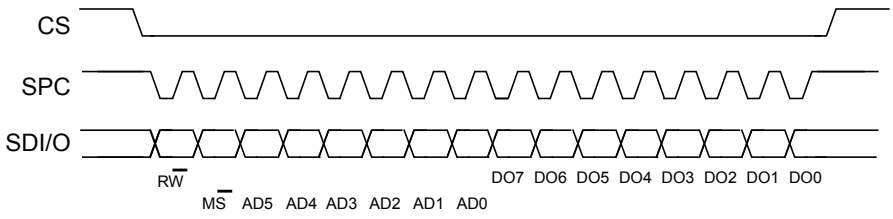
Figure 10. **Multiple byte SPI write protocol (2-byte example)**




### 6.2.3 SPI read in 3-wire mode

In order to enter 3-wire mode, set bit SIM (SPI serial interface mode selection) to 1 in CTRL_REG4 (23h).

Figure 11. **SPI read protocol in 3-wire mode**




The SPI read command is performed with 16 clock pulses:

***bit 0***: READ bit. The value is 1.

***bit 1***: MS bit. When 0, does not increment the address. When 1, increments the address in multiple reads.

***bit 2-7***: address AD(5:0). This is the address field of the indexed register.

***bit 8-15***: data DO(7:0) (read mode). This is the data that is read from the device (MSB first).

The multiple read command is also available in 3-wire mode.

# 7 Register mapping

The following table provides a list of the 8-bit registers embedded in the device and the corresponding addresses.

**Table 14. Register address map**

| Name | Type | Register address | | Default | Comment |
|---|---|---|---|---|---|
| | | Hex | Binary | | |
| Reserved (do not modify) | | 00 - 0E | | | Reserved |
| WHO_AM_I | R | 0F | 000 1111 | 00110010 | Dummy register |
| Reserved (do not modify) | | 10 - 1F | | | Reserved |
| CTRL_REG1 | R/W | 20 | 010 0000 | 00000111 | |
| CTRL_REG2 | R/W | 21 | 010 0001 | 00000000 | |
| CTRL_REG3 | R/W | 22 | 010 0010 | 00000000 | |
| CTRL_REG4 | R/W | 23 | 010 0011 | 00000000 | |
| CTRL_REG5 | R/W | 24 | 010 0100 | 00000000 | |
| HP_FILTER_RESET | R | 25 | 010 0101 | | Dummy register |
| REFERENCE | R/W | 26 | 010 0110 | 00000000 | |
| STATUS_REG | R | 27 | 010 0111 | 00000000 | |
| OUT_X_L | R | 28 | 010 1000 | Output | |
| OUT_X_H | R | 29 | 010 1001 | Output | |
| OUT_Y_L | R | 2A | 010 1010 | Output | |
| OUT_Y_H | R | 2B | 010 1011 | Output | |
| OUT_Z_L | R | 2C | 010 1100 | Output | |
| OUT_Z_H | R | 2D | 010 1101 | Output | |
| Reserved (do not modify) | | 2E - 2F | | | Reserved |
| INT1_CFG | R/W | 30 | 011 0000 | 00000000 | |
| INT1_SRC | R | 31 | 011 0001 | 00000000 | |
| INT1_THS | R/W | 32 | 011 0010 | 00000000 | |
| INT1_DURATION | R/W | 33 | 011 0011 | 00000000 | |
| INT2_CFG | R/W | 34 | 011 0100 | 00000000 | |
| INT2_SRC | R | 35 | 011 0101 | 00000000 | |
| INT2_THS | R/W | 36 | 011 0110 | 00000000 | |
| INT2_DURATION | R/W | 37 | 011 0111 | 00000000 | |
| Reserved (do not modify) | | 38 - 3F | | | Reserved |

Reserved registers must not be changed as they contain the factory calibration values. Their content is automatically restored when the device is powered up. Writing to those registers may change calibration data and thus lead to improper functioning of the device.

# 8 Register description

The device contains a set of registers that are used to control its behavior and to retrieve acceleration data. The register address, consisting of 7 bits, is used to identify them and to write the data over the serial interface.

## 8.1 WHO_AM_I (0Fh)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |

Device identification register

This register contains the device identifier that for the H3LIS331DL is set to 32h.

## 8.2 CTRL_REG1 (20h)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PM2 | PM1 | PM0 | DR1 | DR0 | Zen | Yen | Xen |

| | |
|---|---|
| PM[2:0] | Power mode selection. Default value: 000<br>(000: power-down; others: refer to Table 15) |
| DR[1:0] | Data rate selection. Default value: 00<br>(00: 50 Hz; others: refer Table 16) |
| Zen | Enables Z-axis. Default value: 1<br>(0: Z-axis disabled; 1: Z-axis enabled) |
| Yen | Enables Y-axis. Default value: 1<br>(0: Y-axis disabled; 1: Y-axis enabled) |
| Xen | Enables X-axis. Default value: 1<br>(0: X-axis disabled; 1: X-axis enabled) |

The **PM** bits allow the user to select between power-down and two operating active modes. The device is in power-down mode when the PD bits are set to 000 (default value after boot). Table 15 shows the power mode configurations and respective output data rates. Output data in low-power mode are computed with the low-pass filter cutoff frequency defined by the DR1, DR0 bits.

The **DR** bits, in normal mode operation, select the data rate at which acceleration samples are produced. In low-power modes they define the output data resolution. Table 16 shows the configurations for the DR1 and DR0 bits.

**Table 15. Power mode and low-power output data rate configurations**

| PM2 | PM1 | PM0 | Power mode selection | Output data rate [Hz] $ODR_{LP}$ |
|---|---|---|---|---|
| 0 | 0 | 0 | Power-down | -- |
| 0 | 0 | 1 | Normal mode | ODR |
| 0 | 1 | 0 | Low power | 0.5 |
| 0 | 1 | 1 | Low power | 1 |
| 1 | 0 | 0 | Low power | 2 |
| 1 | 0 | 1 | Low power | 5 |
| 1 | 1 | 0 | Low power | 10 |

Table 16. **Normal mode output data rate configurations and low-pass cutoff frequencies**

| DR1 | DR0 | Output data rate (ODR) [Hz] | Low-pass filter cutoff frequency [Hz] |
|---|---|---|---|
| 0 | 0 | 50 | 37 |
| 0 | 1 | 100 | 74 |
| 1 | 0 | 400 | 292 |
| 1 | 1 | 1000 | 780 |

## 8.3 CTRL_REG2 (21h)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| BOOT | HPM1 | HPM0 | FDS | HPen2 | HPen1 | HPCF1 | HPCF0 |

| | |
|---|---|
| BOOT | Reboot memory content. Default value: 0<br>(0: normal mode; 1: reboot memory content) |
| HPM[1:0] | High-pass filter mode selection. Default value: 00<br>(00: normal mode; others: refer to Table 17) |
| FDS | Filtered data selection. Default value: 0<br>(0: internal filter bypassed; 1: data from internal filter sent to output register) |
| HPen2 | High-pass filter enabled for interrupt 2 source. Default value: 0<br>(0: filter bypassed; 1: filter enabled) |
| HPen1 | High-pass filter enabled for interrupt 1 source. Default value: 0<br>(0: filter bypassed; 1: filter enabled) |
| HPCF[1:0] | High-pass filter cutoff frequency configuration. Default value: 00<br>(00: HPc=8; 01: HPc=16; 10: HPc=32; 11: HPc=64) |

The **BOOT** bit is used to refresh the content of the internal registers stored in the flash memory block. At device power-up, the content of the flash memory block is transferred to the internal registers related to trimming functions in order to permit correct operation of the device itself. If for any reason the content of the trimming registers is changed, it is sufficient to use this bit to restore the correct values. When the BOOT bit is set to 1, the content of the internal flash memory is copied inside the corresponding internal registers and it is used to calibrate the device. These values are factory trimmed and they are different for every accelerometer. They permit correct operation of the device and normally they do not have to be changed. At the end of the boot process, the BOOT bit is set again to 0.

Table 17. **High-pass filter mode configuration**

| HPM1 | HPM0 | High-pass filter mode |
|---|---|---|
| 0 | 0 | Normal mode (reset by reading HP_RESET_FILTER) |
| 0 | 1 | Reference signal for filtering |
| 1 | 0 | Normal mode (reset by reading HP_RESET_FILTER) |

**HPCF[1:0]**. These bits are used to configure the high-pass filter cutoff frequency $f_t$ which is given by:

$$f_t = \ln\left(1 - \frac{1}{HPc}\right) \cdot \frac{f_s}{2\pi}$$

The equation can be simplified to the following approximated equation:

$$f_t = \frac{f_S}{6 \cdot HPc}$$

**Table 18. High-pass filter cutoff frequency configuration**

| HPcoeff2,1 | $f_t$ [Hz] Data rate = 50 Hz | $f_t$ [Hz] Data rate = 100 Hz | $f_t$ [Hz] Data rate = 400 Hz | $f_t$ [Hz] Data rate = 1000 Hz |
|---|---|---|---|---|
| 00 | 1 | 2 | 8 | 20 |
| 01 | 0.5 | 1 | 4 | 10 |
| 10 | 0.25 | 0.5 | 2 | 5 |
| 11 | 0.125 | 0.25 | 1 | 2.5 |

## 8.4 CTRL_REG3 [interrupt CTRL register] (22h)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| IHL | PP_OD | LIR2 | I2_CFG1 | I2_CFG0 | LIR1 | I1_CFG1 | I1_CFG0 |

| | |
|---|---|
| IHL | Interrupt active high, low. Default value: 0<br>(0: active high; 1: active low) |
| PP_OD | Push-pull/open-drain selection on interrupt pin. Default value: 0<br>(0: push-pull; 1: open drain) |
| LIR2 | Latch interrupt request on INT2_SRC register, with INT2_SRC register cleared by reading INT2_SRC itself. Default value: 0<br>(0: interrupt request not latched; 1: interrupt request latched) |
| I2_CFG[1:0] | Data signal on INT 2 pin control bits (see Table 19). Default value: 00 |
| LIR1 | Latch interrupt request on the INT1_SRC register, with the INT1_SRC register cleared by reading the INT1_SRC register. Default value: 0<br>(0: interrupt request not latched; 1: interrupt request latched) |
| I1_CFG[1:0] | Data signal on INT 1 pin control bits (see Table 19). Default value: 00 |

**Table 19. Data signal on INT 1 and INT 2 pin**

| I1(2)_CFG1 | I1(2)_CFG0 | INT 1(2) pin |
|---|---|---|
| 0 | 0 | Interrupt 1 (2) source |
| 0 | 1 | Interrupt 1 source OR interrupt 2 source |
| 1 | 0 | Data ready |
| 1 | 1 | Boot running |

## 8.5 CTRL_REG4 (23h)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| BDU | BLE | FS1 | FS0 | 0 | 0 | 0 | SIM |

| | |
|---|---|
| BDU | Block data update. Default value: 0<br>(0: continuous update; 1: output registers not updated between read of MSB and LSB) |
| BLE | Big/little endian data selection. Default value: 0<br>(0: data LSB @ lower address; 1: data MSB @ lower address) |
| FS[1:0] | Full scale selection. Default value: 00<br>(00: ±100 *g*; 01: ±200 *g*; 11: ±400 *g*) |
| SIM | SPI serial interface mode selection. Default value: 0<br>(0: 4-wire interface; 1: 3-wire interface) |

The **BDU** bit is used to inhibit output register updates between the read of the upper and lower registers. In default mode (BDU = 0), the lower and upper registers are updated continuously. When the BDU is activated (BDU = 1), the content of the output registers is not updated until both MSB and LSB are read, which avoids reading values related to different sample times.

## 8.6 CTRL_REG5 (24h)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | TurnOn1 | TurnOn0 |

The **turn-on** bits are used for turning on the **sleep-to-wake** function.

| | |
|---|---|
| TurnOn[1:0] | Turn-on mode selection for sleep-to-wake function. Default value: 00 |

**Table 20. Sleep-to-wake configuration**

| TurnOn1 | TurnOn0 | Sleep-to-wake status |
|---|---|---|
| 0 | 0 | Sleep-to-wake function is disabled |
| 1 | 1 | Turned on: The device is in low-power mode (the ODR is defined in CTRL_REG1 (20h)) |

Setting the TurnOn[1:0] bits to 11, the sleep-to-wake function is enabled. When an interrupt event occurs, the device switches to normal mode, increasing the ODR to the value defined in CTRL_REG1 (20h). Although the device is in normal mode, the content of CTRL_REG1 (20h) is not automatically changed to the normal mode configuration.

## 8.7 HP_FILTER_RESET (25h)

Dummy register

Reading at this address zeroes instantaneously the content of the internal high-pass filter. If the high-pass filter is enabled, all three axes are instantaneously set to 0 *g*. This allows the settling time of the high-pass filter to be overcome.

## 8.8 REFERENCE (26h)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Ref7 | Ref6 | Ref5 | Ref4 | Ref3 | Ref2 | Ref1 | Ref0 |

| | |
|---|---|
| Ref[7:0] | Reference value for the high-pass filter. Default value: 00h |

This register sets the acceleration value taken as a reference for the high-pass filter output.

When the filter is turned on (at least one of the FDS, HPen2, or HPen1 bits is equal to 1) and the HPM bits are set to 01, a filter-out is generated, taking this value as a reference.

## 8.9 STATUS_REG (27h)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| ZYXOR | ZOR | YOR | XOR | ZYXDA | ZDA | YDA | XDA |

| | |
|---|---|
| ZYXOR | X, Y, and Z-axis data overrun. Default value: 0<br>(0: no overrun has occurred;<br>1: new data has overwritten the previous data before it was read) |
| ZOR | Z-axis data overrun. Default value: 0<br>(0: no overrun has occurred;<br>1: new data for the Z-axis has overwritten the previous data) |
| YOR | Y-axis data overrun. Default value: 0<br>(0: no overrun has occurred;<br>1: new data for the Y-axis has overwritten the previous data) |
| XOR | X-axis data overrun. Default value: 0<br>(0: no overrun has occurred;<br>1: new data for the X-axis has overwritten the previous data) |
| ZYXDA | X, Y and Z-axis new data available. Default value: 0<br>(0: a new set of data is not yet available; 1: a new set of data is available) |
| ZDA | Z-axis new data available. Default value: 0<br>(0: new data for the Z-axis is not yet available;<br>1: new data for the Z-axis is available) |
| YDA | Y-axis new data available. Default value: 0<br>(0: new data for the Y-axis is not yet available;<br>1: new data for the Y-axis is available) |
| XDA | X-axis new data available. Default value: 0<br>(0: new data for the X-axis is not yet available;<br>1: new data for the X-axis is available) |

## 8.10 OUT_X_L (28h), OUT_X_H (29h)

X-axis acceleration data. The value is expressed as two's complement.

## 8.11 OUT_Y_L (2Ah), OUT_Y_H (2Bh)

Y-axis acceleration data. The value is expressed as two's complement.

## 8.12 OUT_Z_L (2Ch), OUT_Z_H (2Dh)

Z-axis acceleration data. The value is expressed as two's complement.

## 8.13 INT1_CFG (30h)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| AOI | 0 | ZHIE | ZLIE | YHIE | YLIE | XHIE | XLIE |

| | |
|---|---|
| AOI | AND/OR combination of interrupt events (see Table 21). Default value: 0. |
| ZHIE | Enables interrupt generation on Z high event. Default value: 0<br>(0: disable interrupt request;<br>1: enable interrupt request on measured accel. value higher than preset threshold) |
| ZLIE | Enables interrupt generation on Z low event. Default value: 0<br>(0: disable interrupt request;<br>1: enable interrupt request on measured accel. value lower than preset threshold) |
| YHIE | Enables interrupt generation on Y high event. Default value: 0<br>(0: disable interrupt request;<br>1: enable interrupt request on measured accel. value higher than preset threshold) |
| YLIE | Enables interrupt generation on Y low event. Default value: 0<br>(0: disable interrupt request;<br>1: enable interrupt request on measured accel. value lower than preset threshold) |
| XHIE | Enables interrupt generation on X high event. Default value: 0<br>(0: disable interrupt request;<br>1: enable interrupt request on measured accel. value higher than preset threshold) |
| XLIE | Enables interrupt generation on X low event. Default value: 0<br>(0: disable interrupt request;<br>1: enable interrupt request on measured accel. value lower than preset threshold) |

Configuration register for interrupt 1 source

**Table 21. Interrupt 1 source configuration**

| AOI | Interrupt mode |
|---|---|
| 0 | OR combination of interrupt events |
| 1 | AND combination of interrupt events |

## 8.14 INT1_SRC (31h)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | IA | ZH | ZL | YH | YL | XH | XL |

| | |
|---|---|
| IA | Interrupt active. Default value: 0<br>(0: no interrupt has been generated; 1: one or more interrupts have been generated) |
| ZH | Z high. Default value: 0<br>(0: no interrupt, 1: Z high event has occurred) |
| ZL | Z low. Default value: 0<br>(0: no interrupt; 1: Z low event has occurred) |
| YH | Y high. Default value: 0<br>(0: no interrupt, 1: Y high event has occurred) |
| YL | Y low. Default value: 0<br>(0: no interrupt, 1: Y low event has occurred) |
| XH | X high. Default value: 0<br>(0: no interrupt, 1: X high event has occurred) |
| XL | X low. Default value: 0<br>(0: no interrupt, 1: X low event has occurred) |

Interrupt 1 source register. Read-only register.

Reading at this address clears the INT1_SRC IA bit (and the interrupt signal on the INT 1 pin) and allows the refresh of data in the INT1_SRC register if the latched option is chosen.

## 8.15 INT1_THS (32h)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | THS6 | THS5 | THS4 | THS3 | THS2 | THS1 | THS0 |

| | |
|---|---|
| THS[6:0] | Interrupt 1 threshold. Default value: 000 0000 |

## 8.16 INT1_DURATION (33h)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

| | |
|---|---|
| D[6:0] | Duration value. Default value: 000 0000 |

The **D6 - D0** bits set the minimum duration of the interrupt 2 event to be recognized. Duration steps and maximum values depend on the ODR chosen.

## 8.17 INT2_CFG (34h)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| AOI | 0 | ZHIE | ZLIE | YHIE | YLIE | XHIE | XLIE |

| | |
|---|---|
| AOI | AND/OR combination of interrupt events (see Table 22). Default value: 0 |
| ZHIE | Enable interrupt generation on Z high event. Default value: 0<br>(0: disable interrupt request;<br>1: enable interrupt request on measured accel. value higher than preset threshold) |
| ZLIE | Enable interrupt generation on Z low event. Default value: 0<br>(0: disable interrupt request;<br>1: enable interrupt request on measured accel. value lower than preset threshold) |
| YHIE | Enable interrupt generation on Y high event. Default value: 0<br>(0: disable interrupt request;<br>1: enable interrupt request on measured accel. value higher than preset threshold) |
| YLIE | Enable interrupt generation on Y low event. Default value: 0<br>(0: disable interrupt request;<br>1: enable interrupt request on measured accel. value lower than preset threshold) |
| XHIE | Enable interrupt generation on X high event. Default value: 0<br>(0: disable interrupt request;<br>1: enable interrupt request on measured accel. value higher than preset threshold) |
| XLIE | Enable interrupt generation on X low event. Default value: 0<br>(0: disable interrupt request;<br>1: enable interrupt request on measured accel. value lower than preset threshold) |

Configuration register for interrupt 2 source

**Table 22. Interrupt mode configuration**

| AOI | Interrupt mode |
|---|---|
| 0 | OR combination of interrupt events |
| 1 | AND combination of interrupt events |

## 8.18 INT2_SRC (35h)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | IA | ZH | ZL | YH | YL | XH | XL |

| | |
|---|---|
| IA | Interrupt active. Default value: 0<br>(0: no interrupt has been generated; 1: one or more interrupts have been generated) |
| ZH | Z high. Default value: 0<br>(0: no interrupt, 1: Z high event has occurred) |
| ZL | Z low. Default value: 0<br>(0: no interrupt; 1: Z low event has occurred) |
| YH | Y high. Default value: 0<br>(0: no interrupt, 1: Y high event has occurred) |
| YL | Y low. Default value: 0<br>(0: no interrupt, 1: Y low event has occurred) |
| XH | X high. Default value: 0<br>(0: no interrupt, 1: X high event has occurred) |
| XL | X low. Default value: 0<br>(0: no interrupt, 1: X low event has occurred) |

Interrupt 2 source register. Read-only register.

Reading at this address clears the INT2_SRC IA bit (and the interrupt signal on the INT 2 pin) and allows the refresh of data in the INT2_SRC register if the latched option is chosen.

## 8.19 INT2_THS (36h)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | THS6 | THS5 | THS4 | THS3 | THS2 | THS1 | THS0 |

| | |
|---|---|
| THS[6:0] | Interrupt 1 threshold. Default value: 000 0000 |

## 8.20 INT2_DURATION (37h)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

| | |
|---|---|
| D[6:0] | Duration value. Default value: 000 0000 |

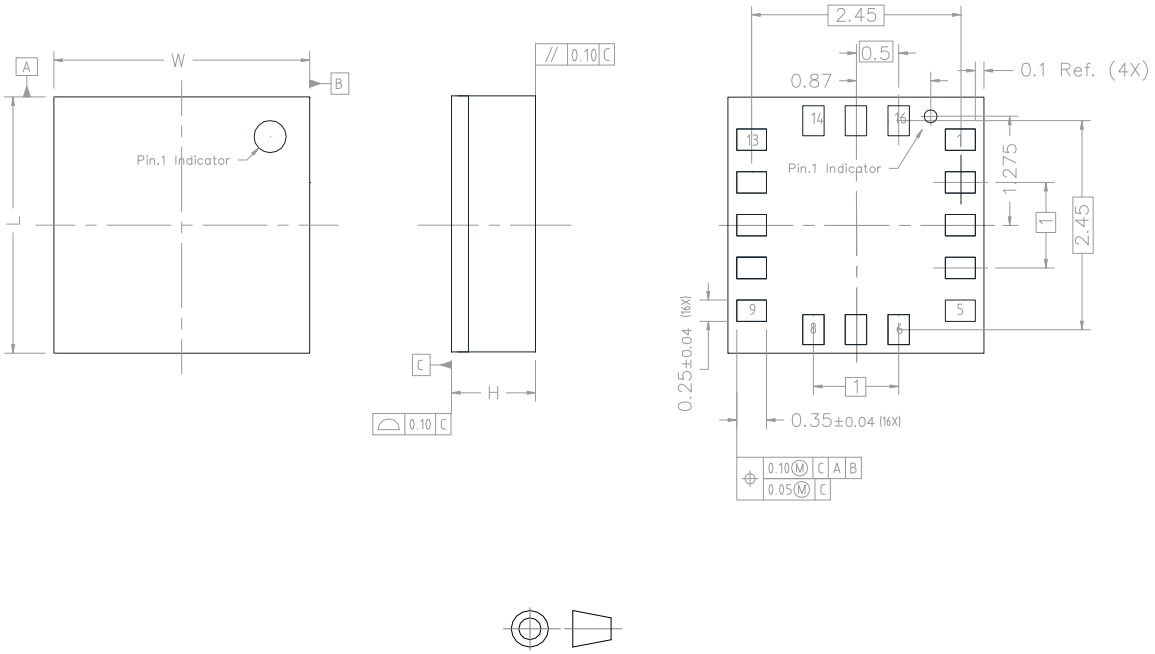
The **D6 - D0** bits set the minimum duration of the interrupt 2 event to be recognized. Duration time steps and maximum values depend on the ODR chosen.

# 9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

## 9.1 TLGA-16L package information

**Figure 12. TFLGA-16L 3 x 3 x 1.0 mm package outline and mechanical data**




Dimensions are in millimeter unless otherwise specified
General Tolerance is +/-0.1mm unless otherwise specified

**OUTER DIMENSIONS**

| ITEM | DIMENSION [mm] | TOLERANCE [mm] |
|---|---|---|
| Length [L] | 3 | ±0.15 |
| Width [W] | 3 | ±0.15 |
| Height [H] | 1 max | / |

7983231_13

## Revision history

Table 23. **Document revision history**

| Date | Version | Changes |
|---|---|---|
| 28-Oct-2022 | 4 | Updated Features, Applications, and Description<br>Updated Table 3. Electrical characteristics<br>Updated Table 6. Absolute maximum ratings<br>Updated Section 9.1 TLGA-16L package information<br>Minor textual changes |

# Contents

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