



STB75NF75L

N-channel 75V - 0.009Ω - 75A - D²PAK
STripFET™ II Power MOSFET

Features

| Type | V _{DSS} | R _{DS(on)} | I _D |
|------------|------------------|---------------------|----------------|
| STB75NF75L | 75V | <0.011Ω | 75A |

- Exceptional dv/dt capability
- 100% avalanche tested
- Low threshold drive

Description

This MOSFET series realized with STMicroelectronics unique STripFET process has specifically been designed to minimize input capacitance and gate charge. It is therefore suitable as primary switch in advanced high-efficiency, high-frequency isolated DC-DC converters for Telecom and Computer applications. It is also intended for any applications with low gate drive requirements.

Applications

- Switching applications

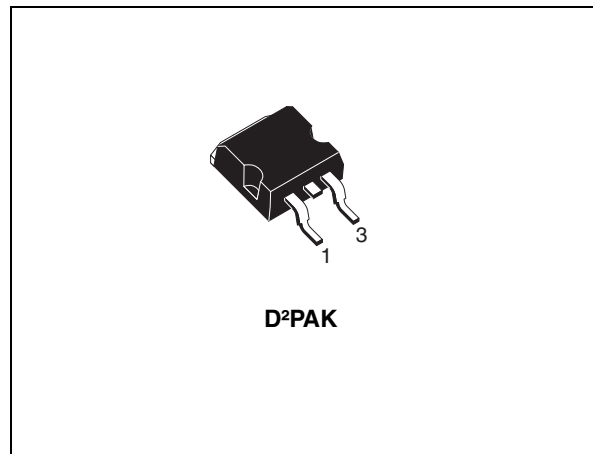


Figure 1. Internal schematic diagram

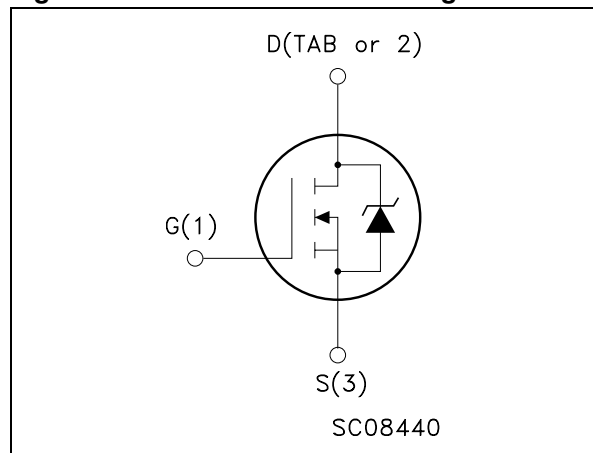


Table 1. Device summary

| Order code | Marking | Package | Packaging |
|--------------|----------|--------------------|-------------|
| STB75NF75LT4 | B75NF75L | D ² PAK | Tape & reel |

Contents

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1 Electrical ratings

Table 2. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|--------------------|---|------------|------|
| V_{DS} | Drain-source voltage ($V_{GS} = 0$) | 75 | V |
| V_{GS} | Gate-source voltage | ± 15 | V |
| $I_D^{(1)}$ | Drain current (continuous) at $T_C = 25^\circ\text{C}$ | 75 | A |
| I_D | Drain current (continuous) at $T_C = 100^\circ\text{C}$ | 70 | A |
| $I_{DM}^{(2)}$ | Drain current (pulsed) | 300 | A |
| P_{TOT} | Total dissipation at $T_C = 25^\circ\text{C}$ | 300 | W |
| | Derating factor | 2 | W/°C |
| $dv/dt^{(3)}$ | Peak diode recovery voltage slope | 10 | V/ns |
| $E_{AS}^{(4)}$ | Single pulse avalanche energy | 680 | mJ |
| T_J T_{stg} | Operating junction temperature Storage temperature | -55 to 175 | °C |

1. Current limited by package
2. Pulse width limited by safe operating area
3. $I_{SD} \leq 75\text{A}$, $di/dt \leq 500\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq T_{JMAX}$
4. Starting $T_J = 25^\circ\text{C}$, $I_D = 37.5\text{A}$, $V_{DD} = 30\text{V}$

Table 3. Thermal data

| Symbol | Parameter | Value | Unit |
|------------|--|-------|------|
| R_{thJC} | Thermal resistance junction-case Max | 0.5 | °C/W |
| R_{thJA} | Thermal resistance junction-ambient Max | 62.5 | °C/W |
| T_l | Maximum lead temperature for soldering purpose | 300 | °C |

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 4. On/off states

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|----------------------|---|---|------|----------------|----------------|----------|
| V _{(BR)DSS} | Drain-source breakdown voltage | I _D = 250µA, V _{GS} = 0 | 75 | | | V |
| I _{DSS} | Zero gate voltage drain current (V _{GS} = 0) | V _{DS} = Max rating, V _{DS} = Max rating @ 125°C | | | 1 10 | µA µA |
| I _{GSS} | Gate body leakage current (V _{DS} = 0) | V _{GS} = ±15V | | | ±100 | nA |
| V _{GS(th)} | Gate threshold voltage | V _{DS} = V _{GS} , I _D = 250µA | 1 | | 2.5 | V |
| R _{DS(on)} | Static drain-source on resistance | V _{GS} = 10V, I _D = 37.5A V _{GS} = 5V, I _D = 37.5A | | 0.009 0.010 | 0.011 0.013 | Ω Ω |

Table 5. Dynamic

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|--------------------------------|------------------------------|--|------|------|------|------|
| g _{fs} ⁽¹⁾ | Forward transconductance | V _{DS} = 15V, I _D = 37.5A | | 120 | | S |
| C _{iss} | Input capacitance | V _{DS} = 25V, f = 1 MHz, V _{GS} = 0 | | 4300 | | pF |
| C _{oss} | Output capacitance | | | 660 | | pF |
| C _{rss} | Reverse transfer capacitance | | | 205 | | pF |
| Q _g | Total gate charge | V _{DD} = 60V, I _D = 75A | | 75 | 90 | nC |
| Q _{gs} | Gate-source charge | V _{GS} = 5V | | 18 | | nC |
| Q _{gd} | Gate-drain charge | see Figure 15 | | 31 | | nC |

1. Pulsed: pulse duration=300µs, duty cycle 1.5%

Table 6. Switching times

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit | |
|---------------------|---------------------|--|------|------|------|------|----|
| t _{d(on)} | Turn-on delay time | V _{DD} = 40V, I _D = 37.5A, R _G = 4.7Ω, V _{GS} = 4.5V see Figure 14 | | 35 | | ns | |
| t _r | Rise time | | | 155 | | ns | |
| t _{d(off)} | Turn-off delay time | | | | 110 | | ns |
| t _f | Fall time | | | | 60 | | ns |
| | | | | | | | |

Table 7. Source drain diode

| Symbol | Parameter | Test conditions | Min | Typ. | Max | Unit |
|-----------------------------------|--|--|-----|-----------------|-----|---------------|
| I_{SD} | Source-drain current | | | | 75 | A |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) | | | | 300 | A |
| $V_{SD}^{(2)}$ | Forward on voltage | $I_{SD} = 75A, V_{GS} = 0$ | | | 1.3 | V |
| t_{rr} Q_{rr} I_{RRM} | Reverse recovery time Reverse recovery charge Reverse recovery current | $I_{SD} = 75A,$ $di/dt = 100A/\mu s,$ $V_{DD} = 24V, T_J = 150^\circ C$ see Figure 16 | | 120 500 9 | | ns nC A |

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

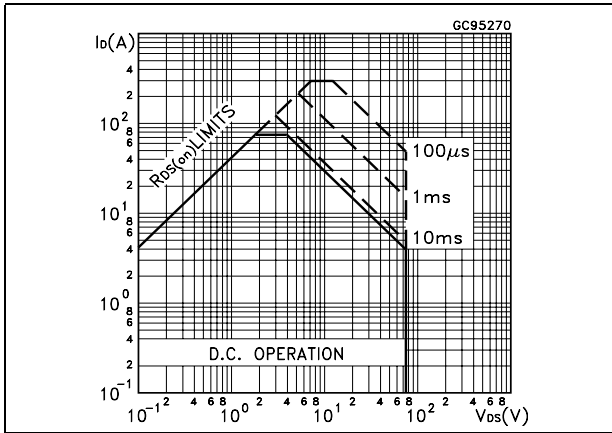


Figure 3. Thermal impedance

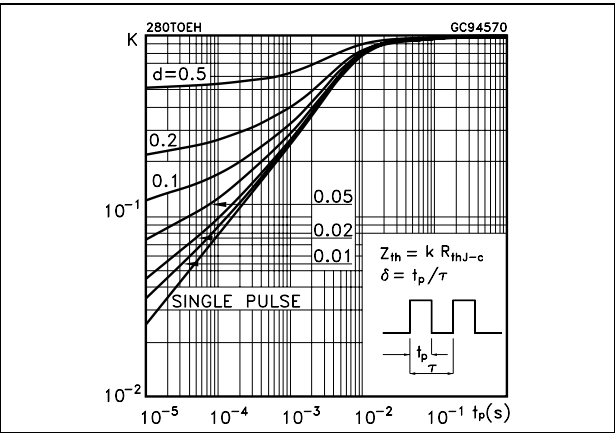


Figure 4. Output characteristics

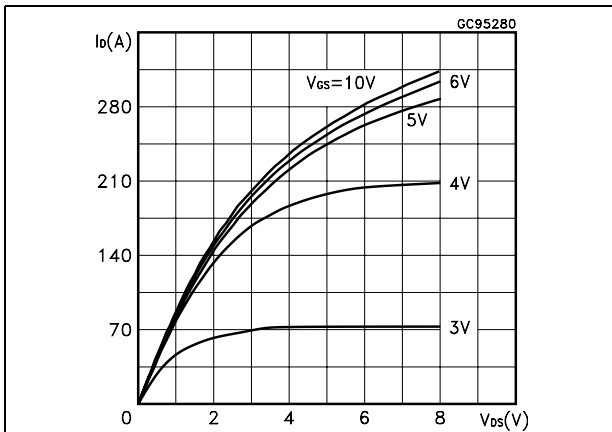


Figure 5. Transfer characteristics

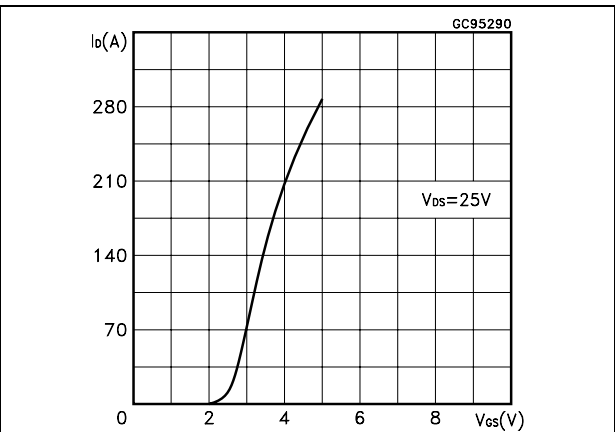


Figure 6. Transconductance

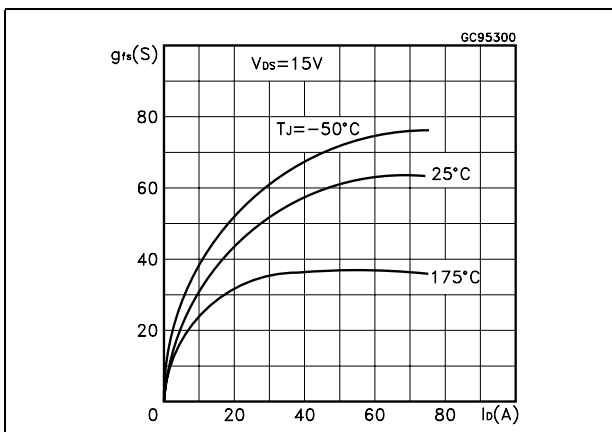


Figure 7. Static drain-source on resistance

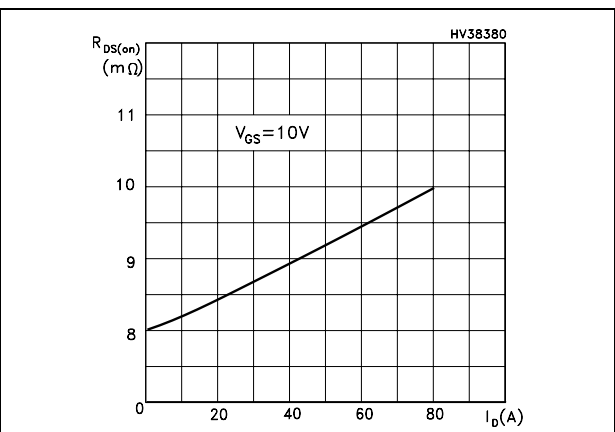


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

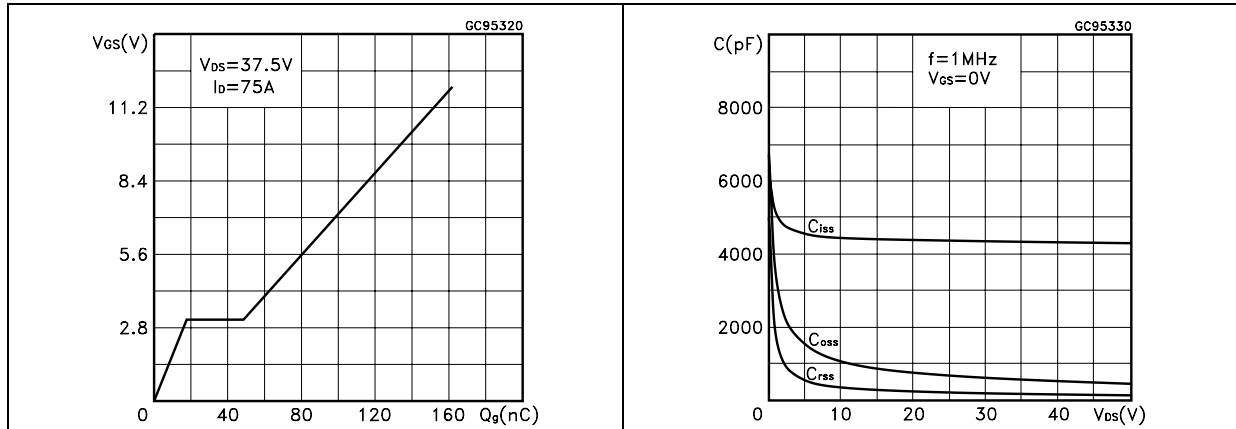


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on resistance vs temperature

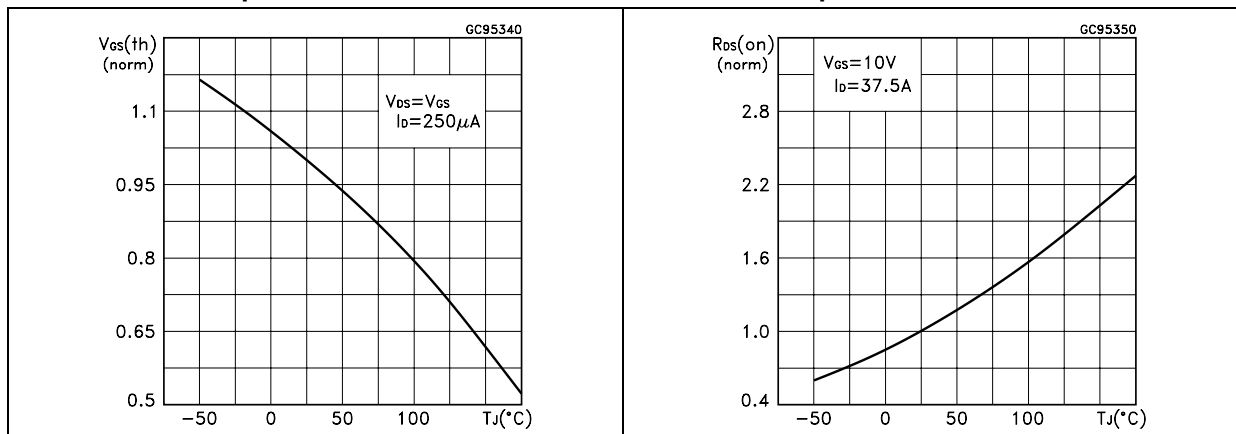
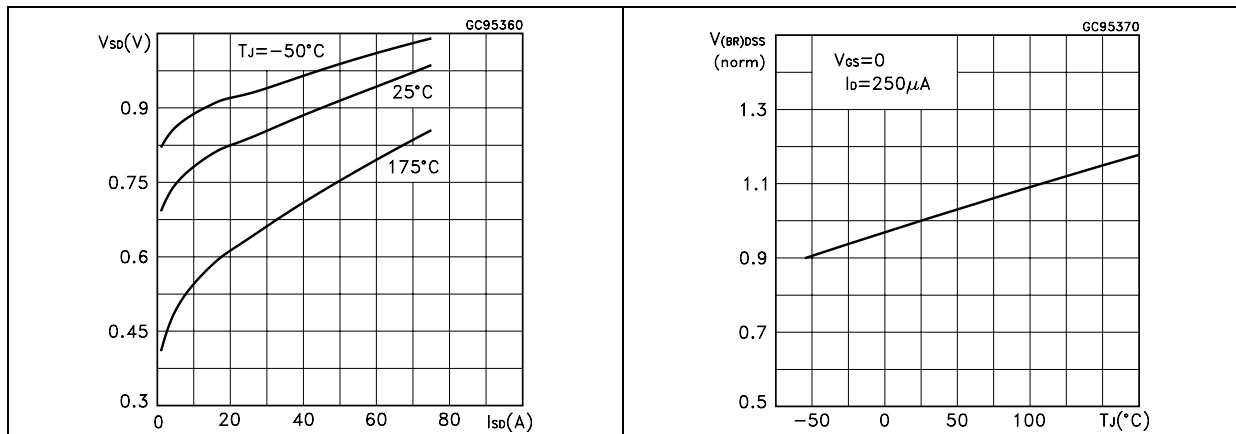


Figure 12. Source-drain diode forward characteristics Figure 13. Normalized $B_{V_{DS}}$ vs temperature



3 Test circuit

Figure 14. Switching times test circuit for resistive load

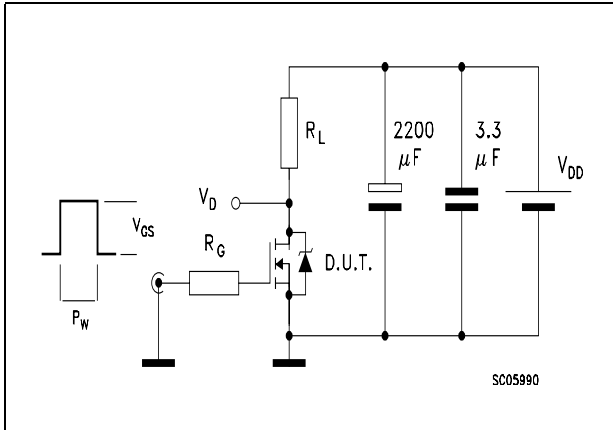


Figure 15. Gate charge test circuit

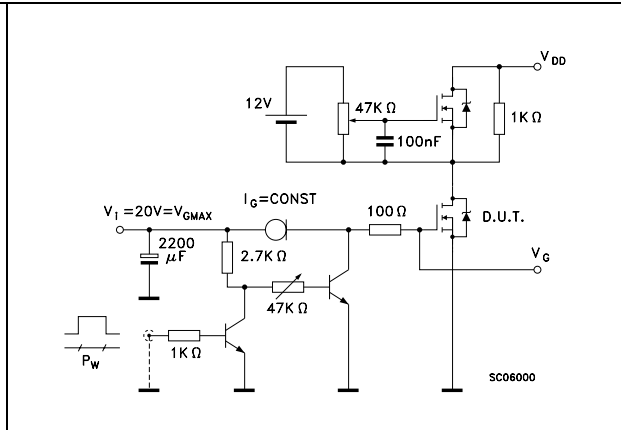


Figure 16. Test circuit for inductive load switching and diode recovery times

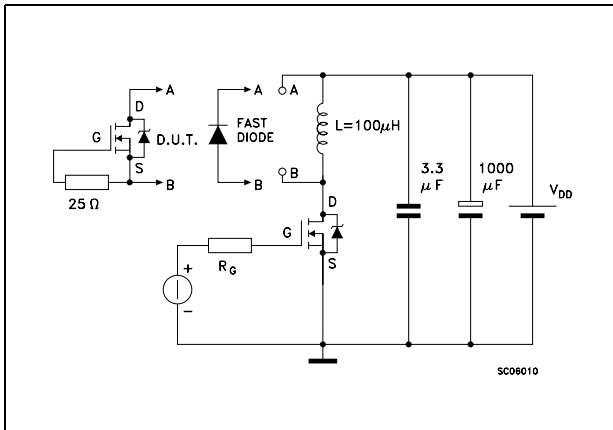


Figure 17. Unclamped Inductive load test circuit

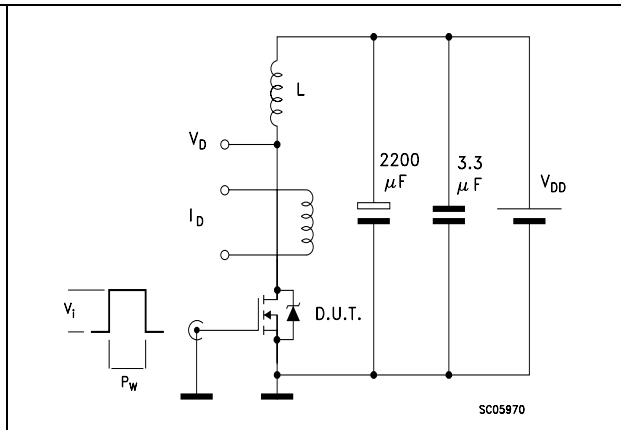
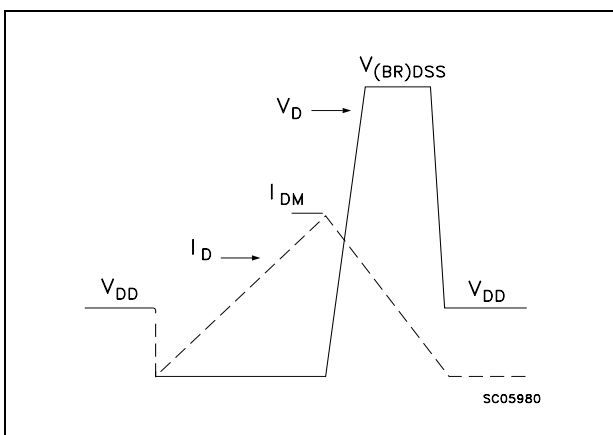


Figure 18. Unclamped inductive waveform

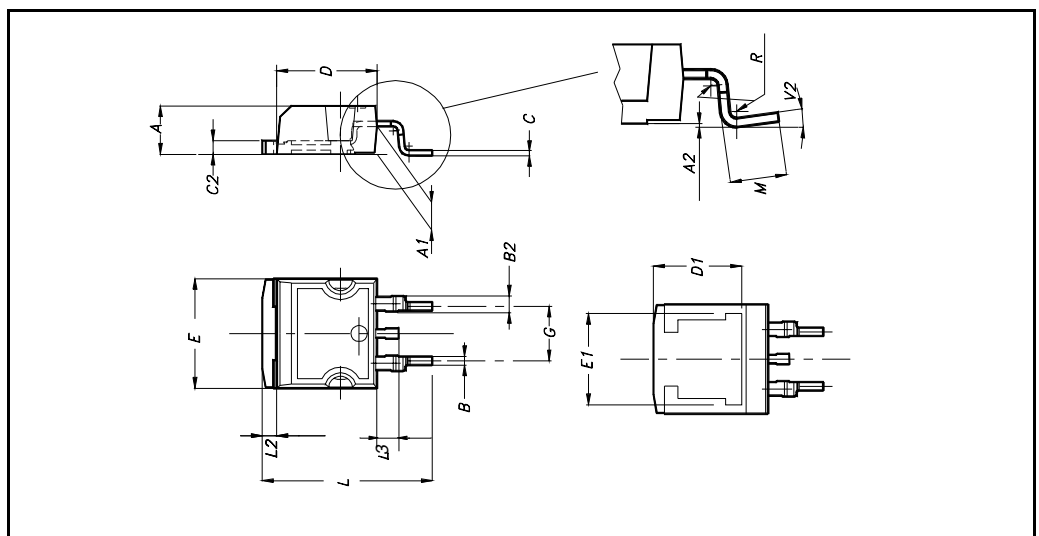


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

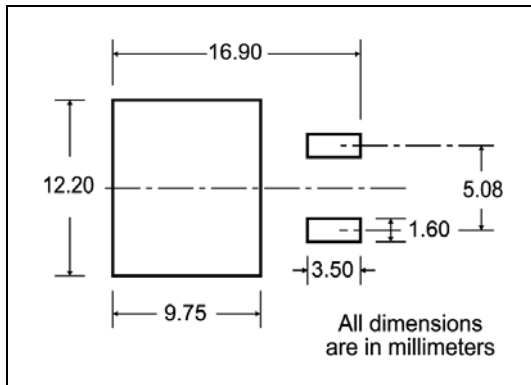
D²PAK MECHANICAL DATA

| DIM. | mm. | | | inch | | |
|------|------|-----|-------|-------|-------|-------|
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| A | 4.4 | | 4.6 | 0.173 | | 0.181 |
| A1 | 2.49 | | 2.69 | 0.098 | | 0.106 |
| A2 | 0.03 | | 0.23 | 0.001 | | 0.009 |
| B | 0.7 | | 0.93 | 0.027 | | 0.036 |
| B2 | 1.14 | | 1.7 | 0.044 | | 0.067 |
| C | 0.45 | | 0.6 | 0.017 | | 0.023 |
| C2 | 1.23 | | 1.36 | 0.048 | | 0.053 |
| D | 8.95 | | 9.35 | 0.352 | | 0.368 |
| D1 | | 8 | | | 0.315 | |
| E | 10 | | 10.4 | 0.393 | | |
| E1 | | 8.5 | | | 0.334 | |
| G | 4.88 | | 5.28 | 0.192 | | 0.208 |
| L | 15 | | 15.85 | 0.590 | | 0.625 |
| L2 | 1.27 | | 1.4 | 0.050 | | 0.055 |
| L3 | 1.4 | | 1.75 | 0.055 | | 0.068 |
| M | 2.4 | | 3.2 | 0.094 | | 0.126 |
| R | | 0.4 | | | 0.015 | |
| V2 | 0° | | 4° | | | |



5 Packaging mechanical data

D²PAK FOOTPRINT



TAPE AND REEL SHIPMENT

TAPE MECHANICAL DATA

| DIM. | mm | | inch | |
|------|------|------|--------|--------|
| | MIN. | MAX. | MIN. | MAX. |
| A0 | 10.5 | 10.7 | 0.413 | 0.421 |
| B0 | 15.7 | 15.9 | 0.618 | 0.626 |
| D | 1.5 | 1.6 | 0.059 | 0.063 |
| D1 | 1.59 | 1.61 | 0.062 | 0.063 |
| E | 1.65 | 1.85 | 0.065 | 0.073 |
| F | 11.4 | 11.6 | 0.449 | 0.456 |
| K0 | 4.8 | 5.0 | 0.189 | 0.197 |
| P0 | 3.9 | 4.1 | 0.153 | 0.161 |
| P1 | 11.9 | 12.1 | 0.468 | 0.476 |
| P2 | 1.9 | 2.1 | 0.075 | 0.082 |
| R | 50 | | 1.574 | |
| T | 0.25 | 0.35 | 0.0098 | 0.0137 |
| W | 23.7 | 24.3 | 0.933 | 0.956 |

REEL MECHANICAL DATA

| DIM. | mm | | inch | |
|------|------|------|-------|--------|
| | MIN. | MAX. | MIN. | MAX. |
| A | | 330 | | 12.992 |
| B | 1.5 | | 0.059 | |
| C | 12.8 | 13.2 | 0.504 | 0.520 |
| D | 20.2 | | 0.795 | |
| G | 24.4 | 26.4 | 0.960 | 1.039 |
| N | 100 | | 3.937 | |
| T | | 30.4 | | 1.197 |

| BASE QTY | BULK QTY |
|----------|----------|
| 1000 | 1000 |

* on sales type

6 Revision history

Table 8. Revision history

| Date | Revision | Changes |
|-------------|----------|--|
| 21-Jun-2004 | 1 | First release |
| 02-Oct-2006 | 2 | New template, no content change |
| 13-Jul-2007 | 3 | New updates on Table 7 |

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