

STD20NF06

General features

Туре	V _{DSS}	R _{DS(on)}	Ι _D
STD20NF06	60V	<0.040Ω	24A

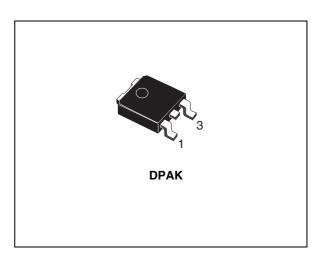
- Exceptional dv/dt capability
- Application oriented characterization
- 100% avalanche tested

Description

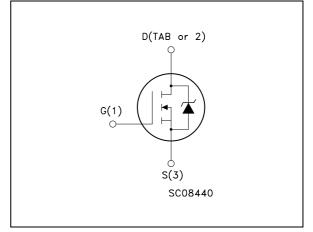
This Power MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

Applications

Switching application



Internal schematic diagram



Order code

Part number	Marking	Package	Packaging
STD20NF06T4	STD20NF06T4 D20NF06		Tape & reel

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Electrical ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	60	V
V _{DGR}	Drain-gate voltage ($R_{GS} = 20 \text{ k}\Omega$)	60	V
V _{GS}	Gate- source voltage	± 20	V
I _D	Drain current (continuous) at $T_C = 25^{\circ}C$	24	A
Ι _D	Drain current (continuous) at $T_C = 100^{\circ}C$	17	А
I _{DM} ⁽¹⁾	Drain current (pulsed)	96	A
P _{tot}	Total dissipation at $T_C = 25^{\circ}C$	60	W
	Derating Factor	0.4	W/°C
dv/dt ⁽²⁾	Peak diode recovery avalanche energy	10 V/r	
E _{AS} ⁽³⁾	Single pulse avalanche energy	300 mJ	
T _{stg}	Storage temperature	-55 to 175 °C	
Тj	Max. operating junction temperature	-55 10 175	°C

1. Pulse width limited by safe operating area.

2. I_{SD} 24A, di/dt $\leq 00A/\mu s$, $V_{DD} = V(_{BR)DSS}$, $T_j \leq T_{JMAX}$

3. Starting $T_j = 25 \text{ °C}$, $I_D = 10A$, $V_{DD} = 45V$

Rthj-case	Thermal resistance junction-case max	2.5	°C/W
Rthj-amb	Thermal resistance junction-to ambient max	100	°C/W
T _J Maximum lead temperature for soldering purpose ⁽¹⁾		275	°C

1. 1.6 mm from case, for 10 sec.



2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 250µA, V _{GS} =0	60			V
I _{DSS}	Zero gate voltage drain current (V _{GS} = 0)	V_{DS} = Max rating V_{DS} = Max rating, T_{C} = 125°C			1 10	μΑ μΑ
I _{GSS}	Gate-body leakage current (V _{DS} = 0)	$V_{GS} = \pm 20V$			±100	nA
V _{GS(th)}	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	2		4	V
R _{DS(on)}	Static drain-source on resistance	V _{GS} = 10V, I _D = 12A		0.032	0.040	Ω

Table 3. On/off states

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
9 _{fs} ⁽¹⁾	Forward transconductance	V _{DS} = 25V, I _D = 12A		15		S
C _{iss} C _{oss} C _{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V _{DS} = 25V, f = 1MHz, V _{GS} = 0		690 170 68		pF pF pF
t _{d(on)} t _r t _{d(off)} t _f	Turn-on delay time Rise time Turn-off delay time Fall time	$V_{DD} = 30V, I_D = 10A$ $R_G = 4.7\Omega V_{GS} = 10V$ (see <i>Figure 13</i>)		10 30 30 8		ns ns ns ns
Q _g Q _{gs} Q _{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 30V, I_D = 20A,$ $V_{GS} = 10V, R_G = 4.7\Omega$ (see <i>Figure 14</i>)		23 5 7.5	31	nC nC nC

1. Pulsed: Pulse duration = 300 μ s, duty cycle 1.5%.

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I _{SD} I _{SDM} ⁽¹⁾	Source-drain current Source-drain current (pulsed)				24 96	A A
V _{SD} ⁽²⁾	Forward on voltage	$I_{SD} = 24A, V_{GS} = 0$			1.5	V
t _{rr} Q _{rr} I _{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 20A, di/dt = 100A/\mu s,$ $V_{DD} = 30V, T_j = 150^{\circ}C$ (see <i>Figure 15</i>)		65 150 4.6		ns nC A

Table 5.Source drain diode

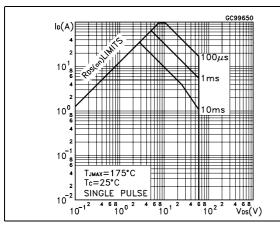
1. Pulse width limited by safe operating area.

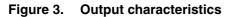
2. Pulsed: Pulse duration = 300 μ s, duty cycle 1.5%



2.1 Electrical characteristics (curves)

Figure 1. Safe operating area





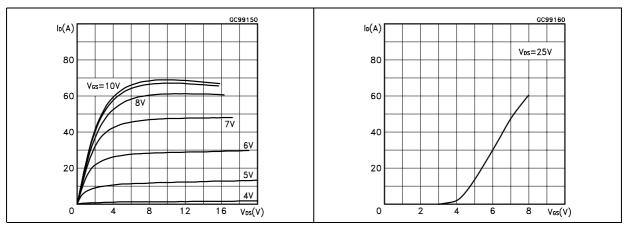


Figure 2.

d=0.5



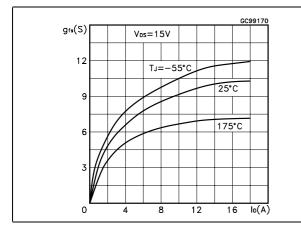


Figure 6. Static drain-source on resistance

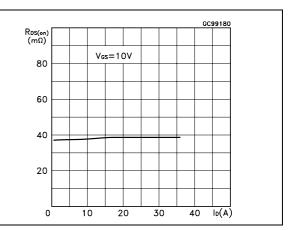
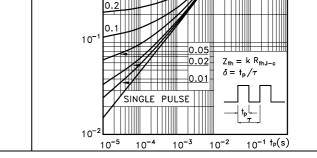
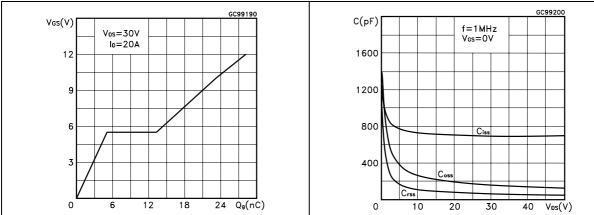




Figure 4. Transfer characteristics



Thermal impedance



Gate charge vs. gate-source voltage Figure 8. Figure 7. **Capacitance variations**

Figure 9. Normalized gate threshold voltage vs. temperature

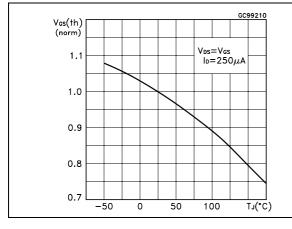


Figure 11. Source-drain diode forward characteristics

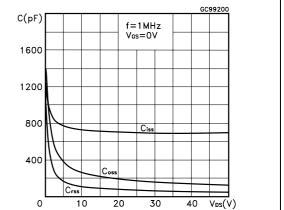


Figure 10. Normalized on resistance vs. temperature

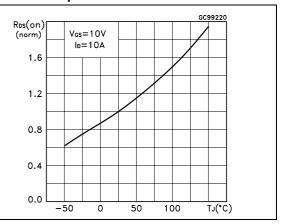
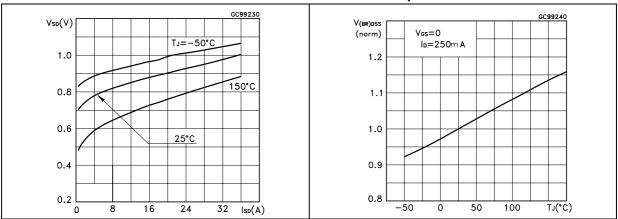


Figure 12. Normalized breakdown voltage vs. temperature



3 Test circuit

Figure 13. Switching times test circuit for resistive load

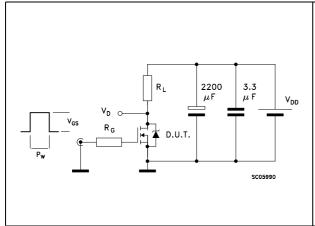
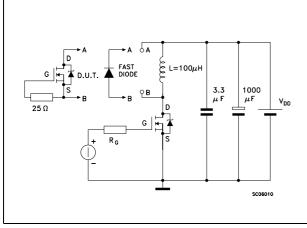


Figure 15. Test circuit for inductive load switching and diode recovery times





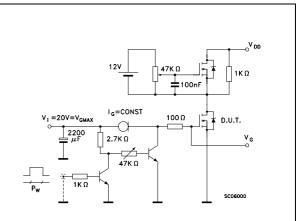
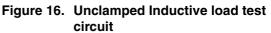


Figure 14. Gate charge test circuit



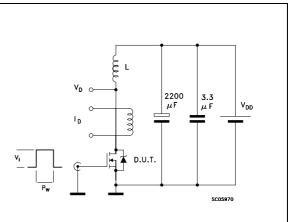
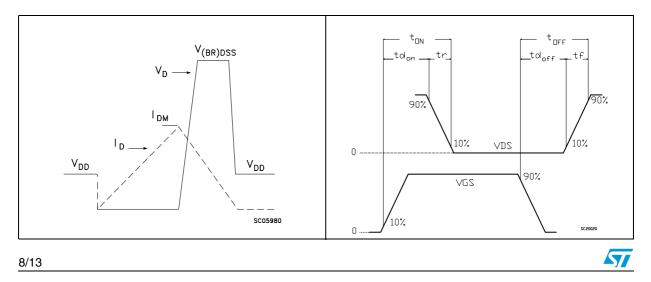


Figure 18. Switching time waveform



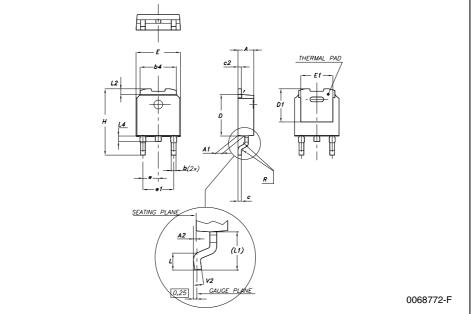
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com



DIM.		mm.			inch	
DIM.	MIN.	ТҮР	MAX.	MIN.	TYP.	MAX.
А	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
В	0.64		0.9	0.025		0.035
b4	5.2		5.4	0.204		0.212
С	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
D1		5.1			0.200	
E	6.4		6.6	0.252		0.260
E1		4.7			0.185	
е		2.28			0.090	
e1	4.4		4.6	0.173		0.181
Н	9.35		10.1	0.368		0.397
L	1			0.039		
(L1)		2.8			0.110	
L2		0.8			0.031	
L4	0.6		1	0.023		0.039
R		0.2			0.008	
V2	0°		8°	0°		8°

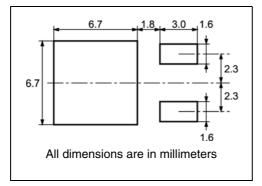


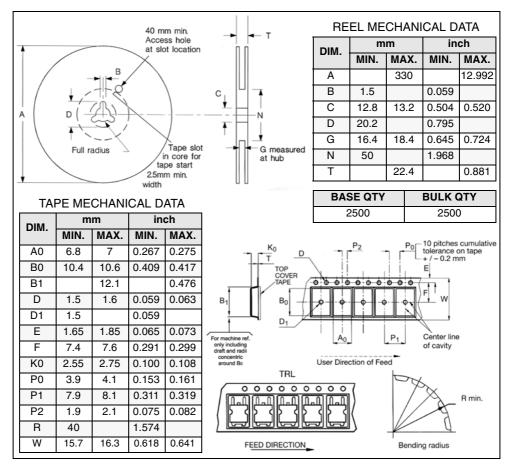




5 Packing mechanical data

DPAK FOOTPRINT





TAPE AND REEL SHIPMENT

6 Revision history

Table 6. Revision history

Date	Revision	Changes
22-Jun-2004	1	First release
16-Jul-2004	2	Change status from preliminary to definitive datasheet
09-Sep-2004	3	Typing error
03-Jul-2006	4	New template, no content change
20-Feb-2007	5	Typo mistake on page 1



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