



STF20NK50Z, STP20NK50Z

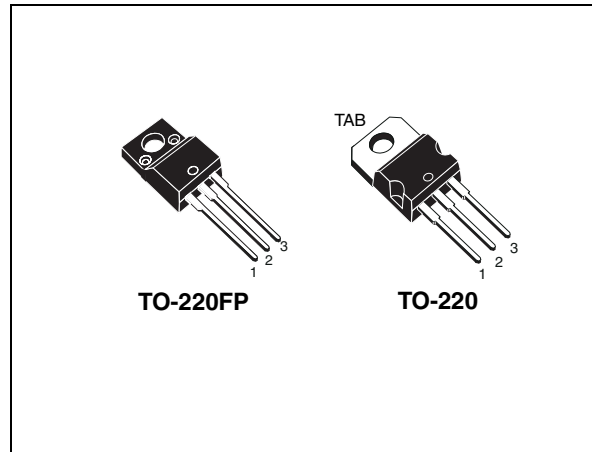
N-channel 500 V, 0.23 Ω , 17 A SuperMESH™ Power MOSFET
Zener-protected in TO-220FP and TO-220 packages

Datasheet — production data

Features

Order codes	V _{DSS}	R _{DS(on) max}	I _D	P _{TOT}
STF20NK50Z	500 V	< 0.27 Ω	17 A	40 W
STP20NK50Z	500 V	< 0.27 Ω	17 A	190 W

- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitance



Applications

- Switching applications

Description

These devices are N-channel Zener-protected Power MOSFETs developed using STMicroelectronics' SuperMESH™ technology, achieved through optimization of ST's well established strip-based PowerMESH™ layout. In addition to a significant reduction in on-resistance, this device is designed to ensure a high level of dv/dt capability for the most demanding applications.

Figure 1. Internal schematic diagram

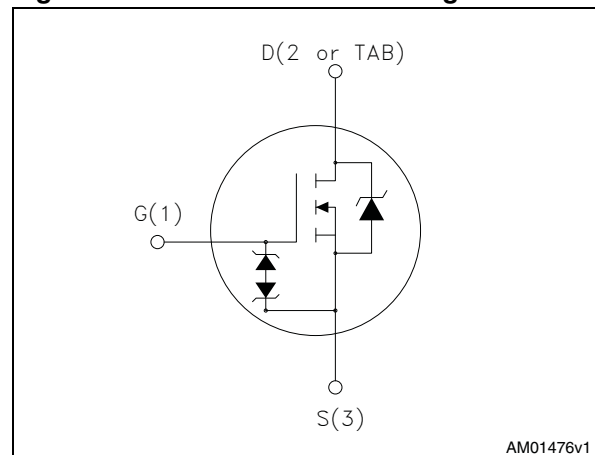


Table 1. Device summary

Order codes	Marking	Package	Packaging
STF20NK50Z	F20NK50Z	TO-220FP	Tube
STP20NK50Z	P20NK50Z	TO-220	

Contents

1	Electrical ratings	3
2	Electrical characteristics	4
	2.1 Electrical characteristics (curves)	6
3	Test circuits	9
4	Package mechanical data	10
5	Revision history	14

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220	TO-220FP	
V_{DS}	Drain-source voltage	500		V
V_{GS}	Gate-source voltage	± 30		V
I_D	Drain current (continuous) at $T_C = 25\text{ °C}$	17	17 ⁽¹⁾	A
I_D	Drain current (continuous) at $T_C = 100\text{ °C}$	10.71	10.71 ⁽¹⁾	A
$I_{DM}^{(2)}$	Drain current (pulsed)	68	68	A
P_{TOT}	Total dissipation at $T_C = 25\text{ °C}$	190	40	W
	Derating factor	1.52	0.32	W/°C
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink ($t = 1\text{ s}$; $T_C = 25\text{ °C}$)		2500	V
ESD	Gate-source human body model ($R=1.5\text{ k}\Omega$, $C=100\text{ pF}$)	6		kV
$dv/dt^{(3)}$	Peak diode recovery voltage slope	4.5		V/ns
T_{stg}	Storage temperature	-55 to 150		°C
T_j	Max operating junction temperature	150		°C

1. Limited by maximum junction temperature.

2. Pulse width limited by safe operating area.

3. $I_{SD} \leq 17\text{ A}$, $di/dt \leq 200\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$.

Table 3. Thermal data

Symbol	Parameter	Value		Unit
		TO-220	TO-220FP	
$R_{thj-case}$	Thermal resistance junction-case max	0.66	3.1	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient max	62.5	62.5	°C/W

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	17	A
E_{AS}	Single pulse avalanche energy (starting $T_J=25\text{ °C}$, $I_D=I_{AR}$, $V_{DD}=50\text{ V}$)	850	mJ

2 Electrical characteristics

($T_{CASE} = 25\text{ °C}$ unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0$	500			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 500\text{ V}$ $V_{DS} = 500\text{ V}$, $T_C = 125\text{ °C}$			1 50	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 100\text{ }\mu\text{A}$	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 8.5\text{ A}$		0.23	0.27	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$		2600		pF	
C_{oss}	Output capacitance		-	328		pF	
C_{rss}	Reverse transfer capacitance				72	pF	
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0$, $V_{DS} = 0$ to 640 V	-	187		pF	
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 250\text{ V}$, $I_D = 8.5\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 16)		28		ns	
t_r	Rise time			20		ns	
$t_{d(off)}$	Turn-off delay time				70		ns
t_f	Fall time				15		ns
Q_g	Total gate charge	$V_{DD} = 400\text{ V}$, $I_D = 17\text{ A}$, $V_{GS} = 10\text{ V}$ (see Figure 17)		85	119	nC	
Q_{gs}	Gate-source charge			15.5		nC	
Q_{gd}	Gate-drain charge			42		nC	

1. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		17	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		68	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 17 \text{ A}, V_{GS} = 0$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 17 \text{ A},$ $di/dt = 100 \text{ A}/\mu\text{s}$ $V_R = 100 \text{ V}$ (see Figure 18)	-	355		ns
Q_{rr}	Reverse recovery charge			3.90		μC
I_{RRM}	Reverse recovery current			22		A
t_{rr}	Reverse recovery time	$I_{SD} = 17 \text{ A},$ $di/dt = 100 \text{ A}/\mu\text{s}$ $V_R = 100 \text{ V}, T_j = 150 \text{ }^\circ\text{C}$ (see Figure 18)	-	440		ns
Q_{rr}	Reverse recovery charge			5.72		μC
I_{RRM}	Reverse recovery current			26		A

1. Pulsed: pulse duration=300 μs , duty cycle 1.5%

2. Pulse width limited by safe operating area

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
BV_{GSO}	Gate-source breakdown voltage	$I_{gs} = \pm 1 \text{ mA}$ (open drain)	30	-		V

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220

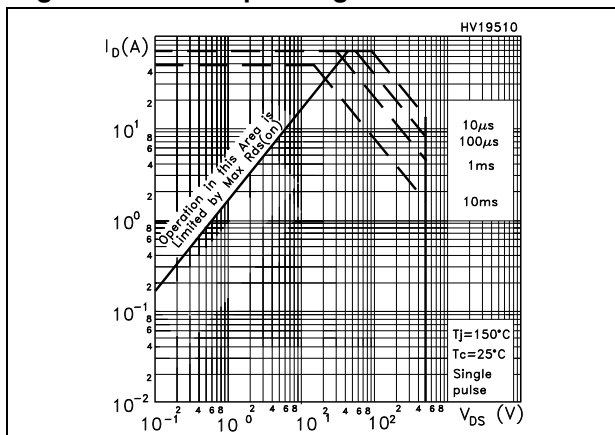


Figure 3. Thermal impedance for TO-220

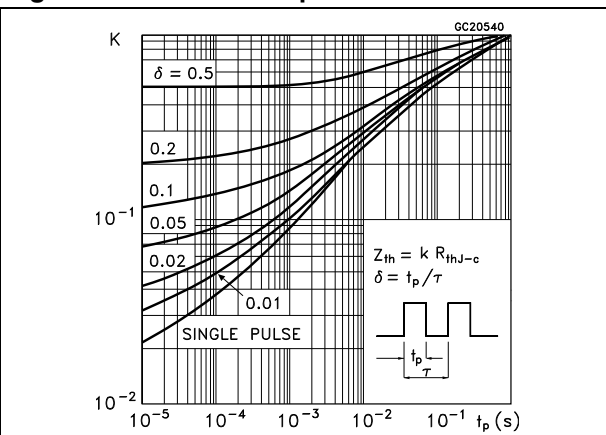


Figure 4. Safe operating area for TO-220FP

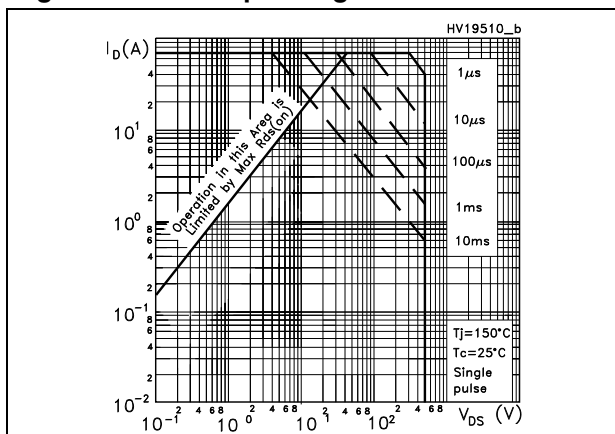


Figure 5. Thermal impedance for TO-220FP

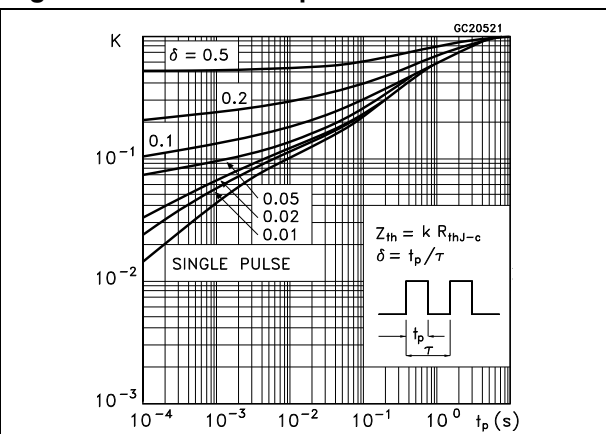


Figure 6. Output characteristics

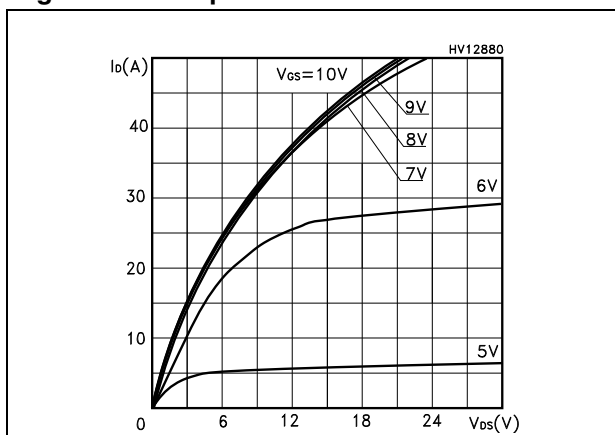


Figure 7. Transfer characteristics

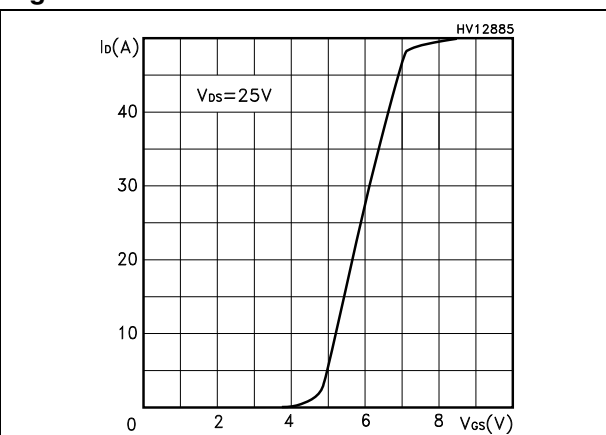


Figure 8. Normalized $B_{V_{DSS}}$ vs temperature

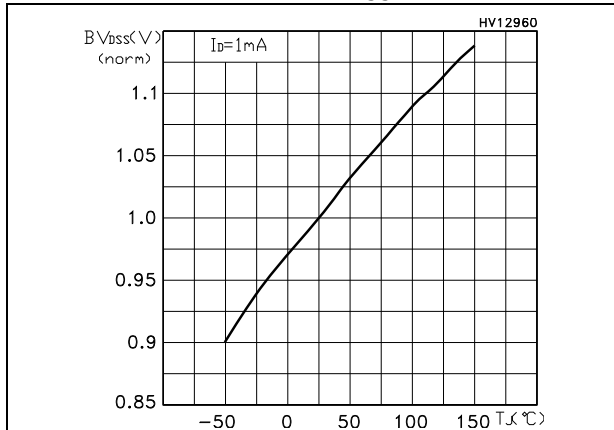


Figure 9. Static drain-source on-resistance

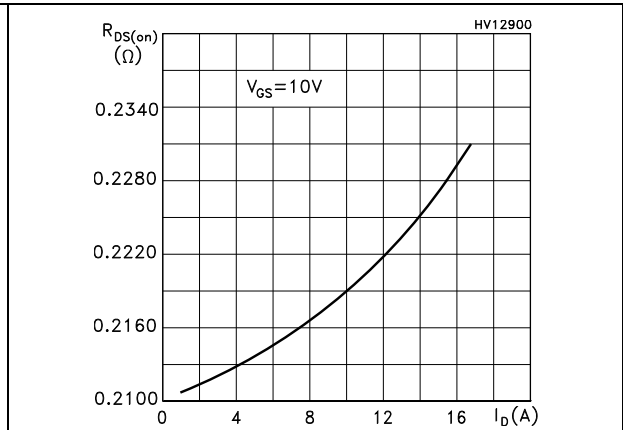


Figure 10. Gate charge vs gate-source voltage

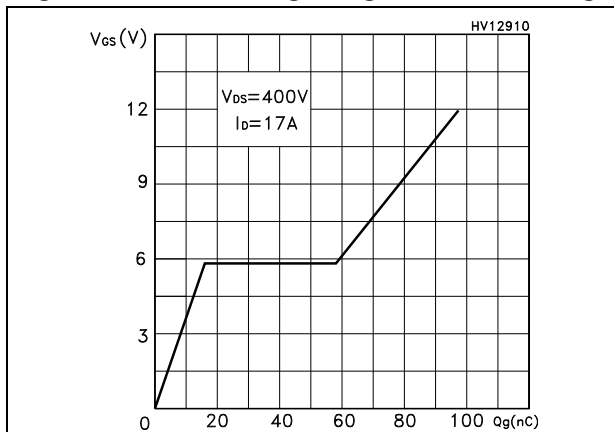


Figure 11. Capacitance variations

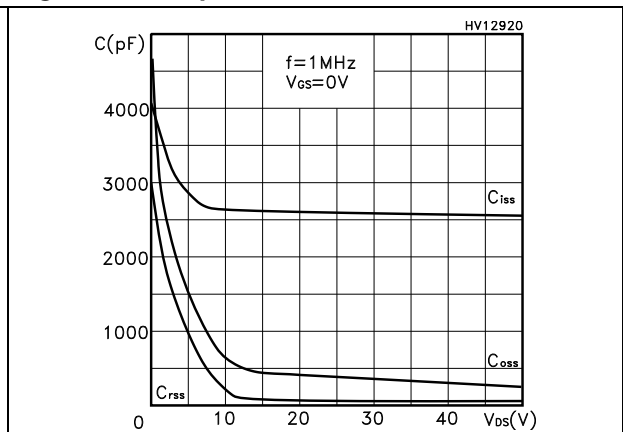


Figure 12. Normalized gate threshold voltage vs temperature

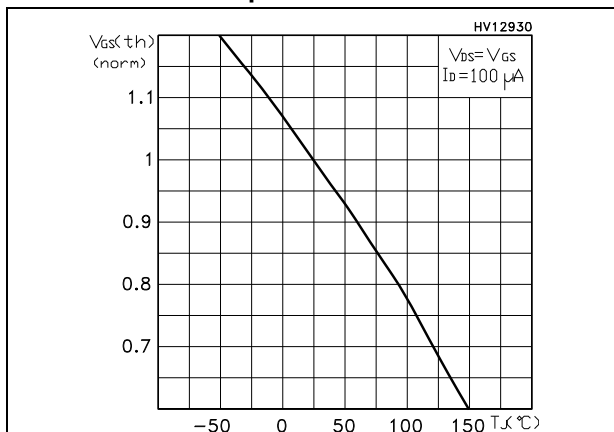


Figure 13. Normalized on-resistance vs temperature

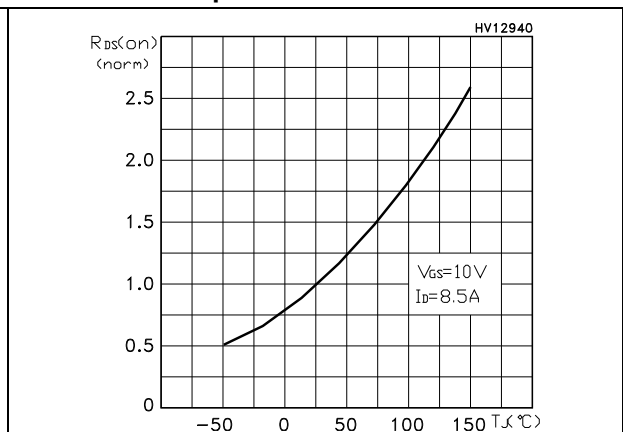


Figure 14. Maximum avalanche energy vs temperature

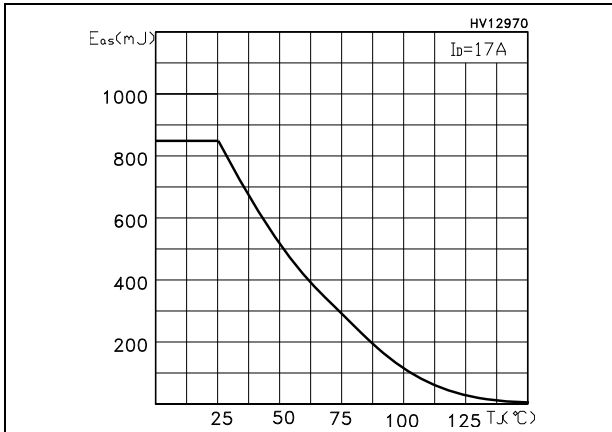
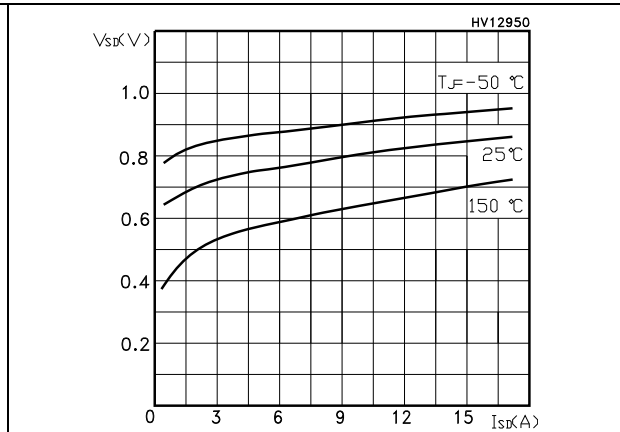


Figure 15. Source-drain diode forward characteristic



3 Test circuits

Figure 16. Switching times test circuit for resistive load



AM01468v1

Figure 17. Gate charge test circuit



AM01469v1

Figure 18. Test circuit for inductive load switching and diode recovery times



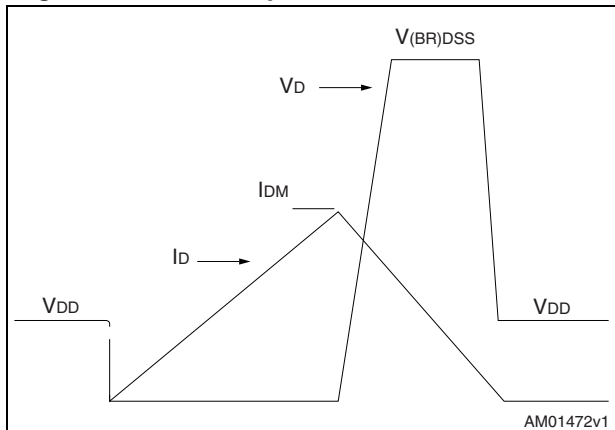
AM01470v1

Figure 19. Unclamped inductive load test circuit



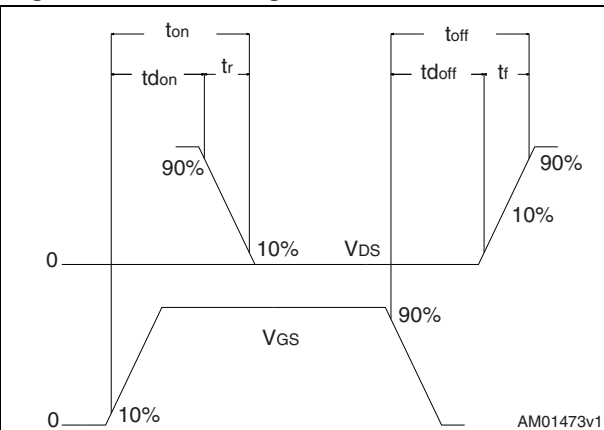
AM01471v1

Figure 20. Unclamped inductive waveform



AM01472v1

Figure 21. Switching time waveform



AM01473v1

4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 9. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Figure 22. TO-220FP drawing

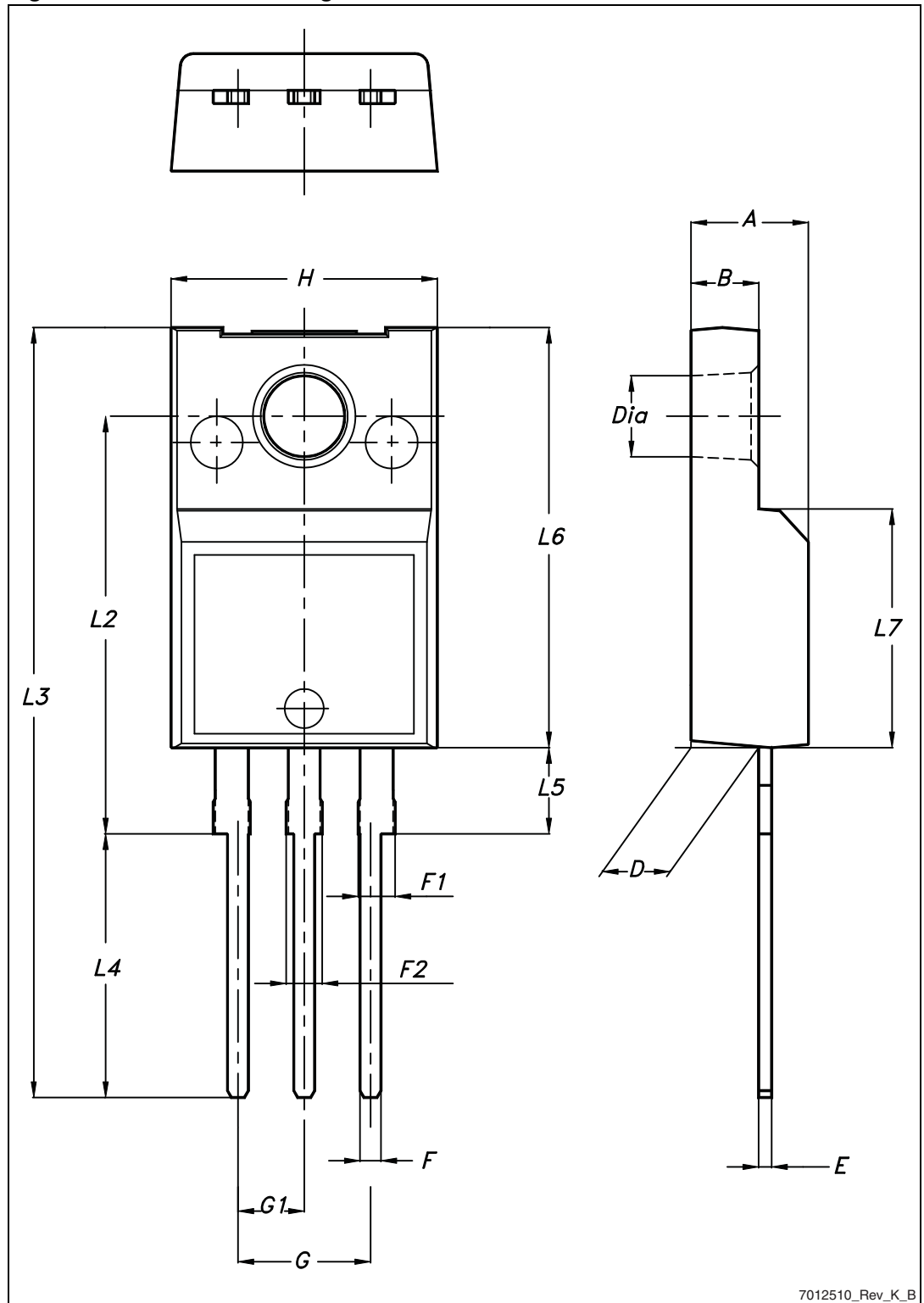
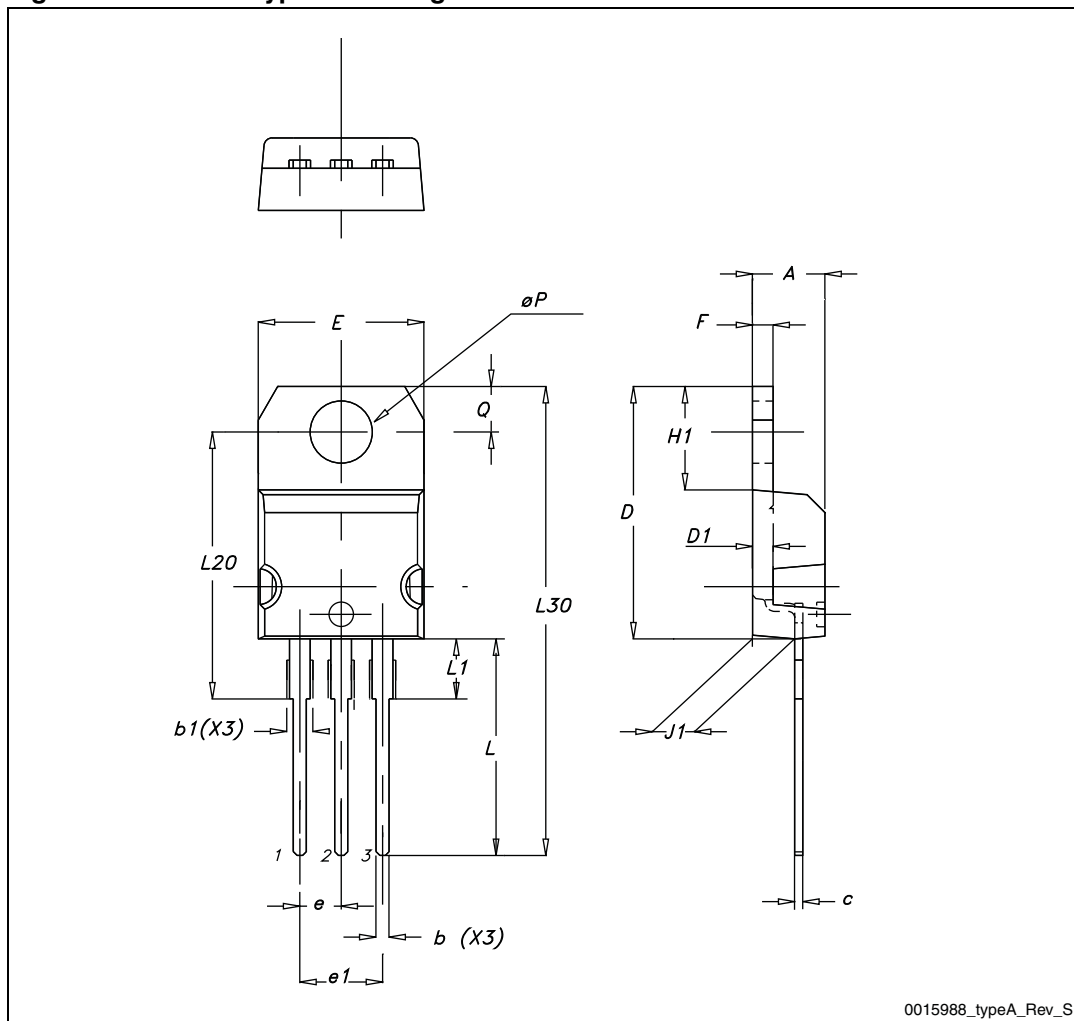


Table 10. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
ØP	3.75		3.85
Q	2.65		2.95

Figure 23. TO-220 type A drawing



5 Revision history

Table 11. Document revision history

Date	Revision	Changes
05-Apr-2012	1	First release.

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