

ESDA6V1-4BC6

QUAD BIDIRECTIONAL TRANSIL™ SUPPRESSOR FOR ESD PROTECTION

ASD™

MAIN APPLICATIONS

Where transient overvoltage protection in ESD sensitive equipment is required, such as:

- Computers
- Printers
- Communication systems
- Video equipment

This device is particularly adapted to the protection of symmetrical signals

FEATURES

- 4 Bidirectional Transil functions
- ESD Protection for data, Signal and V_{CC} Bus
- Stand off voltage range: 5 V
- Low leakage current
- Peak pulse power (8/20µs); 80W
- Channel separation: 80dB typ.@20KHz

DESCRIPTION

The ESDA6V1-4BC6 is a monolithic array designed to protect up to 4 lines in a bidirectional way against ESD transients.

The device is ideal for situations where board space is at a premium.

BENEFITS

- High ESD protection level
- High integration
- Suitable for high density boards

COMPLIES WITH THE FOLLOWING STANDARDS:

■ IEC61000-4-2 level 4:

15kV (air discharge) 8kV (contact discharge)

 MIL STD 883E-Method 3015-7: class3B (Human Body Model)

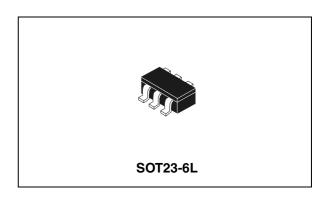
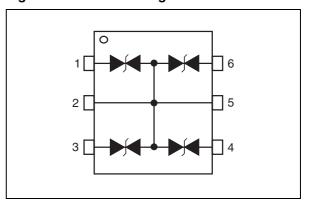


Table 1: Order Code

Part Number	Marking	
ESDA6V1-4BC6	BS77	

Figure 1: Functional Diagram



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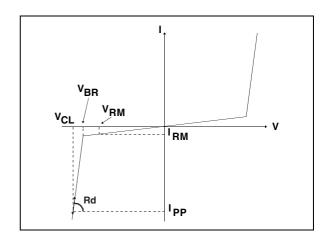
Table 2: Absolute Maximum Ratings $(T_{amb} = 25^{\circ}C)$

Symbol	P	Value	Unit	
V _{PP}	ESD discharge	MIL STD 883C - Method 3015-6 IEC61000-4-2 air discharge IEC61000-4-2 contact discharge	25 15 8	kV
P _{PP}	Peak pulse power (8/20µs)	80	W	
Tj	Junction temperature	150	°C	
T _{stg}	Storage temperature range	-55 to +150	°C	
TL	Maximum lead temperature for case	260	°C	
T _{op}	Operating temperature range	-40 to +125	°C	

Note 1: Variation of parameters is given by curves.

Table 3: Electrical Characteristics $(T_{amb} = 25^{\circ}C)$

Symbol	Parameter
V _{RM}	Stand-off voltage
V_{BR}	Breakdown voltage
V _{CL}	Clamping voltage
I _{RM}	Leakage current
I _{PP}	Peak pulse current
αΤ	Voltage temperature coefficient
V _F	Forward voltage drop
С	Capacitance
R _d	Dynamic resistance



	/	/ _{BR} @	I _R	I _{RM} @	V _{RM}	R_d	αΤ	С
Type	min.	max.		max.		typ.	max.	typ.
Туре						note 2		0V bias
	V	V	mA	μΑ	V	Ω	10 ⁻⁴ /°C	pF
ESDA6V1-4BC6	6.1	8	1	1	3	0.45	3	45

Note 2: Square pulse, Ipp = 3A, t_p =2.5 μ s.

Figure 2: Relative variation of peak pulse power versus initial junction temperature

 $P_{PP}[T_j \text{ initial}] / P_{PP}[T_j \text{ initial=25°C}]$ 1.0 0.9 0.8 0.7 0.6 0.5 0.4 0.3 0.2 0.1 $T_j(^{\circ}C)$ 0.0 25 50 75 100 125

Figure 3: Peak pulse power versus exponential pulse duration

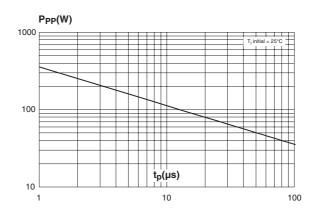


Figure 4: Clamping voltage versus peak pulse current (typical values, rectangular waveform)

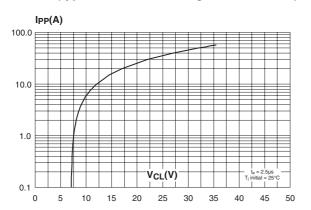
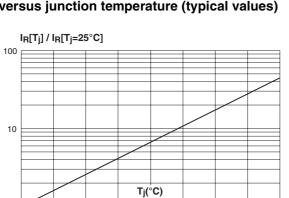


Figure 6: Relative variation of leakage current versus junction temperature (typical values)



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Figure 5: Junction capacitance versus line voltage applied (typical values

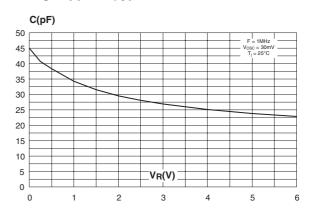
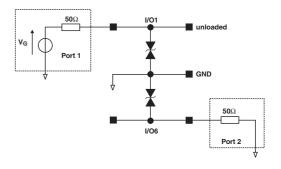


Figure 7: Analog crosstalk test configuration



1. ESD protection by ESDA6V1-4BC6

With the focus of lowering the operation levels, the problem of malfunction caused by the environment is critical. Electrostatic discharge (ESD) is a major cause of failure in electronic system.

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Transient Voltage Suppressors are an ideal choice for ESD protection and have proven capable in suppressing ESD events. They are capable of clamping the incoming transient to a low enough level such that damage to the protected semiconductor is prevented.

Surface mount TVS arrays offer the best choice for minimal lead inductance.

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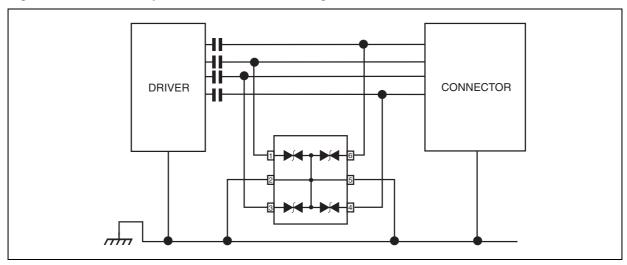
They serve as parallel protection elements, connected between the signal line to ground. As the transient rises above the operating voltage of the device, the TVS array becomes a low impedance path diverting the transient current to ground.

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Figure 8: Bidirectional protection for 0V biased signals



The ESDA6V1-4BC6 array is the ideal product for use as board level protection of ESD sensitive semiconductor components.

The tiny SOT23-6L package allows design flexibility in the design of "crowded" boards where the space saving is at a premium. This enables to shorten the routing and can contribute to improve ESD performance.

2. Circuit Board Layout

Circuit board layout is a critical design step in the suppression of ESD induced transients. The following guidelines are recommended:

- The ESDA6V1-4BC6 should be placed as near as possible to the input terminals or connectors.
- Minimise the path length between the ESD suppressor and the protected device
- Minimise all conductive loops, including power and ground loops
- The ESD transient return path to ground should be kept as short as possible.
- Use ground planes whenever possible.

Figure 9: Ordering information scheme

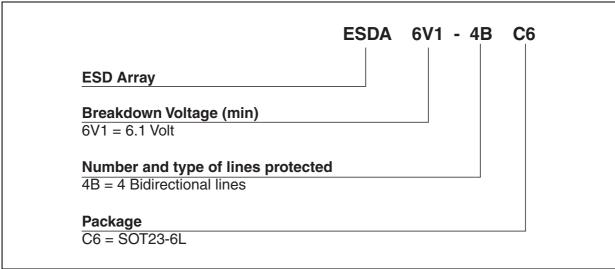
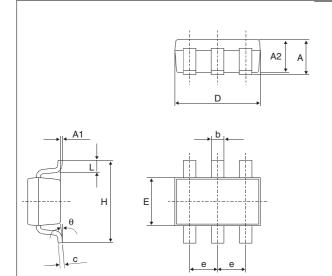


Figure 10: SOT23-6L Package Mechanical Data



			DIMENSIONS				
REF.	Mi	llimete	rs I		Inches		
	Min.	Тур.	Max.	Min.	Тур.	Max.	
Α	0.90		1.45	0.035		0.057	
A1	0		0.10	0		0.004	
A2	0.90		1.30	0.035		0.051	
b	0.35		0.50	0.014		0.02	
С	0.09		0.20	0.004		0.008	
D	2.80		3.05	0.110		0.120	
Е	1.50		1.75	0.059		0.069	
е		0.95			0.037		
Н	2.60		3.00	0.102		0.118	
L	0.10		0.60	0.004		0.024	
θ			10°			10°	

Figure 11: Foot Print Dimensions (in millimeters)

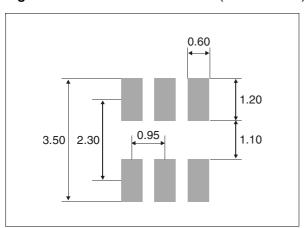


Table 4: Ordering Information

Part Number	Marking	Package	Weight	Base qty	Delivery mode
ESDA6V1-4BC6	BS77	SOT23-6L	16.7 mg	3000	Tape & reel

Table 5: Revision History

Date	Revision	Description of Changes
Nov-2002	1A	First issue.
4-Nov-2004	2	SOT23-6L package dimensions change for reference "D" from 3.0 millimeters (0.118 inches) to 3.05 millimeters (0.120 inches).

5//.

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