

STF24N60DM2

N-channel 600 V, 0.175 Ω typ., 18 A MDmesh™ DM2 Power MOSFET in a TO-220FP package

Datasheet - production data

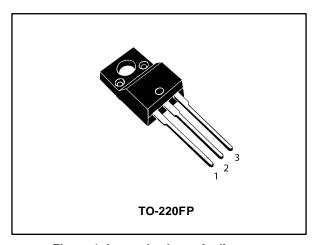
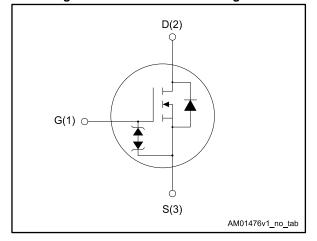


Figure 1: Internal schematic diagram



Features

Order code V _{DS} @ T _{Jmax}		R _{DS(on)} max.	ΙD
STF24N60DM2	650 V	0.200 Ω	18 A

- Fast-recovery body diode
- Extremely low gate charge and input capacitance
- Low on-resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected

Applications

Switching applications

Description

This high voltage N-channel Power MOSFET is part of the MDmesh $^{\text{TM}}$ DM2 fast recovery diode series. It offers very low recovery charge (Q_{rr}) and time (t_{rr}) combined with low R_{DS(on)}, rendering it suitable for the most demanding high efficiency converters and ideal for bridge topologies and ZVS phase-shift converters.

Table 1: Device summary

Order code	Marking	Package	Packing
STF24N60DM2	24N60DM2	TO-220FP	Tube

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STF24N60DM2 Electrical ratings

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _G s	Gate-source voltage	± 25	V
Ip ⁽¹⁾	Drain current (continuous) at T _C = 25 °C	18	Λ
ID(*/	Drain current (continuous) at T _C = 100 °C	11	Α
I _{DM} ⁽²⁾⁽¹⁾	Drain current (pulsed)	72	Α
P _{TOT}	Total dissipation at T _C = 25 °C		W
dv/dt ⁽³⁾	Peak diode recovery voltage slope	40	V/ns
dv/dt ⁽⁴⁾	MOSFET dv/dt ruggedness	50	V/IIS
V _{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; T _C = 25 °C)		V
T _{stg}	Storage temperature range	55 to 150	°C
Tj	Max. operating junction temperature range	–55 to 150	

Notes:

Table 3: Thermal data

Symbol	Parameter	Value	Unit
R _{thj-case}	e Thermal resistance junction-case max.		°C/W
R _{thj-amb}	Thermal resistance junction-ambient max.		C/VV

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I _{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T _{Jmax})	3.5	А
Eas	Single pulse avalanche energy (starting $T_J = 25$ °C, $I_D = I_{AR}$; $V_{DD} = 50$ V)	180	mJ

⁽¹⁾ Limited by package.

⁽²⁾ Pulse width is limited by safe operating area.

 $^{^{(3)}}$ IsD \leq 18 A, di/dt \leq 400 A/µS, VDS(peak) < V(BR)DSS, VDD = 400 V.

 $^{^{(4)}}$ V_{DS} ≤ 480 V.

2 Electrical characteristics

(T_{case}= 25 °C unless otherwise specified)

Table 5: On /off states

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0 \text{ V}, I_D = 1 \text{ mA}$	600			٧
	Zoro goto voltago droin	V _{GS} = 0 V, V _{DS} = 600 V			1.5	μΑ
IDSS	Zero gate voltage drain current	$V_{GS} = 0 \text{ V}, V_{DS} = 600 \text{ V},$ $T_{C} = 125 ^{\circ}\text{C}$ (1)			100	μΑ
Igss	Gate-body leakage current	V _{DS} = 0 V, V _{GS} = ±25 V			±10	μΑ
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	3	4	5	V
R _{DS(on)}	Static drain-source on- resistance	V _{GS} = 10 V, I _D = 9 A		0.175	0.200	Ω

Notes:

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
Ciss	Input capacitance		-	1055	ı	pF
Coss	Output capacitance	V _{DS} = 100 V, f = 1 MHz,	-	56	ı	pF
Crss	Reverse transfer capacitance	Ves = 0 V	-	2.4	-	pF
Coss eq. (1)	Equivalent output capacitance	V _{DS} = 0 to 480 V, V _{GS} = 0 V	-	259	-	pF
Rg	Intrinsic gate resistance	sistance $f = 1 \text{ MHz}, I_D = 0 \text{ A}$		7	-	Ω
Qg	Total gate charge	V _{DD} = 480 V, I _D = 18 A,		29	-	nC
Q _{gs}	Gate-source charge	V _{GS} = 10 V	-	6	-	nC
Q_{gd}	Gate-drain charge	(see Figure 15: "Test circuit for gate charge behavior")	-	12	-	nC

Notes:

⁽¹⁾Defined by design, not subject to production test.

 $^{^{(1)}}C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{OSS} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 300 V, I _D = 9 A	ı	15	-	ns
tr	Rise time	$R_G = 4.7 \Omega$, $V_{GS} = 10 V$	ı	8.7	-	ns
t _{d(off)}	Turn-off-delay time	(see Figure 14: "Test circuit for resistive load switching times"	-	60	-	ns
t _f	Fall time	and Figure 19: "Switching time waveform")	-	15	-	ns

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I _{SD}	Source-drain current		-		18	Α
I _{SDM} ⁽¹⁾	Source-drain current (pulsed)		-		72	Α
V _{SD} (2)	Forward on voltage	V _{GS} = 0 V, I _{SD} = 18 A	-		1.6	V
t _{rr}	Reverse recovery time	I _{SD} = 18 A, di/dt = 100 A/μs,	-	155		ns
Qrr	Reverse recovery charge	V _{DD} = 60 V (see Figure 16: "Test circuit for inductive load	-	956		nC
I _{RRM}	Reverse recovery current	switching and diode recovery times")	-	12.5		Α
t _{rr}	Reverse recovery time	I _{SD} = 18 A, di/dt = 100 A/μs,	-	200		ns
Qrr	Reverse recovery charge	$V_{DD} = 60 \text{ V}, T_j = 150 ^{\circ}\text{C}$ (see Figure 16: "Test circuit for	-	1450		nC
I _{RRM}	Reverse recovery current	inductive load switching and diode recovery times")	-	13		Α

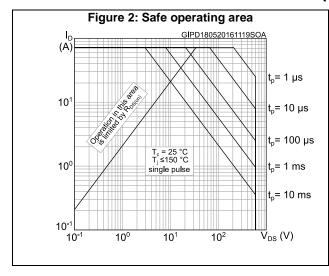
Notes:



 $^{^{\}left(1\right) }$ Pulse width is limited by safe operating area.

 $^{^{(2)}}$ Pulse test: pulse duration = 300 μ s, duty cycle 1.5%.

2.1 Electrical characteristics (curves)



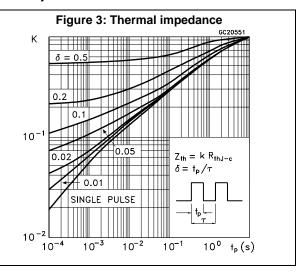
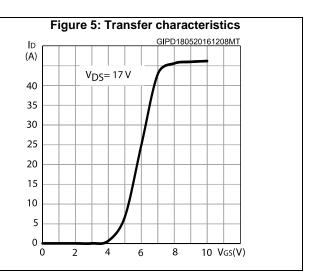
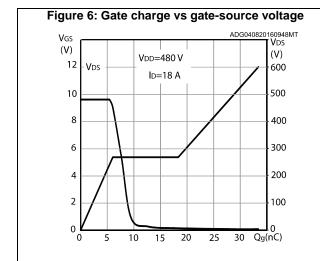
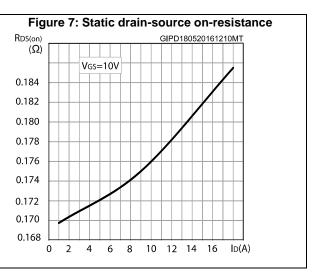


Figure 4: Output characteristics GIPD180520161207MT V_{GS}= 8, 9, 10 V (A) $V_{GS} = 7 V$ 40 35 30 25 V_{GS}= 6 V 20 15 10 $V_{GS} = 5 V$ 5 $V_{GS} = 4 V$ 0 5 10 15 20 VDS(V)

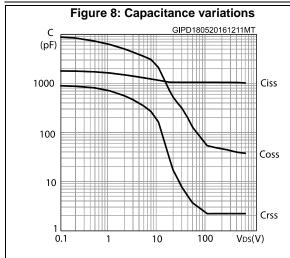




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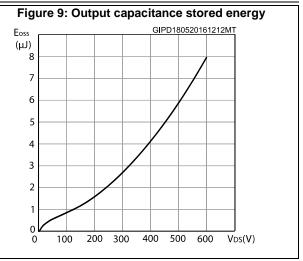
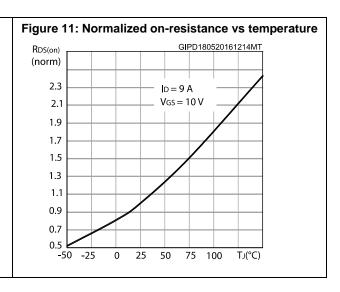
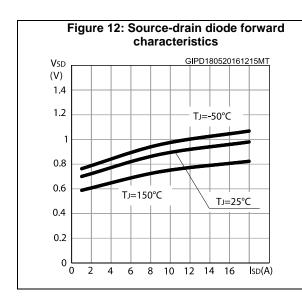
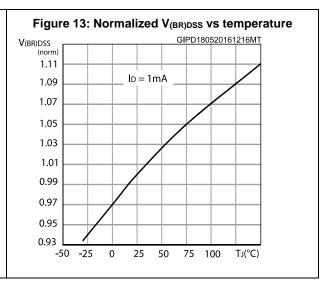


Figure 10: Normalized gate threshold voltage vs temperature $V_{GS(th)}$ GIPD180520161213MT (norm) $I_D = 250 \; \mu A$ 1.1 1.0 0.9 0.8 0.7 0.6 0 25 50 75 100









Test circuits STF24N60DM2

3 Test circuits

Figure 14: Test circuit for resistive load switching times

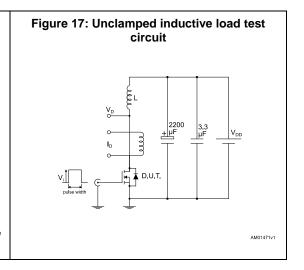
Figure 15: Test circuit for gate charge behavior

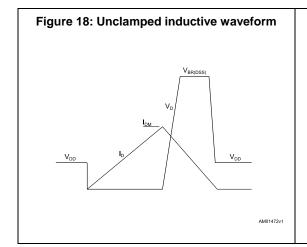
12 V 47 kΩ 100 nF D.U.T.

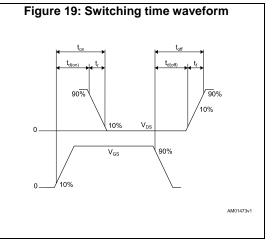
2200 V_G 47 kΩ 0 V_G

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Figure 16: Test circuit for inductive load switching and diode recovery times







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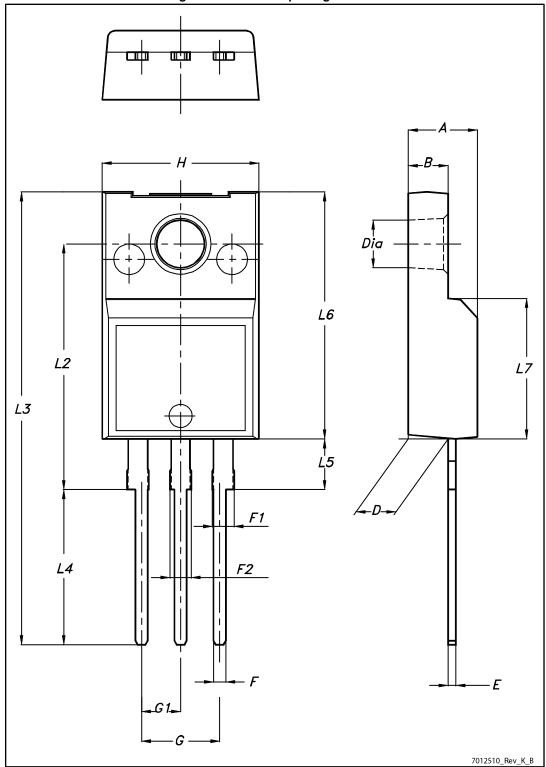
4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: **www.st.com**. ECOPACK® is an ST trademark.



4.1 TO-220FP package information

Figure 20: TO-220FP package outline



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Table 9: TO-220FP package mechanical data

Di		mm	
Dim.	Min.	Тур.	Max.
А	4.4		4.6
В	2.5		2.7
D	2.5		2.75
Е	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
Н	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2



Revision history STF24N60DM2

5 Revision history

Table 10: Document revision history

Date	Revision	Changes
12-Nov-2013	1	First release.
21-Jan-2014	2	 Modified: dv/dt value in Table 2 Modified: I_{AR} value in Table 4 Modified: I_{DSS} and V_{GS(th)} in Table 5 Minor text changes
03-Mar-2014	3	- Modified: Figure 1 - Modified: P _{TOT} value and note 1 in Table 2 - Modified: R _{thj-case} value in Table 3 - Modified: I _{AR} value in Table 4 - Minor text changes
05-Mar-2015	4	Document status promoted from preliminary to production data.Updated title, features and description in cover page.
20-Sep-2016	5	Updated Figure 2: "Safe operating area". Minor text changes

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