



# STF17N62K3 STP17N62K3, STW17N62K3

N-channel 620 V, 0.28  $\Omega$ , 15.5 A, TO-220FP, TO-220, TO-247  
SuperMESH3™ Power MOSFET

## Features

Order codes	V <sub>DSS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>	P <sub>w</sub>
STF17N62K3	620 V	< 0.34 $\Omega$	15.5 A	40 W
STP17N62K3	620 V	< 0.34 $\Omega$	15.5 A	190 W
STW17N62K3	620 V	< 0.34 $\Omega$	15.5 A	190 W

- 100% avalanche tested
- Extremely high dv/dt capability
- Gate charge minimized
- Very low intrinsic capacitance
- Improved diode reverse recovery characteristics
- Zener-protected

## Applications

- Switching applications

## Description

This SuperMESH3™ Power MOSFET is the result of improvements applied to STMicroelectronics' SuperMESH™ technology, combined with a new optimized vertical structure. This device boasts an extremely low on-resistance, superior dynamic performance and high avalanche capability, rendering it suitable for the most demanding applications.

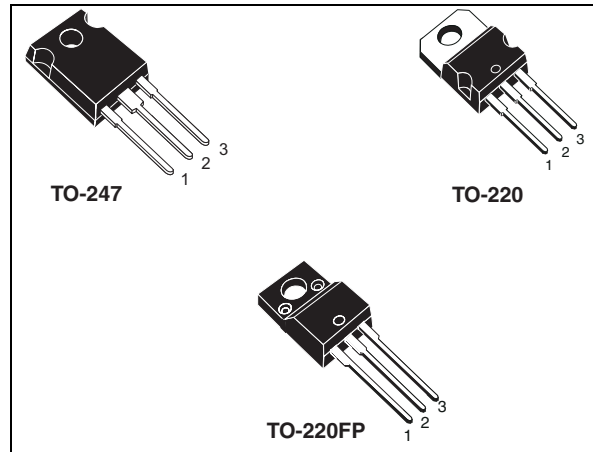


Figure 1. Internal schematic diagram

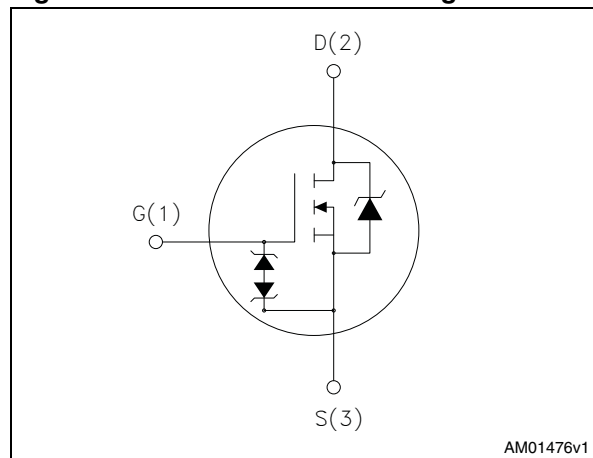


Table 1. Device summary

Order codes	Marking	Package	Packaging
STF17N62K3	17N62K3	TO-220FP	Tube
STP17N62K3	17N62K3	TO-220	Tube
STW17N62K3	17N62K3	TO-247	Tube

# Contents

<b>1</b>	<b>Electrical ratings</b> .....	<b>3</b>
<b>2</b>	<b>Electrical characteristics</b> .....	<b>4</b>
2.1	Electrical characteristics (curves) .....	6
<b>3</b>	<b>Test circuits</b> .....	<b>9</b>
<b>4</b>	<b>Package mechanical data</b> .....	<b>10</b>
<b>5</b>	<b>Revision history</b> .....	<b>16</b>



# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value		Unit
		TO-220 TO-247	TO-220FP	
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	620		V
$V_{GS}$	Gate- source voltage	$\pm 30$		V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	15.5	15.5 <sup>(1)</sup>	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	10	10 <sup>(1)</sup>	A
$I_{DM}$ <sup>(2)</sup>	Drain current (pulsed)	62	62 <sup>(1)</sup>	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	190	40	W
$I_{AR}$ <sup>(3)</sup>	Avalanche current, repetitive or not-repetitive	15.5		A
$E_{AS}$ <sup>(4)</sup>	Single pulse avalanche energy	260		mJ
	Derating factor	1.52	0.32	W/ $^\circ\text{C}$
$dv/dt$ <sup>(5)</sup>	Peak diode recovery voltage slope	9		V/ns
$V_{ISO}$	Insulation withstand voltage (RMS) from all three leads to external heat sink ( $t = 1\text{ s}$ ; $T_C = 25\text{ }^\circ\text{C}$ )		2500	V
$T_{stg}$	Storage temperature	-55 to 150		$^\circ\text{C}$
$T_j$	Max. operating junction temperature	150		$^\circ\text{C}$

- Limited only by temperature allowed.
- Pulse width limited by safe operating area.
- Pulse width limited by  $T_j$  max.
- Starting  $T_j = 25\text{ }^\circ\text{C}$ ,  $I_D = I_{AR}$ ,  $V_{DD} = 50\text{ V}$ .
- $I_{SD} \leq 15.5\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ,  $V_{DD} = 80\% V_{(BR)DSS}$ ,  $V_{DS\text{ peak}} < V_{(BR)DSS}$ .

**Table 3. Thermal data**

Symbol	Parameter	TO-220FP	TO-220	TO-247	Unit
$R_{thj-case}$	Thermal resistance junction-case max	3.13	0.66		$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	62.5		50	$^\circ\text{C}/\text{W}$
$T_l$	Maximum lead temperature for soldering purpose	300			$^\circ\text{C}$

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified)

**Table 4. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage ( $V_{GS} = 0$ )	$I_D = 1\text{ mA}$	620			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = 620\text{ V}$ $V_{DS} = 620\text{ V}, T_C = 125\text{ °C}$			1 50	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20\text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 100\text{ }\mu\text{A}$	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}, I_D = 7.5\text{ A}$		0.28	0.34	$\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 50\text{ V}, f = 1\text{ MHz}, V_{GS} = 0$	-	3100	-	pF
$C_{oss}$	Output capacitance			200		pF
$C_{rss}$	Reverse transfer capacitance			35		pF
$C_{o(tr)}^{(1)}$	Equivalent capacitance time related	$V_{DS} = 0\text{ to }496\text{ V}, V_{GS} = 0$	-	140	-	pF
$C_{o(er)}^{(2)}$	Equivalent capacitance energy related			200		pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz open drain}$	-	2.3	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 496\text{ V}, I_D = 15.5\text{ A},$ $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 20</a> )	-	105	-	nC
$Q_{gs}$	Gate-source charge			16		nC
$Q_{gd}$	Gate-drain charge			62		nC

- $C_{oss\text{ eq.}}$  time related is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$
- $C_{oss\text{ eq.}}$  energy related is defined as a constant equivalent capacitance giving the same stored energy as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 310\text{ V}$ , $I_D = 7.5\text{ A}$ , $R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 19</a> )	-	22	-	ns
$t_r$	Rise time			29		ns
$t_{d(off)}$	Turn-off-delay time			110		ns
$t_f$	Fall time			62		ns

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		15.5	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				62	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 15.5\text{ A}$ , $V_{GS} = 0$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 15.5\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ (see <a href="#">Figure 24</a> )	-	380		ns
$Q_{rr}$	Reverse recovery charge			5000		nC
$I_{RRM}$	Reverse recovery current			26		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 15.5\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$ (see <a href="#">Figure 24</a> )	-	450		ns
$Q_{rr}$	Reverse recovery charge			6500		nC
$I_{RRM}$	Reverse recovery current			29		A

1. Pulse width limited by safe operating area

2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

**Table 8. Gate-source Zener diode**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$BV_{GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1\text{ mA}$ (open drain)	30			V

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220FP

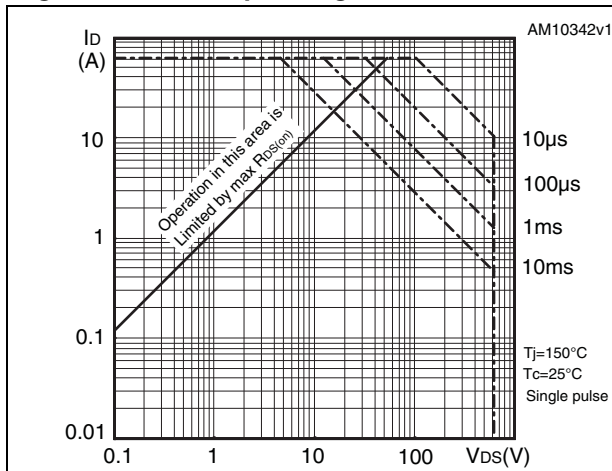


Figure 3. Thermal impedance for TO-220FP

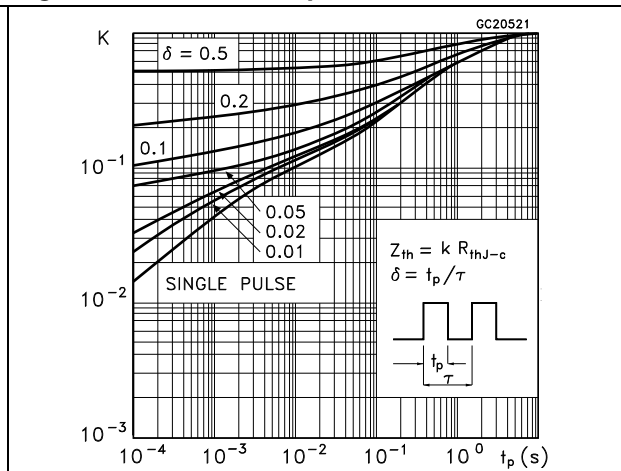


Figure 4. Safe operating area for TO-220

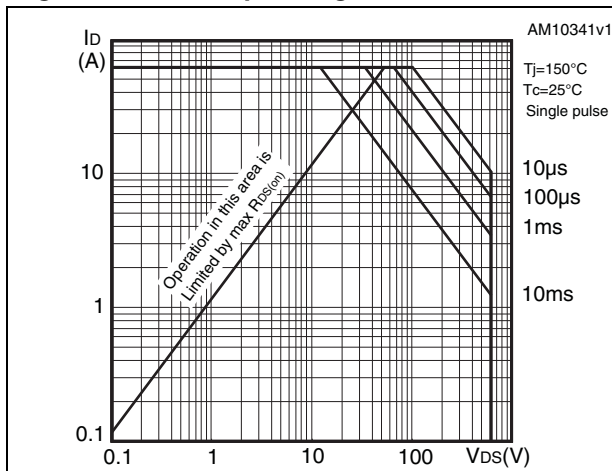


Figure 5. Thermal impedance for TO-220

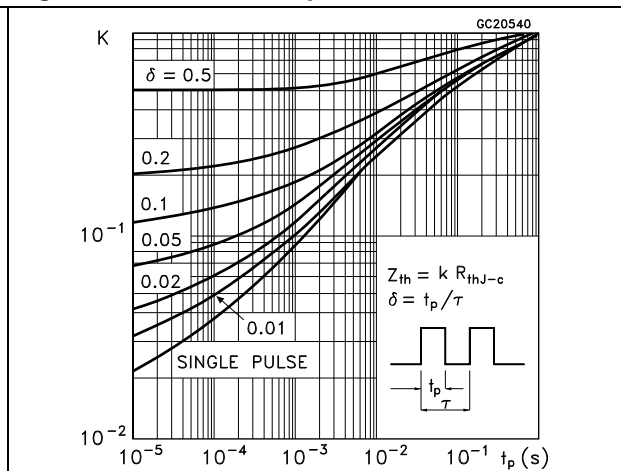


Figure 6. Safe operating area for TO-247

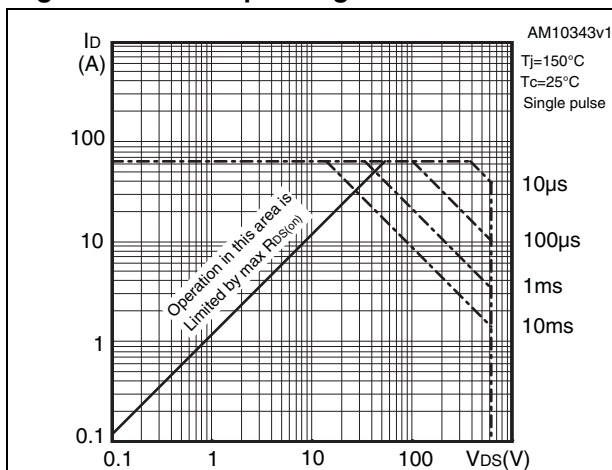


Figure 7. Thermal impedance for TO-247

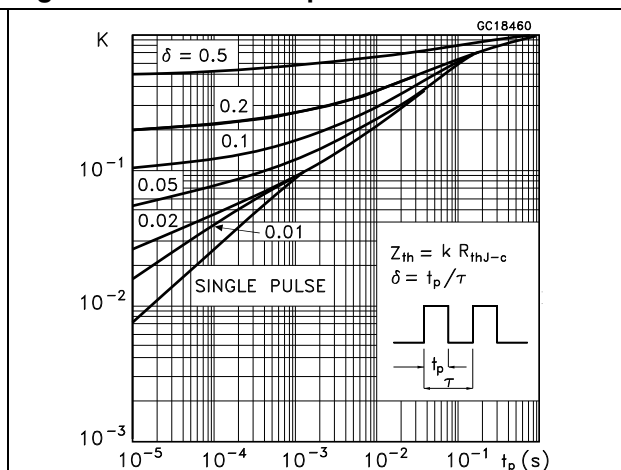


Figure 8. Output characteristics

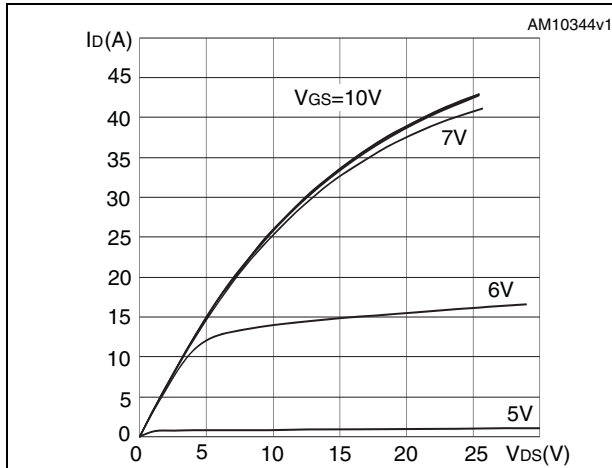


Figure 9. Transfer characteristics

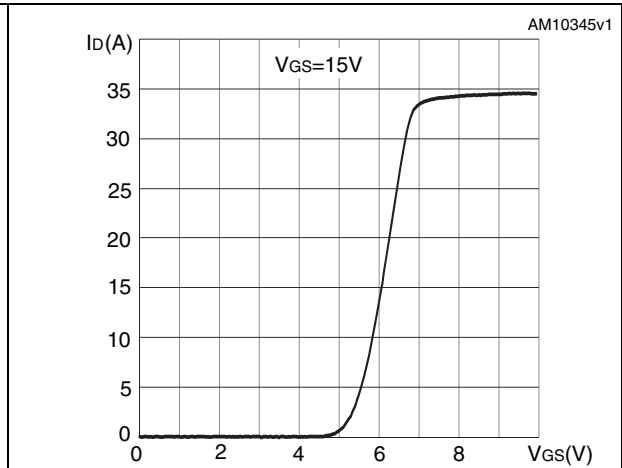


Figure 10. Gate charge vs gate-source voltage

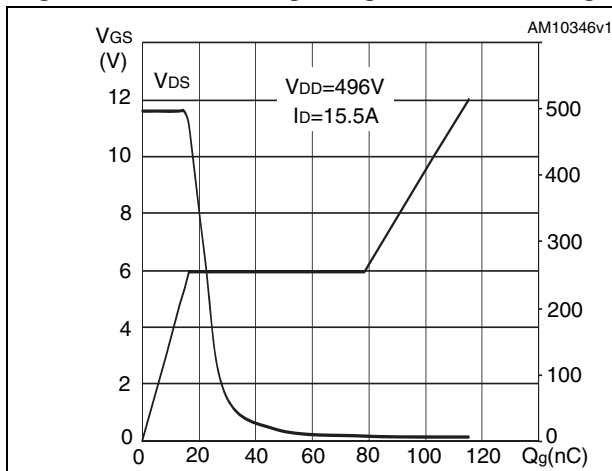


Figure 11. Static drain-source on resistance

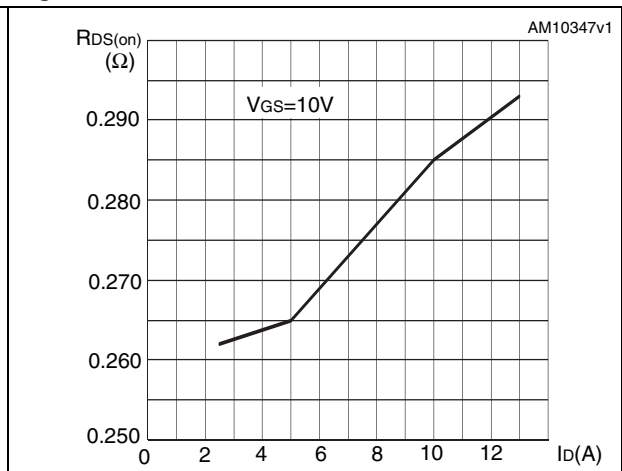


Figure 12. Capacitance variations

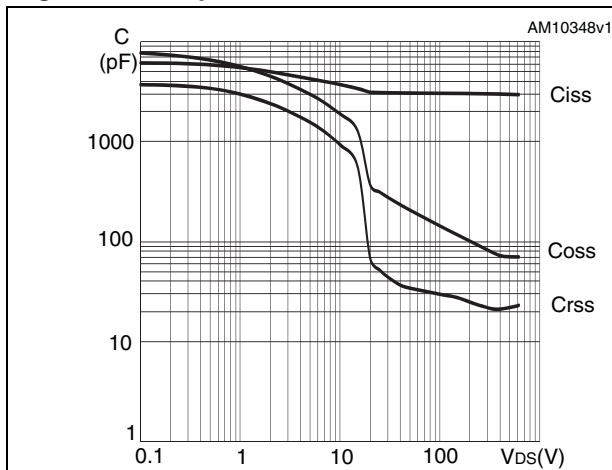


Figure 13. Output capacitance stored energy

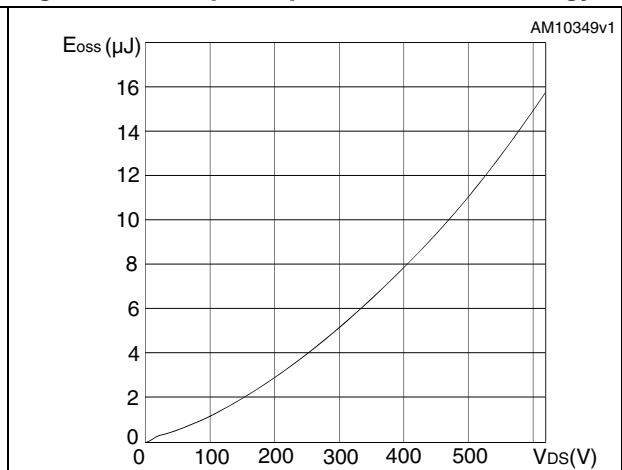


Figure 14. Normalized gate threshold voltage vs temperature

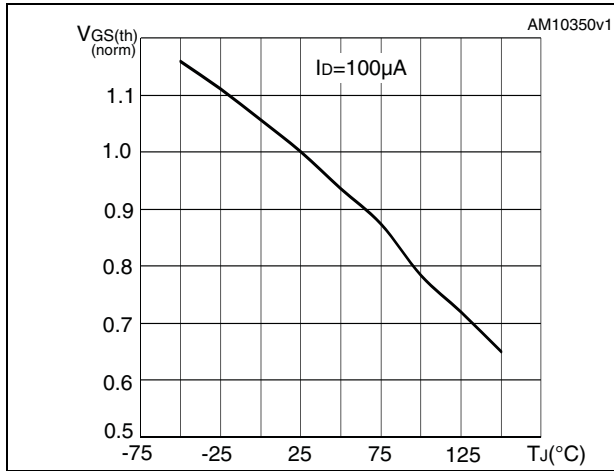


Figure 15. Normalized on resistance vs temperature

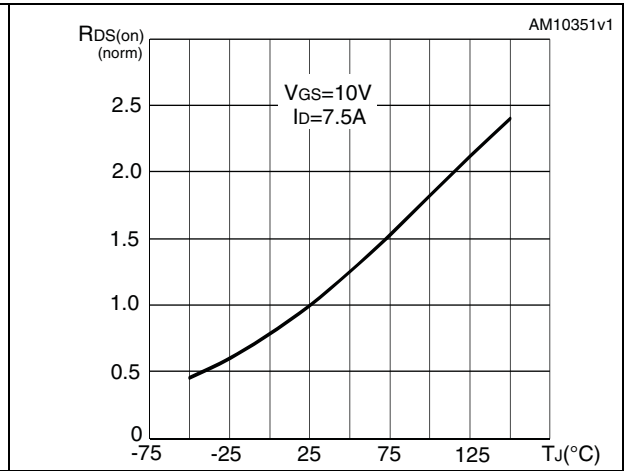


Figure 16. Source-drain diode forward characteristics

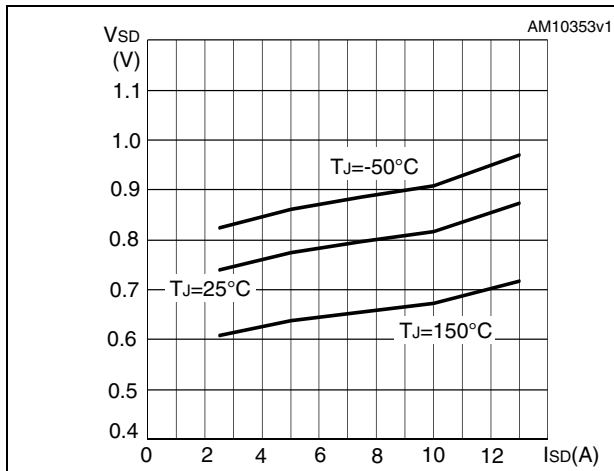


Figure 17. Normalized BV<sub>DSS</sub> vs temperature

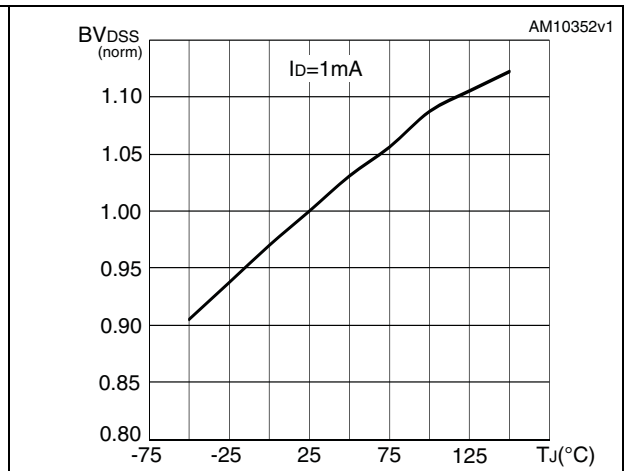
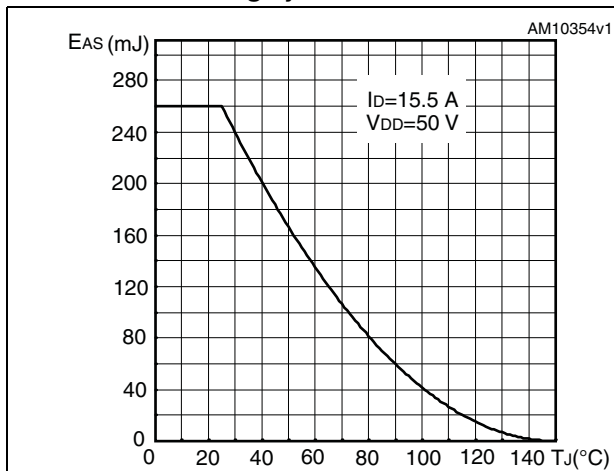


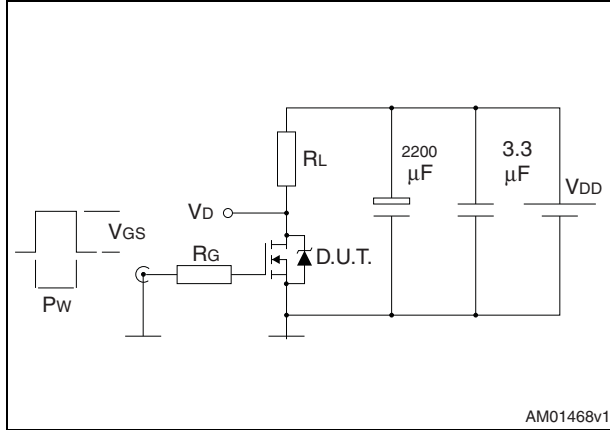
Figure 18. Maximum avalanche energy vs starting Tj





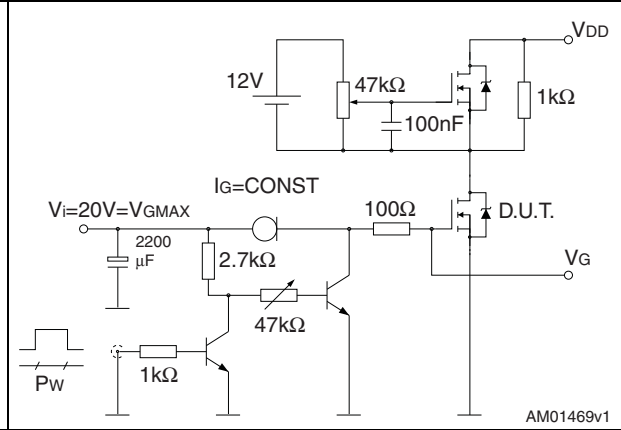
### 3 Test circuits

**Figure 19. Switching times test circuit for resistive load**



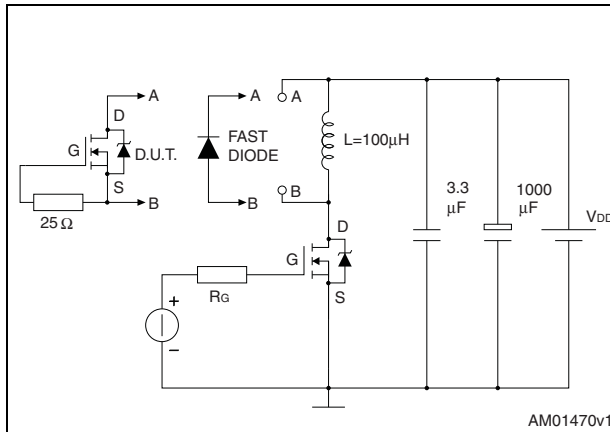
AM01468v1

**Figure 20. Gate charge test circuit**



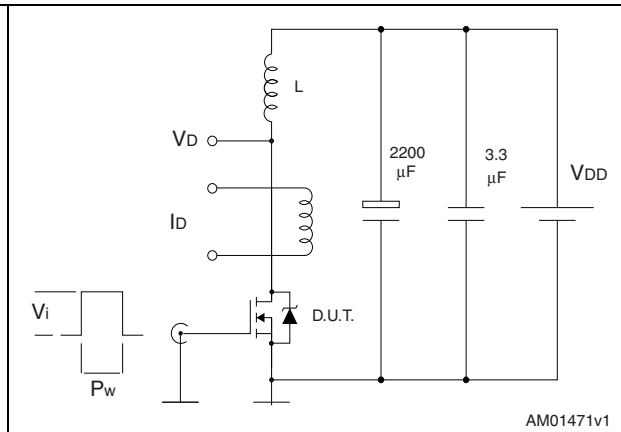
AM01469v1

**Figure 21. Test circuit for inductive load switching and diode recovery times**



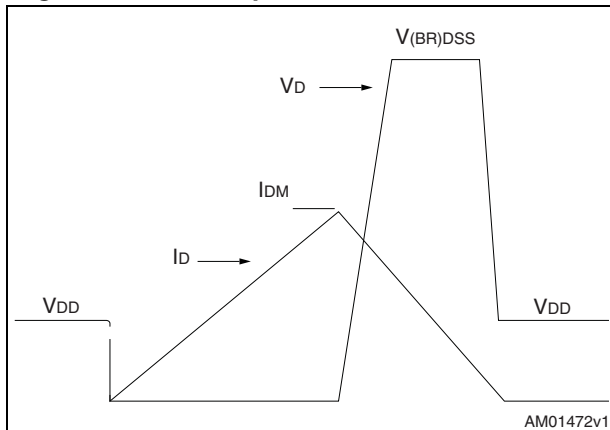
AM01470v1

**Figure 22. Unclamped Inductive load test circuit**



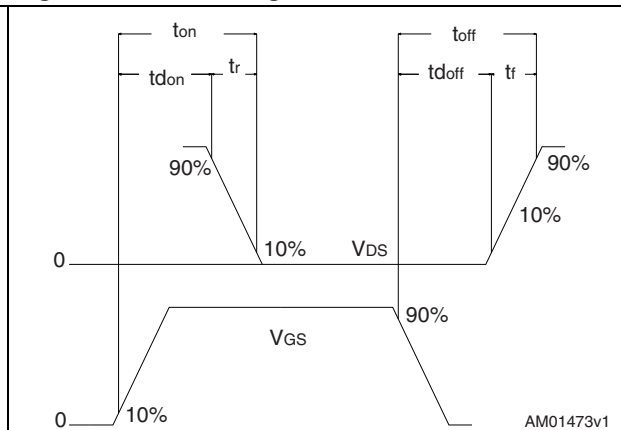
AM01471v1

**Figure 23. Unclamped inductive waveform**



AM01472v1

**Figure 24. Switching time waveform**



AM01473v1

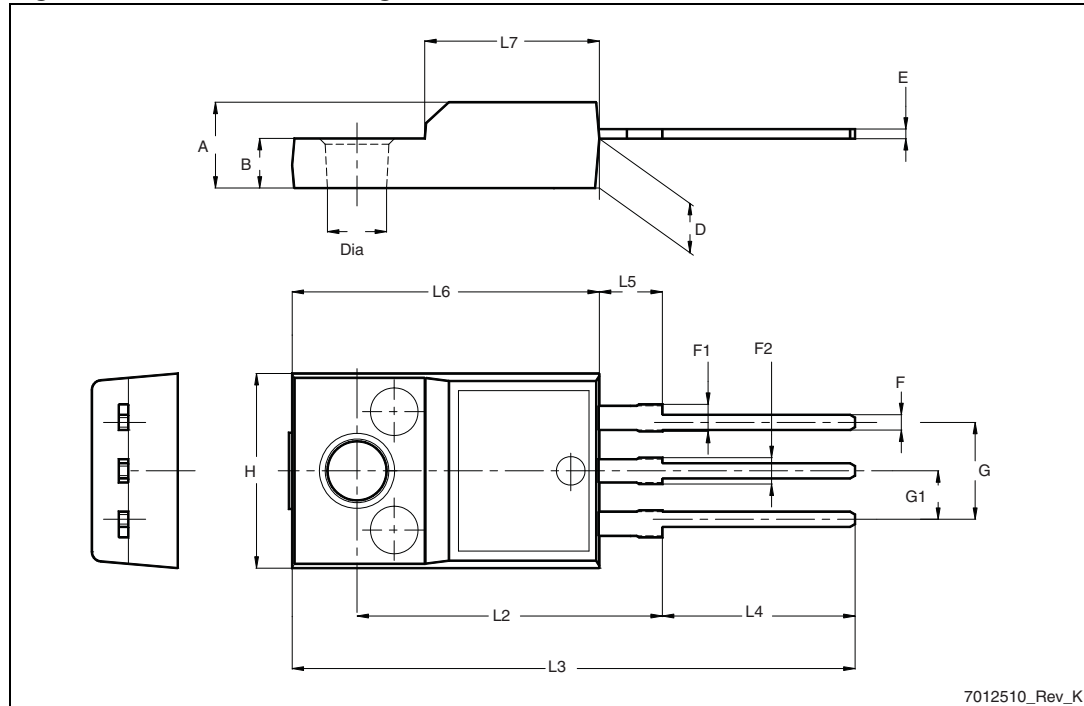
## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

Table 9. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Figure 25. TO-220FP drawing

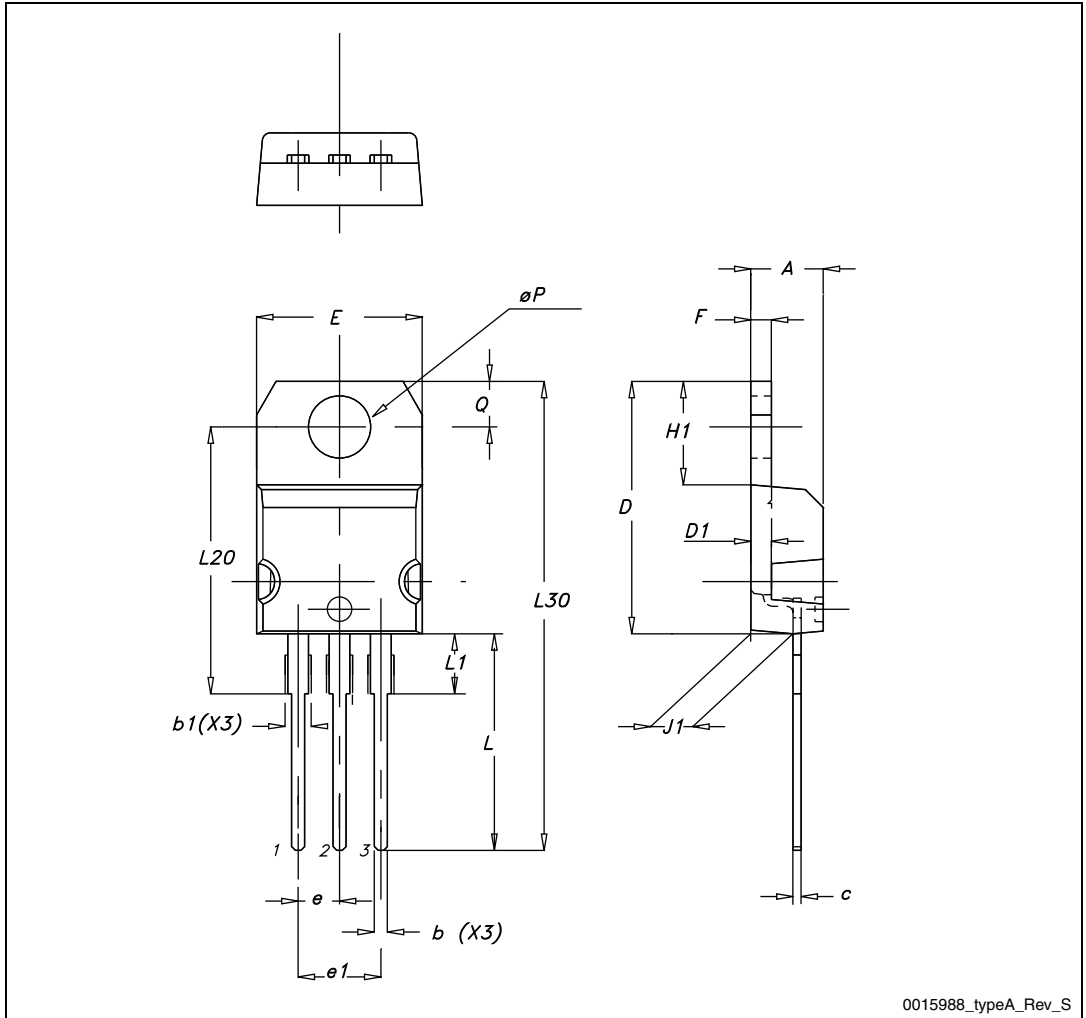


7012510\_Rev\_K

Table 10. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
ØP	3.75		3.85
Q	2.65		2.95

Figure 26. TO-220 type A drawing

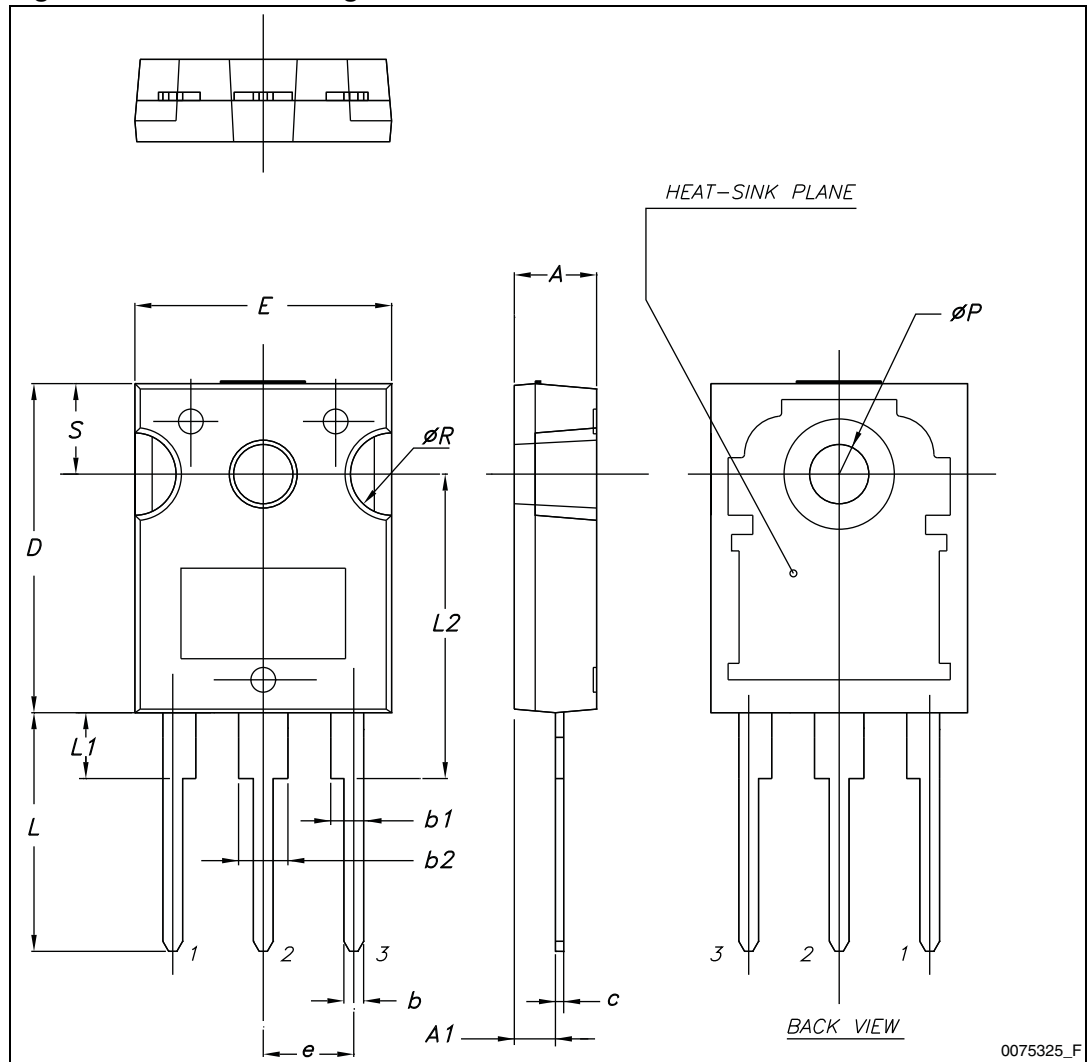


0015988\_typeA\_Rev\_S

Table 11. TO-247 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e		5.45	
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S		5.50	

Figure 27. TO-247 drawing



## 5 Revision history

Table 12. Document revision history

Date	Revision	Changes
11-Nov-2008	1	First release.
27-Jul-2011	2	<a href="#">Section 2.1: Electrical characteristics (curves)</a> has been updated. Minor text changes.



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