

## N-channel 950 V, 1 $\Omega$ typ., 6 A MDmesh™ K5 Power MOSFET in a H<sup>2</sup>PAK-2 package

Datasheet - production data

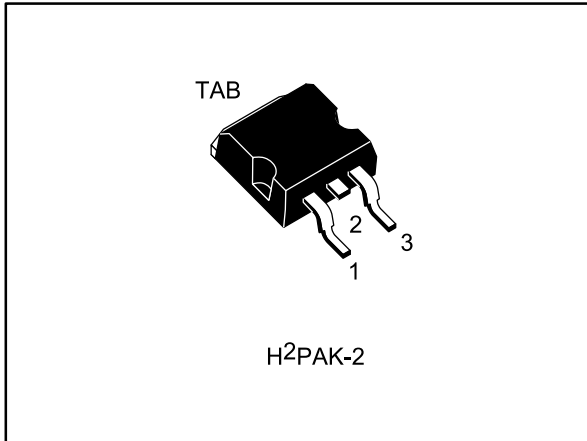
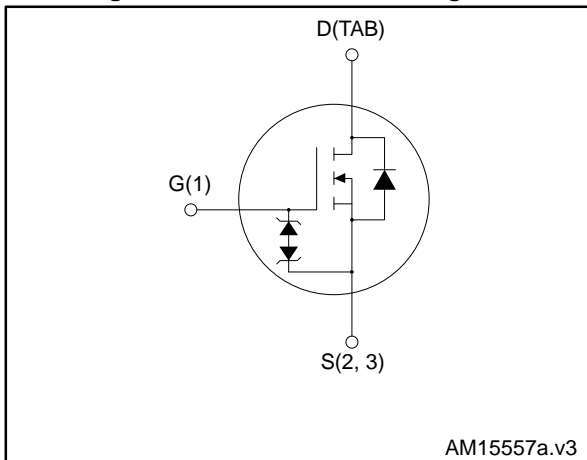


Figure 1: Internal schematic diagram



### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>	P <sub>TOT</sub>
STH6N95K5-2	950 V	1.25 $\Omega$	6 A	110 W

- Industry's lowest R<sub>DS(on)</sub> x area
- Industry's best figure of merit (FoM)
- Ultra low gate charge
- 100% avalanche tested
- Zener-protected

### Applications

- Switching applications

### Description

This very high voltage N-channel Power MOSFET is designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Table 1: Device summary

Order code	Marking	Package	Packaging
STH6N95K5-2	6N95K5	H <sup>2</sup> PAK-2	Tape and reel

---

**Contents**

<b>1</b>	<b>Electrical ratings .....</b>	<b>3</b>
<b>2</b>	<b>Electrical characteristics .....</b>	<b>4</b>
	2.1 Electrical characteristics (curves) .....	6
<b>3</b>	<b>Test circuits .....</b>	<b>9</b>
<b>4</b>	<b>Package mechanical data .....</b>	<b>10</b>
	4.1 Package mechanical data .....	11
<b>5</b>	<b>Packing information .....</b>	<b>14</b>
<b>6</b>	<b>Revision history .....</b>	<b>16</b>

# 1 Electrical ratings

**Table 2: Absolute maximum ratings**

Symbol	Parameter	Value	Unit
V <sub>GS</sub>	Gate-source voltage	± 30	V
I <sub>D</sub>	Drain current at T <sub>C</sub> = 25 °C	6	A
I <sub>D</sub>	Drain current at T <sub>C</sub> = 100 °C	3.8	A
I <sub>DM</sub> <sup>(1)</sup>	Drain current (pulsed)	24	A
P <sub>TOT</sub>	Total dissipation at T <sub>C</sub> = 25 °C	110	W
I <sub>AR</sub> <sup>(2)</sup>	Max current during repetitive or single pulse avalanche	3	A
E <sub>AS</sub> <sup>(3)</sup>	Single pulse avalanche energy	90	mJ
dv/dt <sup>(4)</sup>	Peak diode recovery voltage slope	4.5	V/ns
dv/dt <sup>(5)</sup>	MOSFET dv/dt ruggedness	50	V/ns
T <sub>j</sub>	Operating junction temperature	- 55 to 150	°C
T <sub>stg</sub>	Storage temperature		

**Notes:**

- (1)Pulse width limited by safe operating area.
- (2)Pulse width limited by T<sub>jmax</sub>.
- (3)Starting T<sub>j</sub> = 25 °C, I<sub>D</sub> = I<sub>AS</sub>, V<sub>DD</sub> = 50 V.
- (4)|I<sub>SD</sub> ≤ 6 A, di/dt ≤ 100 A/μs, V<sub>DS(peak)</sub> ≤ V<sub>(BR)DSS</sub>.
- (5)V<sub>DS</sub> ≤ 760 V.

**Table 3: Thermal data**

Symbol	Parameter	Value	Unit
R <sub>thj-case</sub>	Thermal resistance junction-case max	1.14	°C/W
R <sub>thj-pcb</sub> <sup>(1)</sup>	Thermal resistance junction-pcb max	30	

**Notes:**

- (1)When mounted on 1 inch<sup>2</sup> FR-4 board, 2 oz Cu.

## 2 Electrical characteristics

$T_C = 25\text{ °C}$  unless otherwise specified

**Table 4: On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$	950			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 950\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ , $V_{DS} = 950\text{ V}$ , $T_C = 125\text{ °C}$			50	$\mu\text{A}$
$I_{GSS}$	Gate body leakage current	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 20\text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 100\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{CS} = 10\text{ V}$ , $I_D = 3\text{ A}$		1	1.25	$\Omega$

**Table 5: Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{GS} = 0\text{ V}$ , $V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$	-	450	-	pF
$C_{oss}$	Output capacitance		-	30	-	
$C_{oss}$	Output capacitance		-	1.6	-	
$C_{o(tr)}^{(1)}$	Equivalent capacitance, time-related	$V_{GS} = 0\text{ V}$ , $V_{DS} = 0\text{ to }760\text{ V}$	-	45	-	pF
$C_{o(er)}^{(2)}$	Equivalent capacitance, energy-related		-	19	-	
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz}$ , $I_D = 0\text{ A}$	-	7	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 760\text{ V}$ , $I_D = 6\text{ A}$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 16: "Gate charge test circuit"</a> )	-	13	-	nC
$Q_{gs}$	Gate-source charge		-	3	-	
$Q_{gd}$	Gate-drain charge		-	7	-	

**Notes:**

(1)Time-related is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ .

(2)Energy-related is defined as a constant equivalent capacitance giving the same stored energy as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ .

**Table 6: Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 475\text{ V}$ , $I_D = 3\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$	-	12	-	ns
$t_r$	Rise time		-	12	-	ns
$t_{d(off)}$	Turn-off-delay time		-	33	-	ns
$t_f$	Fall time		-	21	-	ns

**Table 7: Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		6	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		24	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 6\text{ A}, V_{GS} = 0$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 6\text{ A},$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$	-	372		ns
$Q_{rr}$	Reverse recovery charge		-	4		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	22		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 6\text{ A},$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}, T_j = 150\text{ }^\circ\text{C}$	-	522		ns
$Q_{rr}$	Reverse recovery charge		-	5		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	20		A

**Notes:**

(1)Pulse width limited by safe operating area

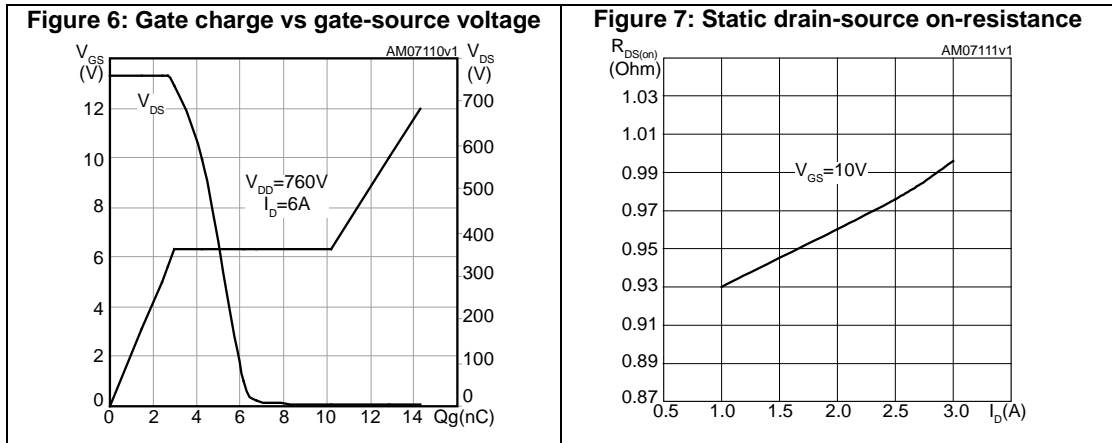
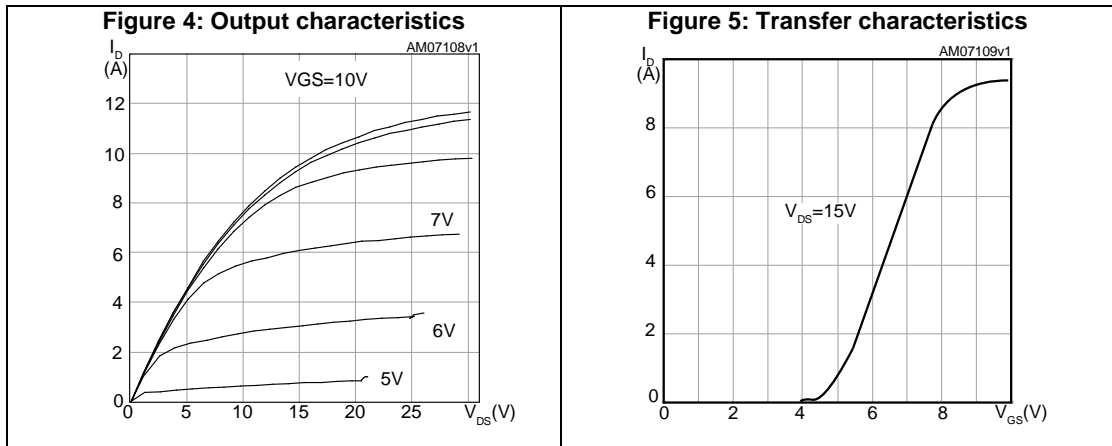
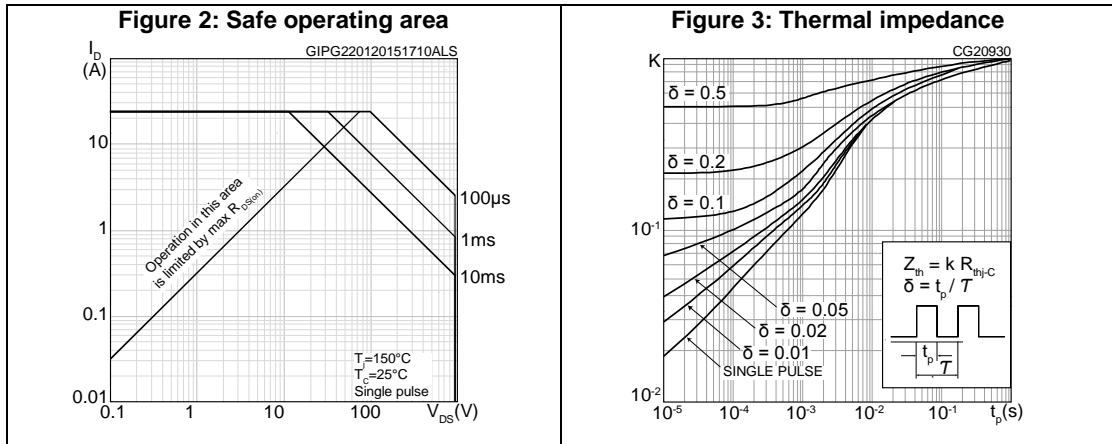
(2)Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

**Table 8: Gate-source Zener diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1\text{ mA}, I_D=0$	30	-	-	V

The built-in back-to-back Zener diodes have specifically been designed to enhance the device's ESD capability. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

## 2.1 Electrical characteristics (curves)



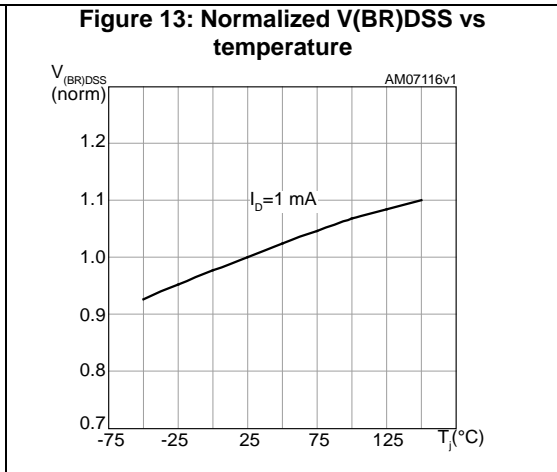
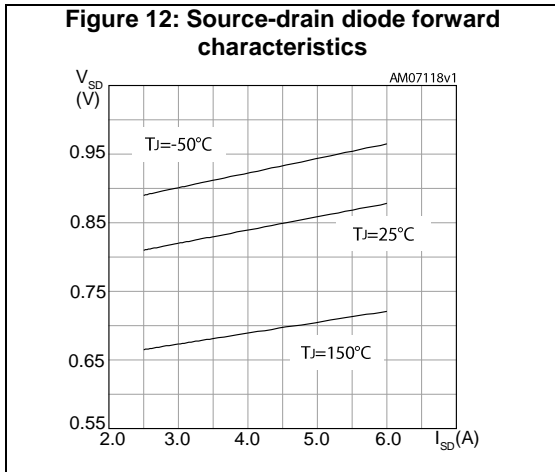
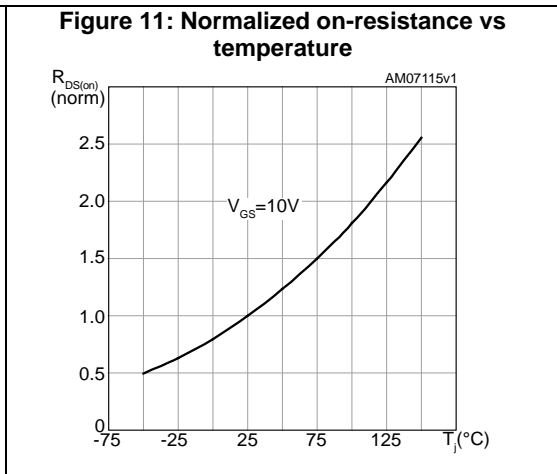
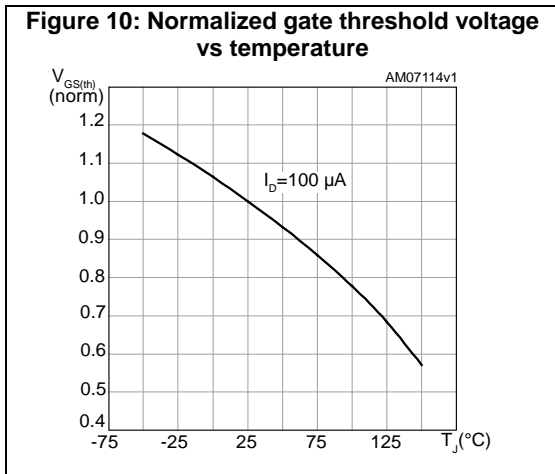
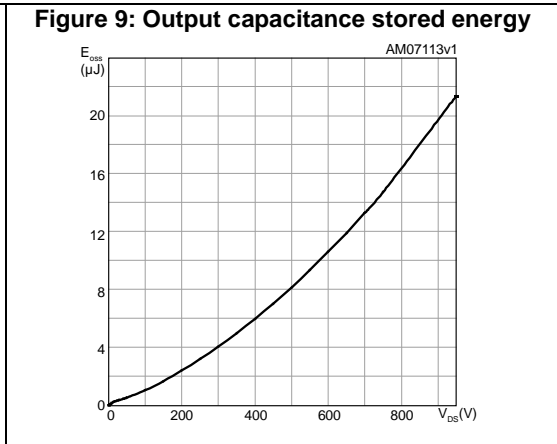
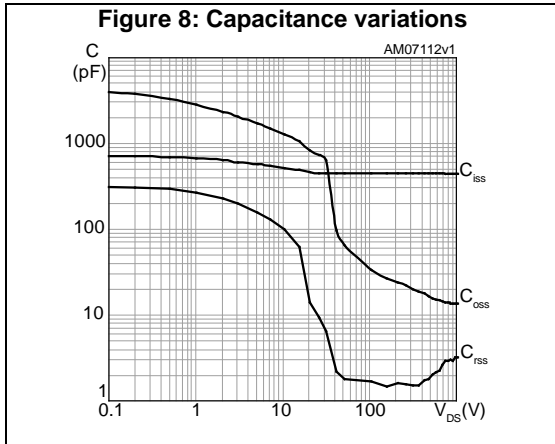
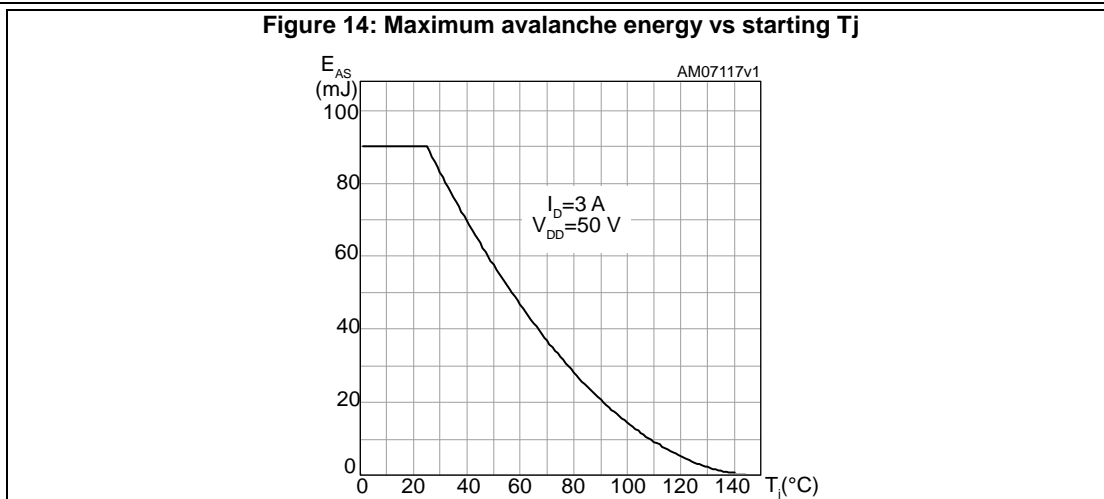
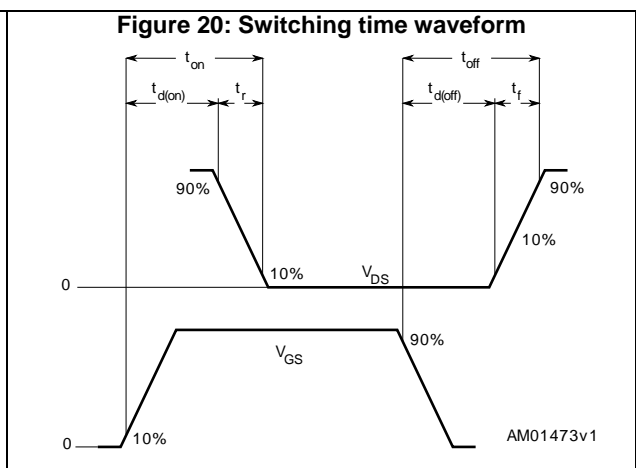
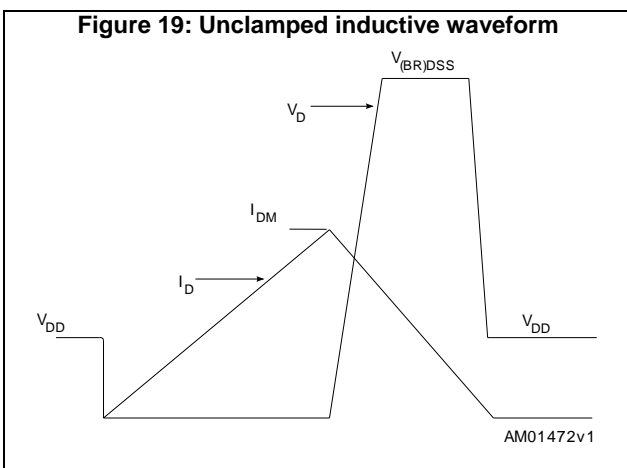
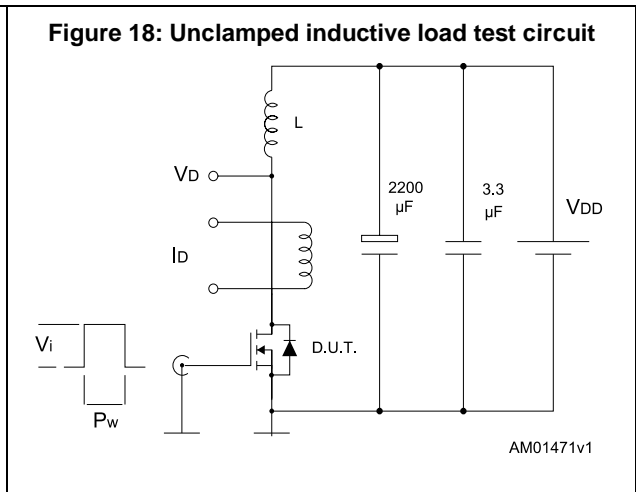
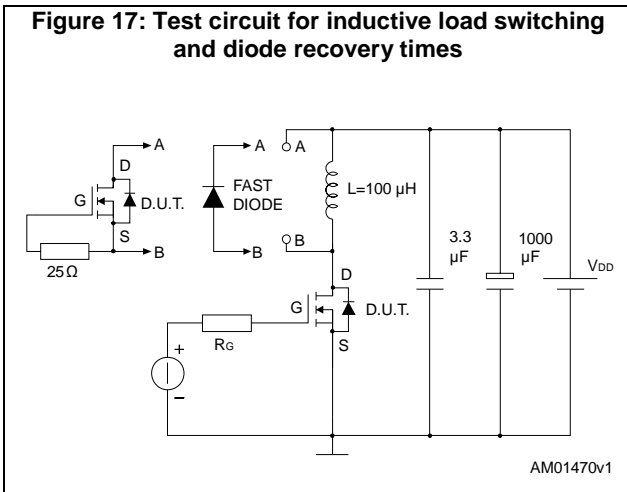
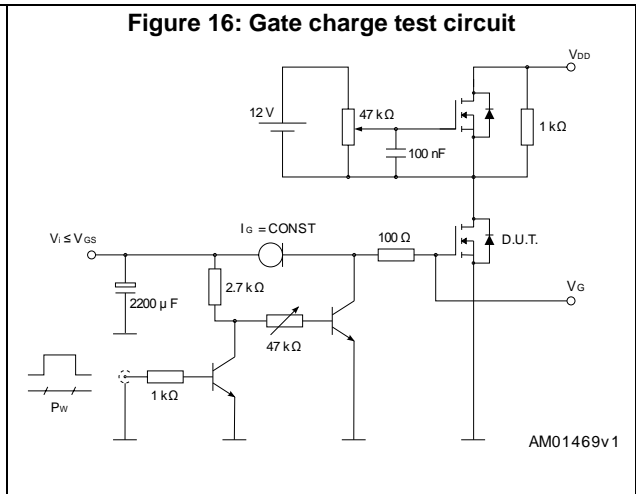
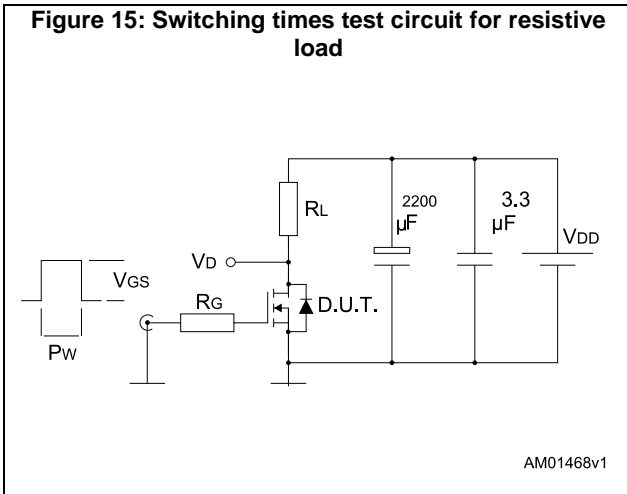


Figure 14: Maximum avalanche energy vs starting Tj





### 3 Test circuits



## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 4.1 Package mechanical data

Figure 21: H<sup>2</sup>PAK-2 outline

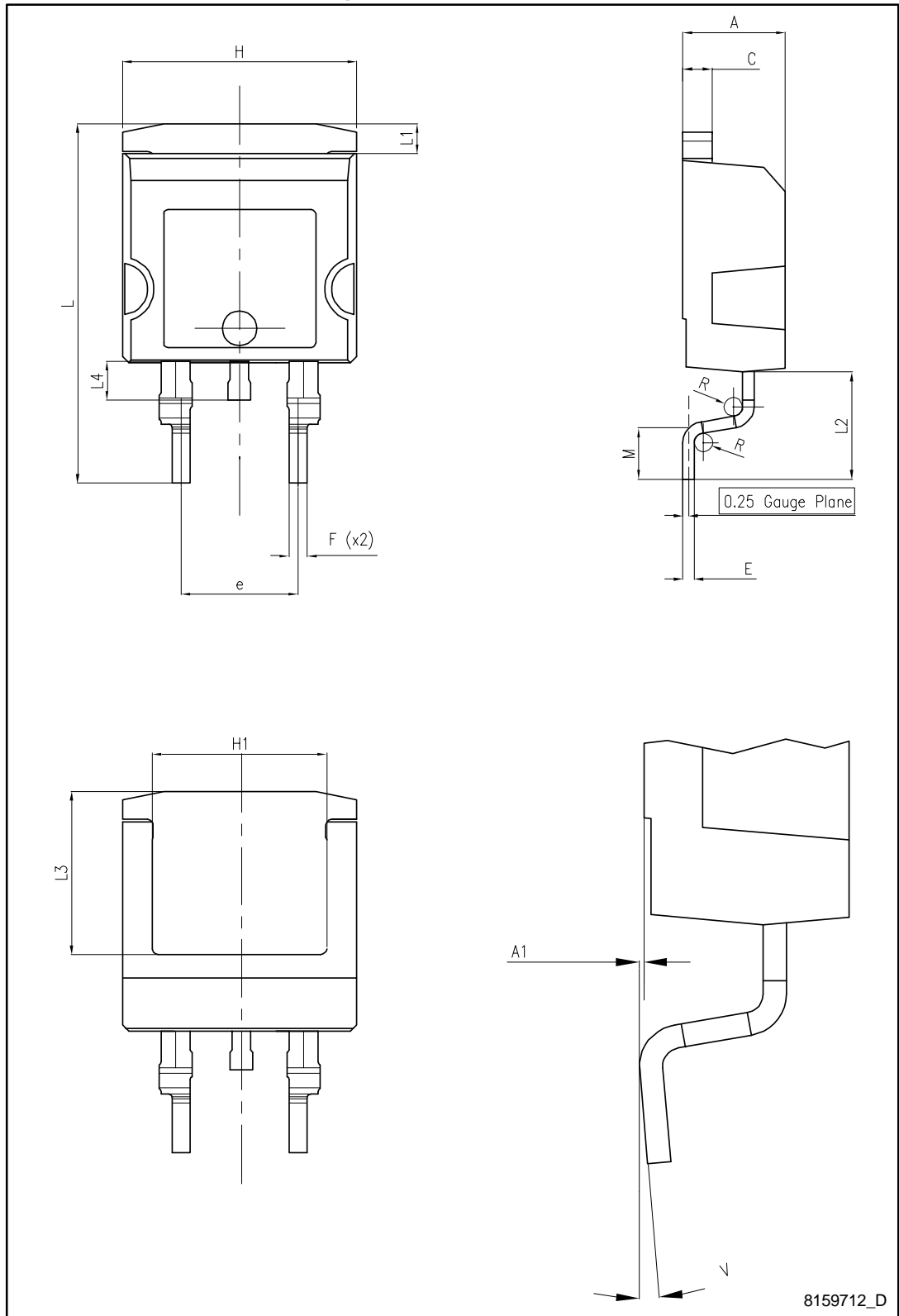
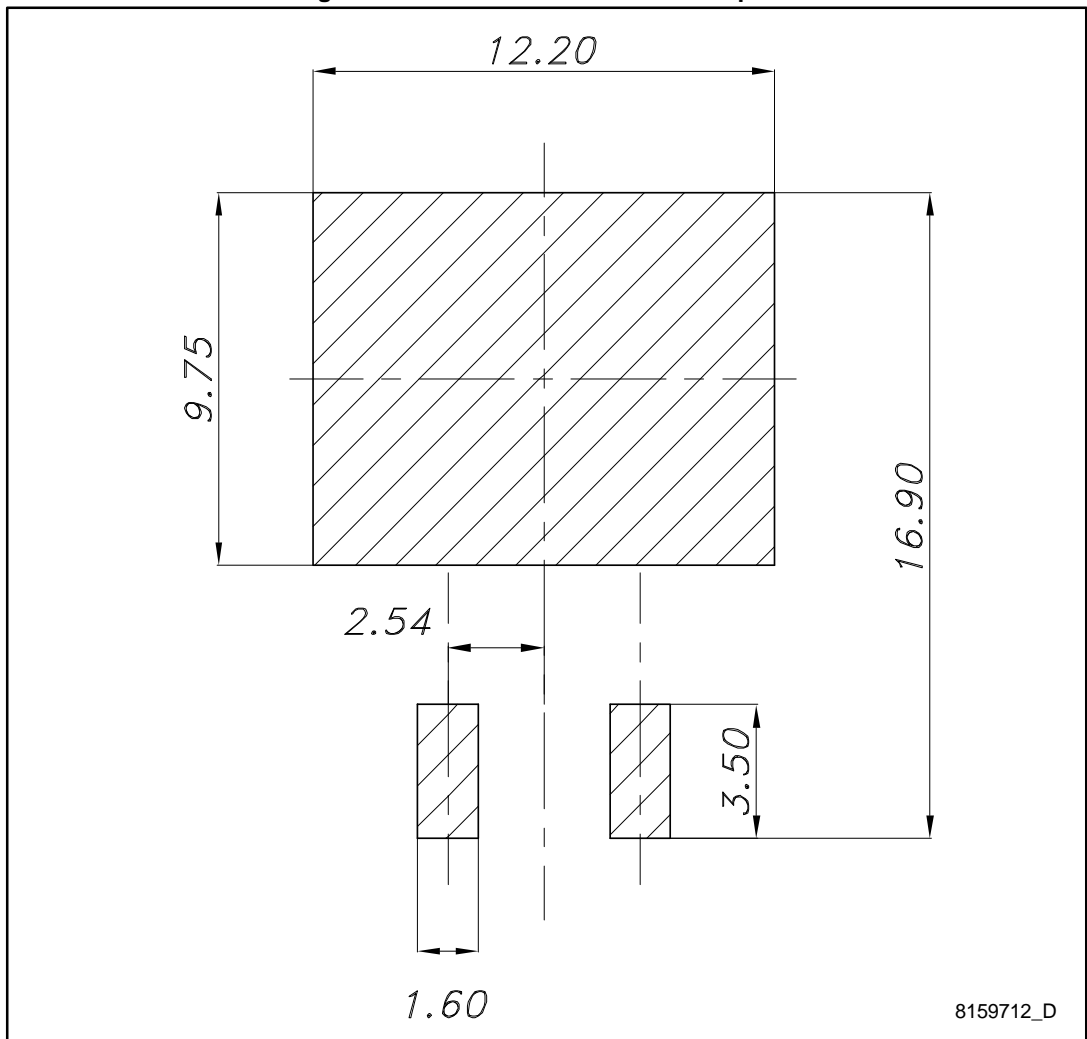


Table 9: H<sup>2</sup>PAK-2 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.30		4.80
A1	0.03		0.20
C	1.17		1.37
e	4.98		5.18
E	0.50		0.90
F	0.78		0.85
H	10.00		10.40
H1	7.40		7.80
L	15.30		15.80
L1	1.27		1.40
L2	4.93		5.23
L3	6.85		7.25
L4	1.5		1.7
M	2.6		2.9
R	0.20		0.60
V	0°		8°

Figure 22: H<sup>2</sup>PAK-2 recommended footprint



8159712\_D

# 5 Packing information

Figure 23: Tape outline

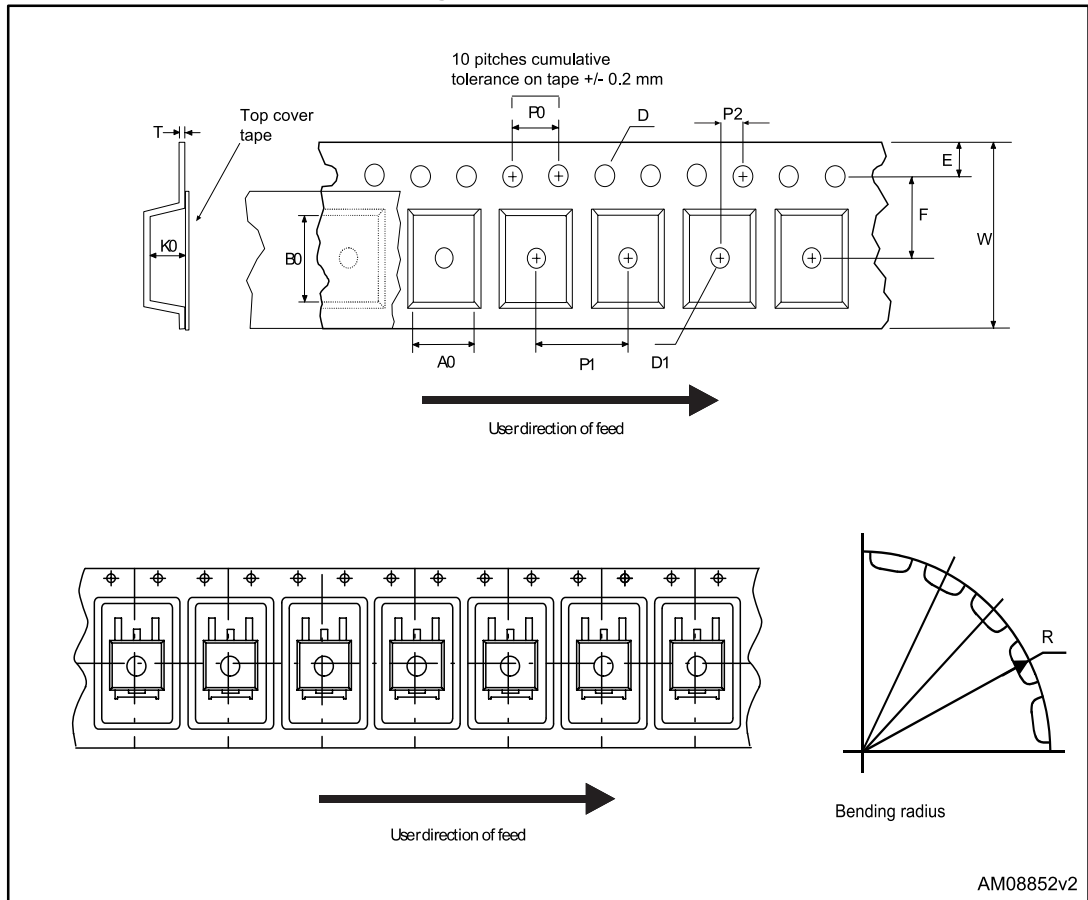


Figure 24: Reel outline

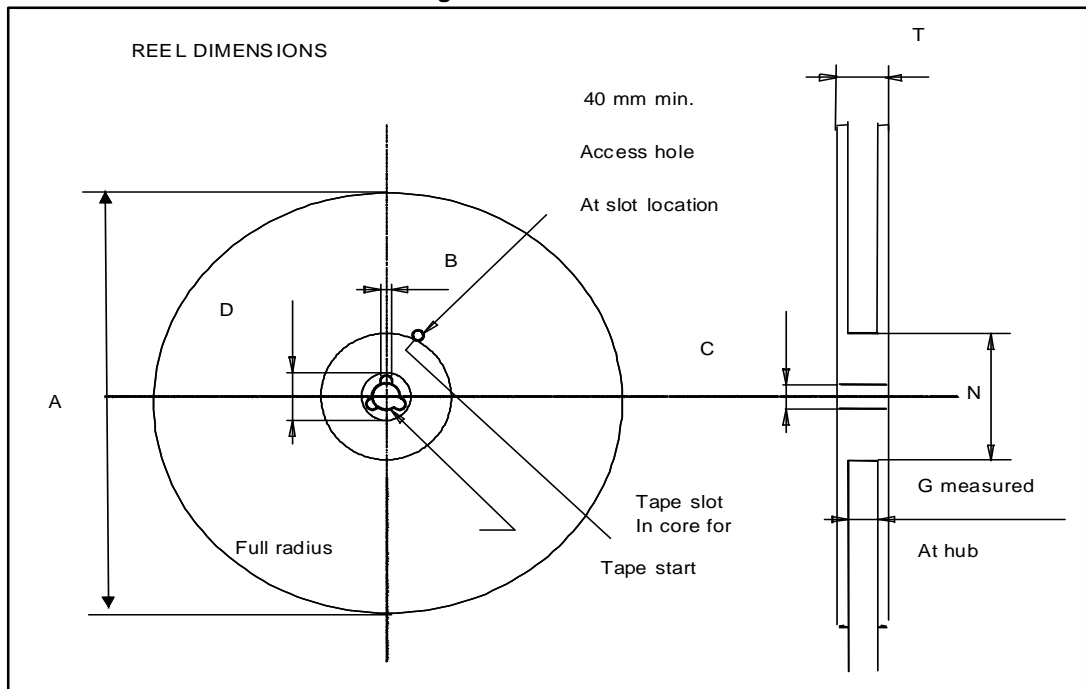


Table 10: Tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base quantity		1000
P2	1.9	2.1	Bulk quantity		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

## 6 Revision history

Table 11: Document revision history

Date	Revision	Changes
23-Jan-2015	1	First release.
04-Feb-2015	2	Updated <i>Section 2: "Electrical characteristics"</i>
12-Mar-2015	3	Document status changed from preliminary to production data.



**IMPORTANT NOTICE – PLEASE READ CAREFULLY**

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2015 STMicroelectronics – All rights reserved

单击下面可查看定价，库存，交付和生命周期等信息

[>>STMicro\(意法半导体\)](#)