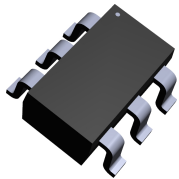
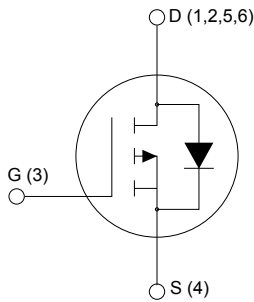


## P-channel 30 V, 48 mΩ typ., 4 A, STripFET H6 Power MOSFET in an SOT23-6L package



SOT23-6L



PG3D1256S4

### Features

Order code	$V_{DS}$	$R_{DS(on)}$ max.	$I_D$
STT4P3LLH6	30 V	56 mΩ at 10 V	4 A

- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

### Applications

- Switching applications

### Description

This device is a P-channel Power MOSFET developed using the STripFET H6 technology with a new trench gate structure. The resulting Power MOSFET exhibits very low  $R_{DS(on)}$  in all packages.



#### Product status link

[STT4P3LLH6](#)

#### Product summary

<b>Order code</b>	STT4P3LLH6
<b>Marking</b>	4K3L
<b>Package</b>	SOT23-6L
<b>Packing</b>	Tape and reel

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	30	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D$	Drain current (continuous) at $T_{amb} = 25\text{ }^\circ\text{C}$	4	A
	Drain current (continuous) at $T_{amb} = 100\text{ }^\circ\text{C}$	2.5	
$I_{DM}^{(1)}$	Drain current (pulsed)	16	A
$P_{TOT}$	Total power dissipation at $T_{amb} = 25\text{ }^\circ\text{C}$	1.6	W
$T_{stg}$	Storage temperature range	-55 to 150	$^\circ\text{C}$
$T_J$	Operating junction temperature		

1. Pulse width limited by safe operating area.

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thJA}^{(1)}$	Thermal resistance, junction-to-ambient	78	$^\circ\text{C/W}$

1. When mounted on 1 inch<sup>2</sup> FR-4 board, 2 oz. Cu.,  $t \leq 10\text{ s}$ .

**Note:** For the P-channel Power MOSFET the actual polarity of the voltages and the current must be reversed.

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified)

**Table 3. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ , $I_D = 250\text{ }\mu\text{A}$	30			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 30\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ , $V_{DS} = 30\text{ V}$ , $T_C = 125\text{ °C}^{(1)}$			10	
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 20\text{ V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	1.0		2.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 2\text{ A}$		48	56	m $\Omega$
		$V_{GS} = 4.5\text{ V}$ , $I_D = 2\text{ A}$		75	90	

1. Defined by design, not subject to production test.

**Table 4. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$	-	639	-	pF
$C_{oss}$	Output capacitance		-	79	-	pF
$C_{rSS}$	Reverse transfer capacitance		-	52	-	pF
$Q_g$	Total gate charge	$V_{DD} = 15\text{ V}$ , $I_D = 4\text{ A}$ , $V_{GS} = 4.5\text{ V}$ (see Figure 13. Gate charge test circuit)	-	6	-	nC
$Q_{gs}$	Gate-source charge		-	1.9	-	nC
$Q_{gd}$	Gate-drain charge		-	2.1	-	nC

**Table 5. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 15\text{ V}$ , $I_D = 2\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$ (see Figure 12. Switching times test circuit for resistive load)	-	5.4	-	ns
$t_r$	Rise time		-	5	-	ns
$t_{d(off)}$	Turn-off delay time		-	19.2	-	ns
$t_f$	Fall time		-	3.4	-	ns

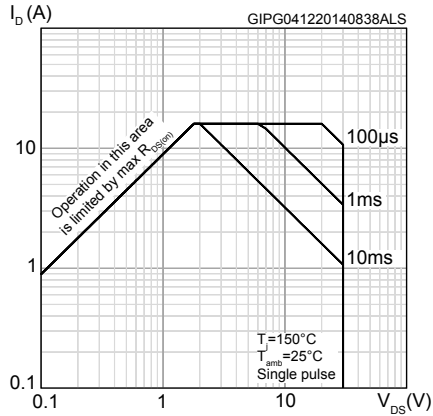
**Table 6. Source-drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 4\text{ A}$ , $V_{GS} = 0\text{ V}$	-		1.1	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 4\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ ,	-	11.2		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 16\text{ V}$ , $T_J = 150\text{ °C}$	-	3.5		nC
$I_{RRM}$	Reverse recovery current	(see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	0.6		A

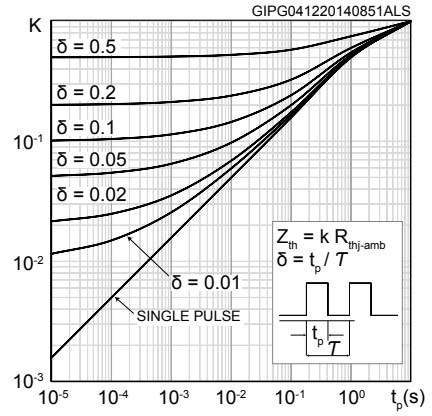
1. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)

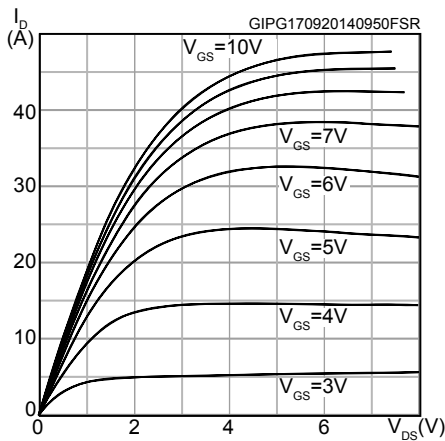
**Figure 1. Safe operating area**



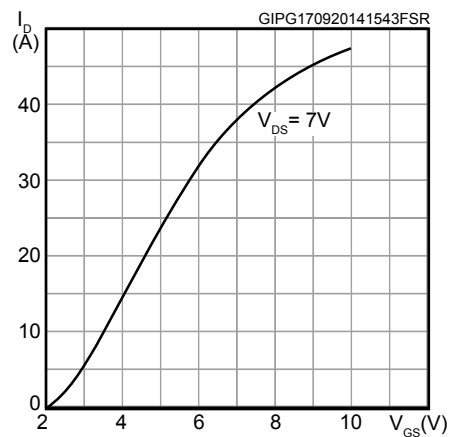
**Figure 2. Normalized transient thermal impedance**



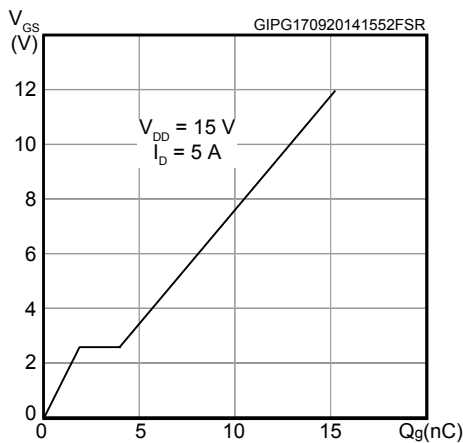
**Figure 3. Typical output characteristics**



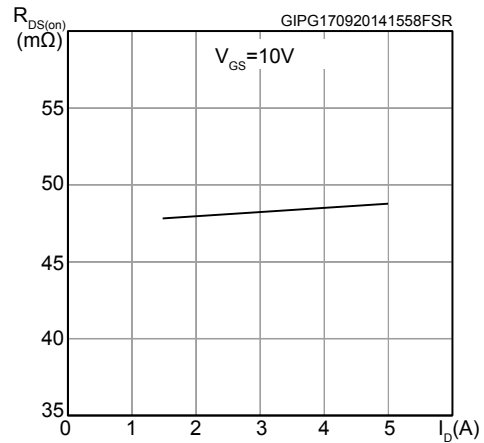
**Figure 4. Typical transfer characteristics**



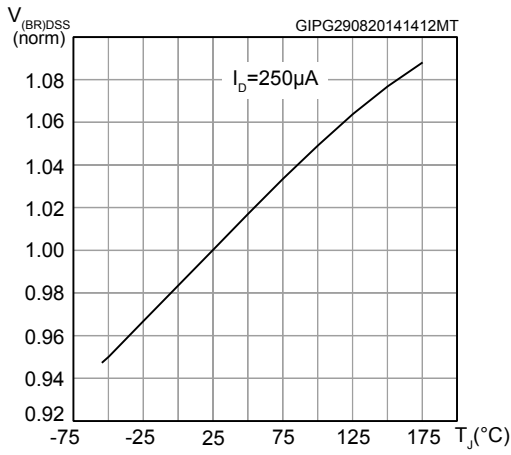
**Figure 5. Typical gate charge vs gate-source voltage**



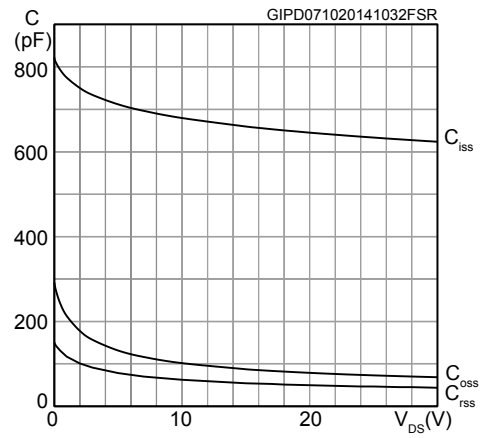
**Figure 6. Typical static drain-source on-resistance**



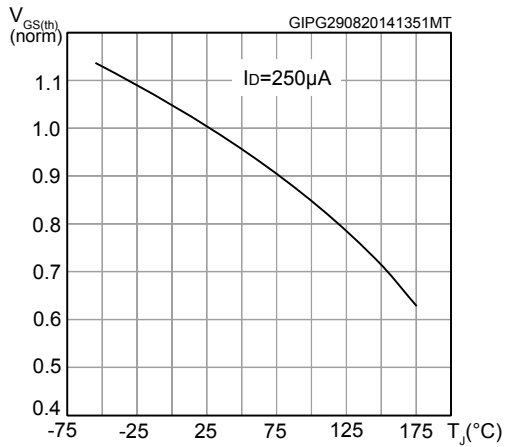
**Figure 7. Normalized breakdown voltage vs temperature**



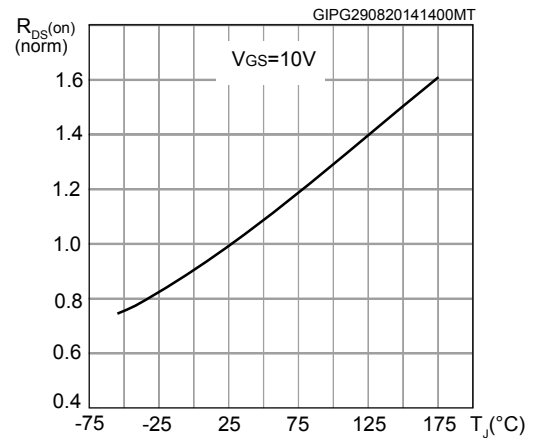
**Figure 8. Typical capacitance characteristics**



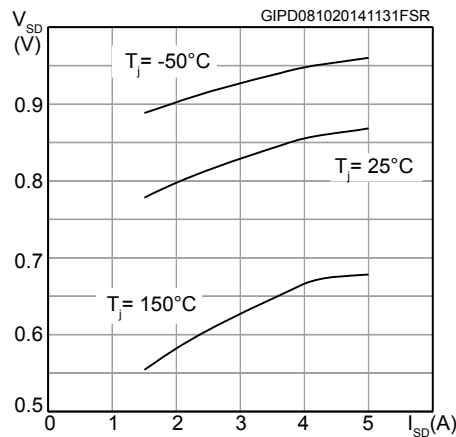
**Figure 9. Normalized gate threshold voltage vs temperature**



**Figure 10. Normalized on-resistance vs temperature**



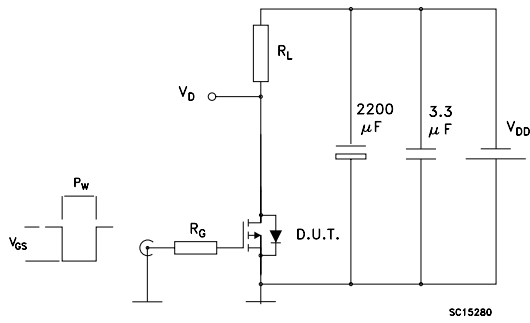
**Figure 11. Typical reverse diode forward characteristics**



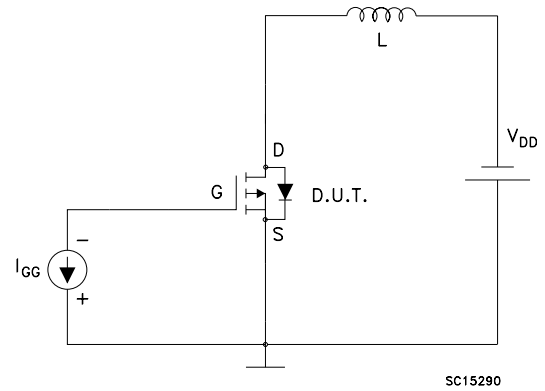
*Note:* For the P-channel Power MOSFET, current and voltage polarities are reversed.

### 3 Test circuits

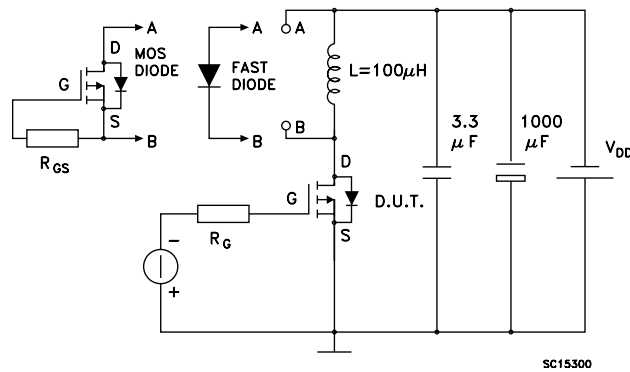
**Figure 12. Switching times test circuit for resistive load**



**Figure 13. Gate charge test circuit**



**Figure 14. Test circuit for inductive load switching and diode recovery times**



## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 4.1 SOT23-6L package information

Figure 15. SOT23-6L package outline

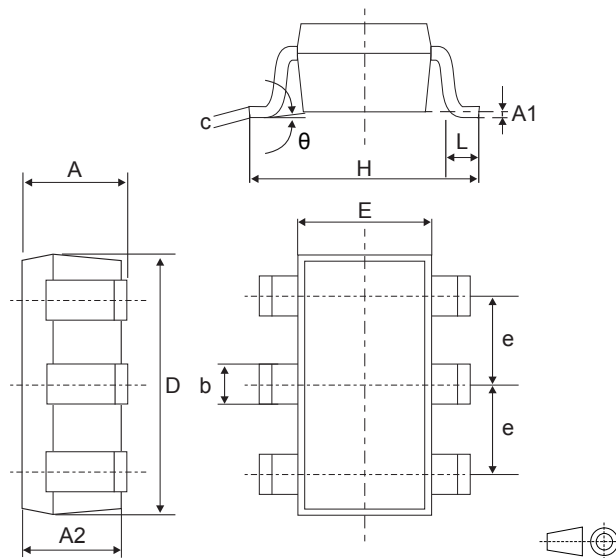
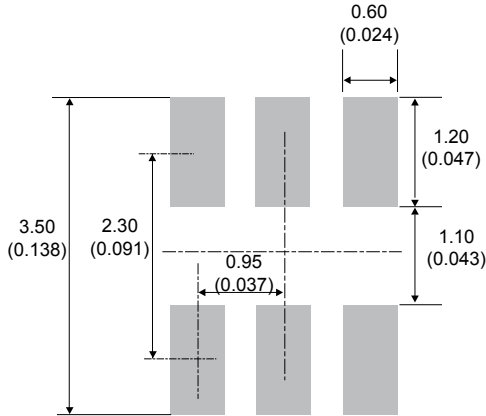


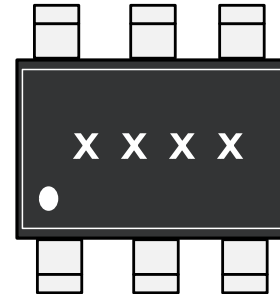
Table 7. SOT23-6L package mechanical data

Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
A			1.25
A1	0		0.15
A2	1.0	1.10	1.20
b	0.36		0.50
C	0.14		0.20
D	2.826	2.926	3.026
E	1.526	1.626	1.726
e	0.90	0.95	1.00
H	2.60	2.80	3.00
L	0.35	0.45	0.60
$\theta$	0		8

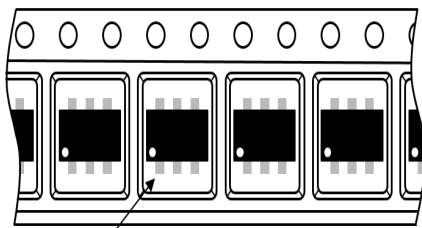
**Figure 16. Footprint recommendations, dimensions in mm (inches)**



**Figure 17. Marking layout (refer to ordering information table for marking)**



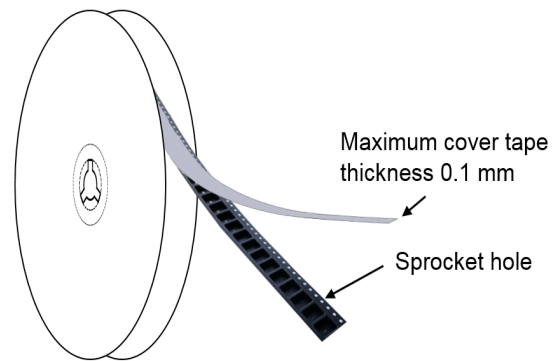
**Figure 18. Package orientation in reel**



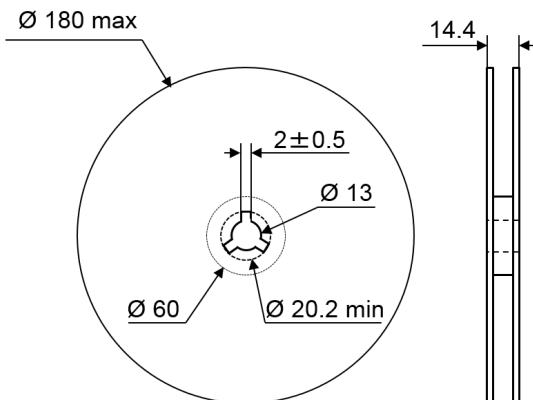
Pin 1 located according to EIA-481

Note: Pocket dimensions are not on scale  
Pocket shape may vary depending on package

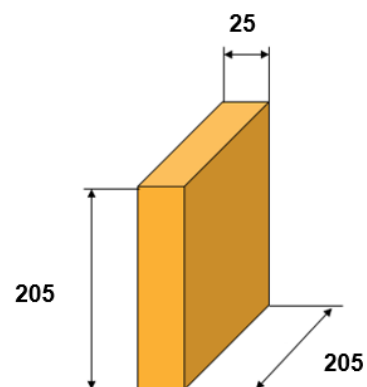
**Figure 19. Tape and reel orientation**



**Figure 20. Reel dimensions (mm)**

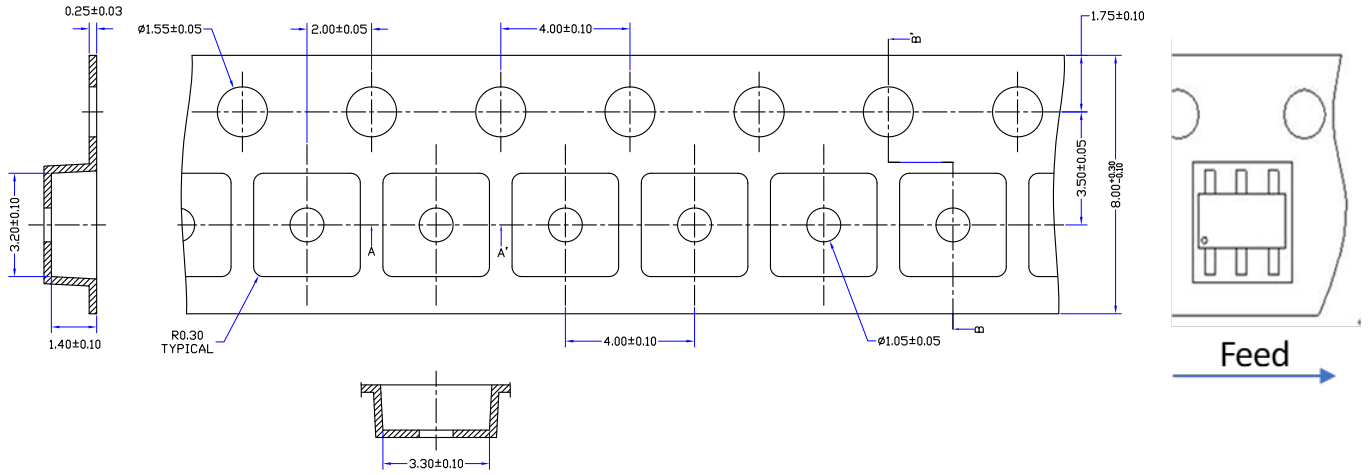


**Figure 21. Inner box dimensions (mm)**



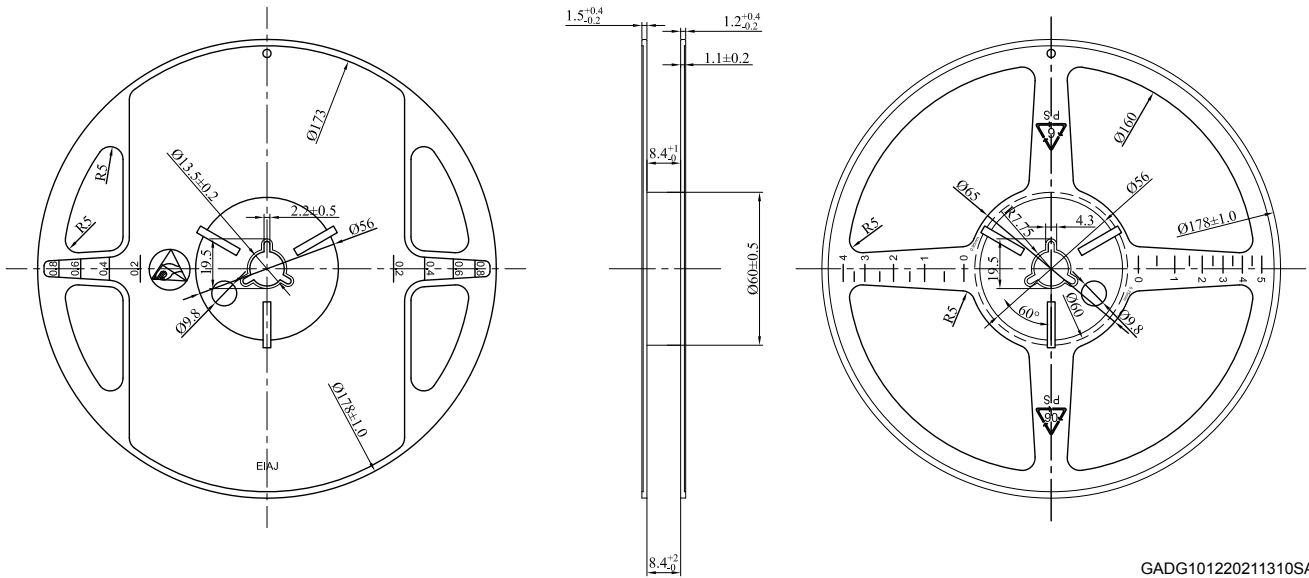


**Figure 22. Tape outline**



GADG101220211254SA

**Figure 23. Reel outline**



GADG101220211310SA

## Revision history

**Table 8. Document revision history**

Date	Version	Changes
09-May-2013	1	First revision.
09-Dec-2014	2	Text edits throughout document On cover page: – changed title description – updated Features – updated Description Updated <i>Table 4</i> In <i>Table 5</i> , changed values and test conditions In <i>Table 6</i> , changed values and test conditions In <i>Table 7</i> , changed values and test conditions Added <i>Section 2.1: Electrical characteristics (curves)</i> Updated <i>Section 3: Test circuits</i> Updated <i>Section 4: Package mechanical data</i>
10-Dec-2021	3	Updated <a href="#">Section 4 Package information</a> . Minor text changes.

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