

N-channel 600 V, 0.14 Ω typ., 20 A MDmesh™ M2 Power MOSFETs in TO-220FP and I²PAKFP packages

Datasheet - production data

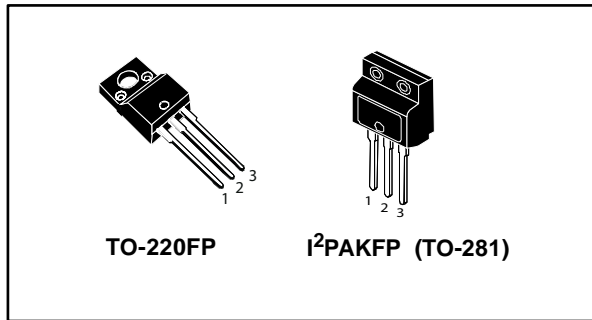
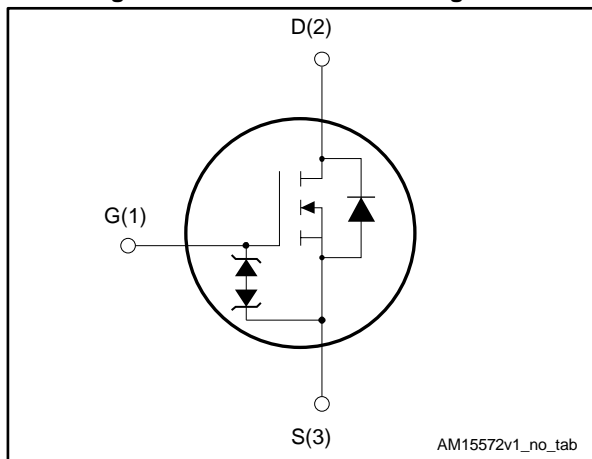


Figure 1: Internal schematic diagram



Features

| Order code | V _{DS} @ T _{Jmax} | R _{DS(on)} max. | I _D | P _{TOT} |
|-------------|-------------------------------------|--------------------------|----------------|------------------|
| STF26N60M2 | 650 V | 0.165 Ω | 20 A | 30 W |
| STF126N60M2 | | | | |

- Extremely low gate charge
- Excellent output capacitance (C_{OSS}) profile
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications
- LCC converters, resonant converters

Description

These devices are N-channel Power MOSFETs developed using MDmesh™ M2 technology. Thanks to their strip layout and improved vertical structure, these devices exhibit low on-resistance and optimized switching characteristics, rendering them suitable for the most demanding high efficiency converters.

Table 1: Device summary

| Order code | Marking | Package | Packing |
|-------------|---------|----------------------|---------|
| STF26N60M2 | 26N60M2 | TO-220FP | Tube |
| STF126N60M2 | | I ² PAKFP | |

Contents

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1 Electrical ratings

Table 2: Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|----------------|---|------------|------------------|
| V_{GS} | Gate-source voltage | ± 25 | V |
| $I_D^{(1)}$ | Drain current (continuous) at $T_{case} = 25\text{ }^\circ\text{C}$ | 20 | A |
| | Drain current (continuous) at $T_{case} = 100\text{ }^\circ\text{C}$ | 13 | |
| $I_{DM}^{(2)}$ | Drain current (pulsed) | 80 | A |
| P_{TOT} | Total dissipation at $T_{case} = 25\text{ }^\circ\text{C}$ | 30 | W |
| $dv/dt^{(3)}$ | Peak diode recovery voltage slope | 15 | V/ns |
| $dv/dt^{(4)}$ | MOSFET dv/dt ruggedness | 50 | |
| V_{ISO} | Insulation withstand voltage (RMS) from all three leads to external heat sink ($t = 1\text{ s}$; $T_C = 25\text{ }^\circ\text{C}$) | 2.5 | kV |
| T_{stg} | Storage temperature | -55 to 150 | $^\circ\text{C}$ |
| T_j | Operating junction temperature | | |

Notes:

- (1) Limited by maximum junction temperature.
 (2) Pulse width is limited by safe operating area.
 (3) $I_{SD} \leq 20\text{ A}$, $di/dt = 400\text{ A}/\mu\text{s}$; $V_{DS(peak)} < V_{(BR)DSS}$, $V_{DD} = 80\% V_{(BR)DSS}$.
 (4) $V_{DS} \leq 480\text{ V}$.

Table 3: Thermal data

| Symbol | Parameter | Value | Unit |
|----------------|-------------------------------------|-------|---------------------------|
| $R_{thj-case}$ | Thermal resistance junction-case | 4.2 | $^\circ\text{C}/\text{W}$ |
| $R_{thj-amb}$ | Thermal resistance junction-ambient | 62.5 | |

Table 4: Avalanche characteristics

| Symbol | Parameter | Value | Unit |
|----------------|---|-------|------|
| $I_{AR}^{(1)}$ | Avalanche current, repetitive or not repetitive | 3.8 | A |
| $E_{AR}^{(2)}$ | Single pulse avalanche energy | 250 | mJ |

Notes:

- (1) Pulse width limited by T_{jmax} .
 (2) starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$.

2 Electrical characteristics

($T_{\text{case}} = 25\text{ °C}$ unless otherwise specified)

Table 5: Static

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------------------------|-----------------------------------|--|------|------|----------|---------------|
| $V_{(\text{BR})\text{DSS}}$ | Drain-source breakdown voltage | $V_{\text{GS}} = 0\text{ V}$, $I_{\text{D}} = 1\text{ mA}$ | 600 | | | V |
| I_{DSS} | Zero gate voltage drain current | $V_{\text{GS}} = 0\text{ V}$, $V_{\text{DS}} = 600\text{ V}$ | | | 1 | μA |
| | | $V_{\text{GS}} = 0\text{ V}$, $V_{\text{DS}} = 600\text{ V}$, $T_{\text{case}} = 125\text{ °C}$ | | | 100 | |
| I_{GSS} | Gate-body leakage current | $V_{\text{DS}} = 0\text{ V}$, $V_{\text{GS}} = \pm 25\text{ V}$ | | | ± 10 | μA |
| $V_{\text{GS(th)}}$ | Gate threshold voltage | $V_{\text{DS}} = V_{\text{GS}}$, $I_{\text{D}} = 250\text{ }\mu\text{A}$ | 2 | 3 | 4 | V |
| $R_{\text{DS(on)}}$ | Static drain-source on-resistance | $V_{\text{GS}} = 10\text{ V}$, $I_{\text{D}} = 10\text{ A}$ | | 0.14 | 0.165 | Ω |

Table 6: Dynamic

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|----------------------------|-------------------------------|--|------|------|------|-------------|
| C_{iss} | Input capacitance | $V_{\text{DS}} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{\text{GS}} = 0\text{ V}$ | - | 1360 | - | pF |
| C_{oss} | Output capacitance | | - | 88 | - | |
| C_{rss} | Reverse transfer capacitance | | - | 2 | - | |
| $C_{\text{oss eq.}}^{(1)}$ | Equivalent output capacitance | $V_{\text{DS}} = 0\text{ to }480\text{ V}$, $V_{\text{GS}} = 0\text{ V}$ | - | 124 | - | pF |
| R_{G} | Intrinsic gate resistance | $f = 1\text{ MHz}$, $I_{\text{D}} = 0\text{ A}$ | - | 4 | - | Ω |
| Q_{g} | Total gate charge | $V_{\text{DD}} = 480\text{ V}$, $I_{\text{D}} = 20\text{ A}$, $V_{\text{GS}} = 10\text{ V}$ (see Figure 15 : "Gate charge test circuit") | - | 34 | - | nC |
| Q_{gs} | Gate-source charge | | - | 5.6 | - | |
| Q_{gd} | Gate-drain charge | | - | 16.3 | - | |

Notes:

⁽¹⁾ $C_{\text{oss eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 7: Switching times

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------------|---------------------|---|------|------|------|-------------|
| $t_{\text{d(on)}}$ | Turn-on delay time | $V_{\text{DD}} = 300\text{ V}$, $I_{\text{D}} = 10\text{ A}$ $R_{\text{G}} = 4.7\text{ }\Omega$, $V_{\text{GS}} = 10\text{ V}$ (see Figure 14 : "Switching times test circuit for resistive load" and Figure 19 : "Switching time waveform") | - | 20.2 | - | ns |
| t_{r} | Rise time | | - | 8 | - | |
| $t_{\text{d(off)}}$ | Turn-off delay time | | - | 66 | - | |
| t_{f} | Fall time | | - | 10 | - | |

Table 8: Source-drain diode

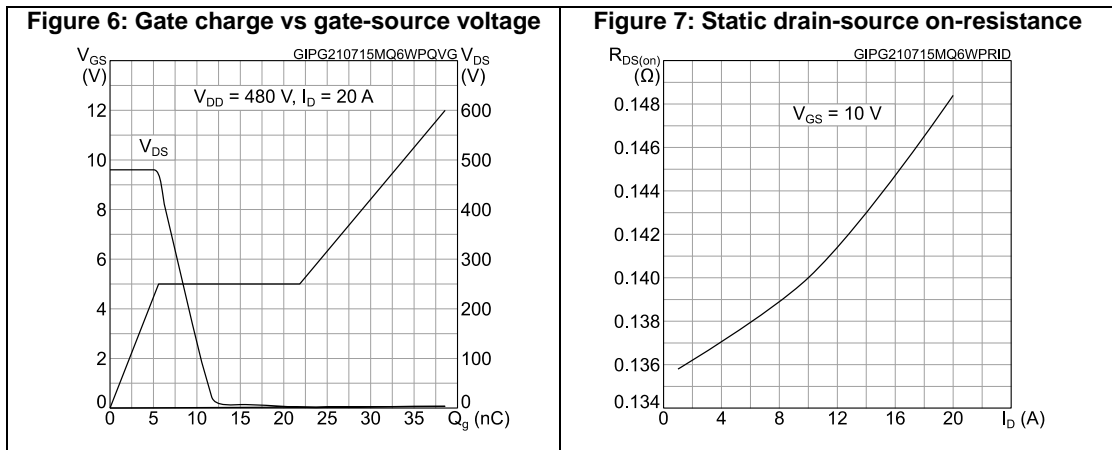
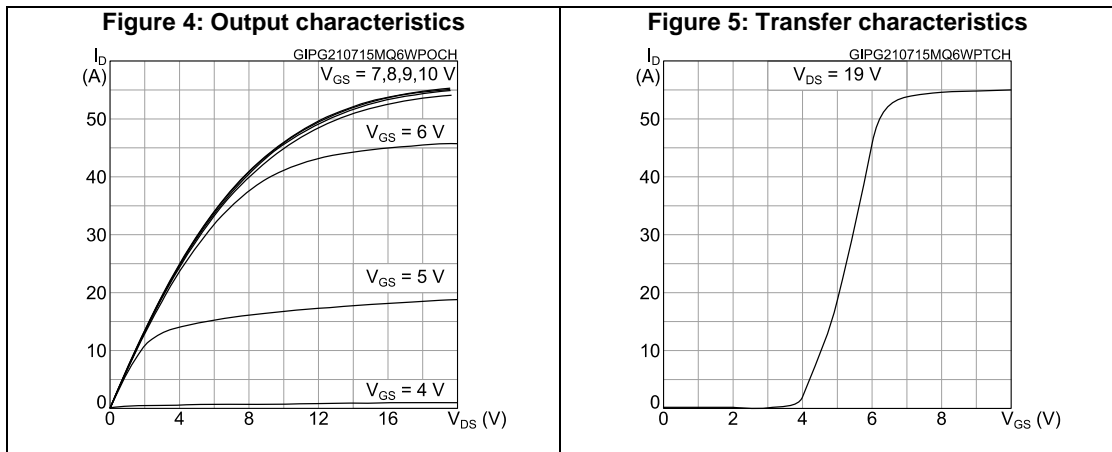
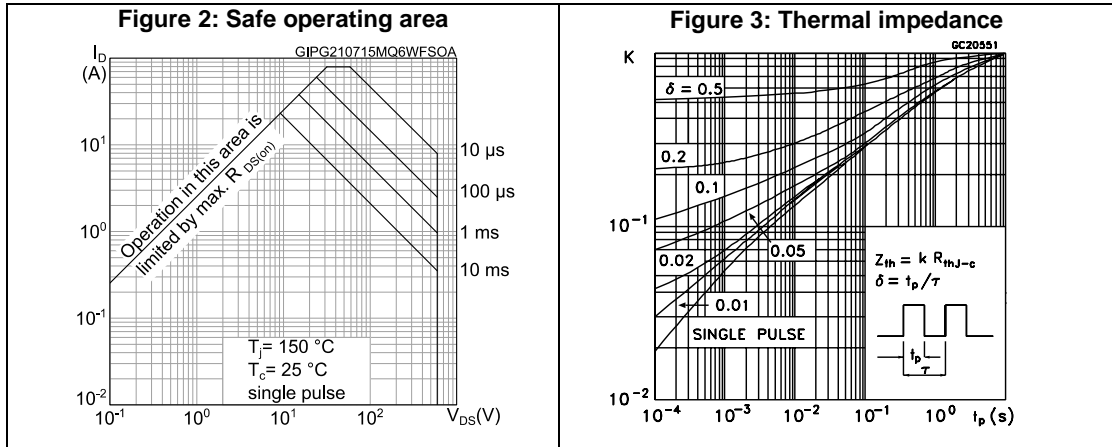
| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------------|-------------------------------|---|------|------|------|---------------|
| I_{SD} | Source-drain current | | - | | 20 | A |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) | | - | | 80 | A |
| $V_{SD}^{(2)}$ | Forward on voltage | $V_{GS} = 0\text{ V}$, $I_{SD} = 20\text{ A}$ | - | | 1.6 | V |
| t_{rr} | Reverse recovery time | $I_{SD} = 20\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$ (see Figure 16 : "Test circuit for inductive load switching and diode recovery times") | - | 360 | | ns |
| Q_{rr} | Reverse recovery charge | | - | 5 | | μC |
| I_{RRM} | Reverse recovery current | | - | 27 | | A |
| t_{rr} | Reverse recovery time | $I_{SD} = 20\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 16 : "Test circuit for inductive load switching and diode recovery times") | - | 556 | | ns |
| Q_{rr} | Reverse recovery charge | | - | 8 | | μC |
| I_{RRM} | Reverse recovery current | | - | 29 | | A |

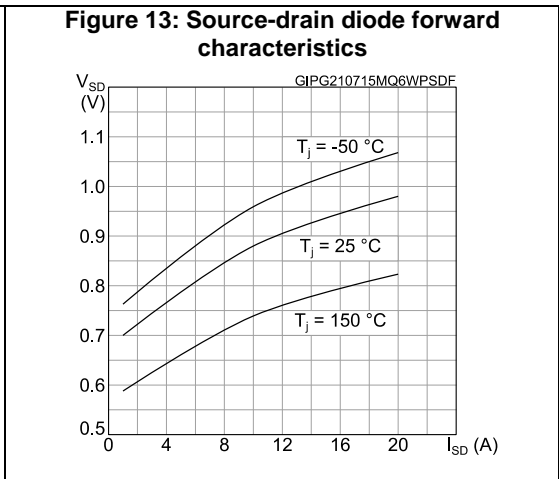
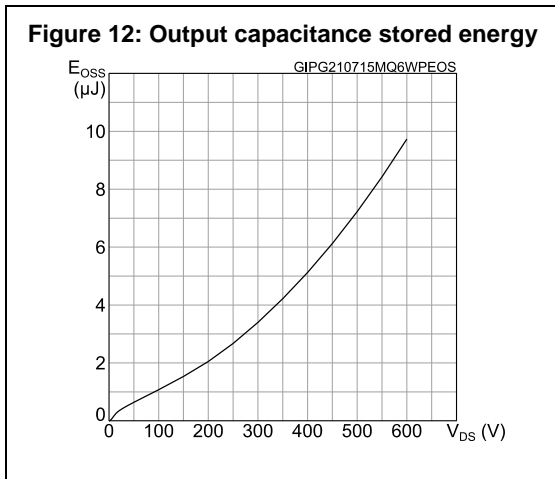
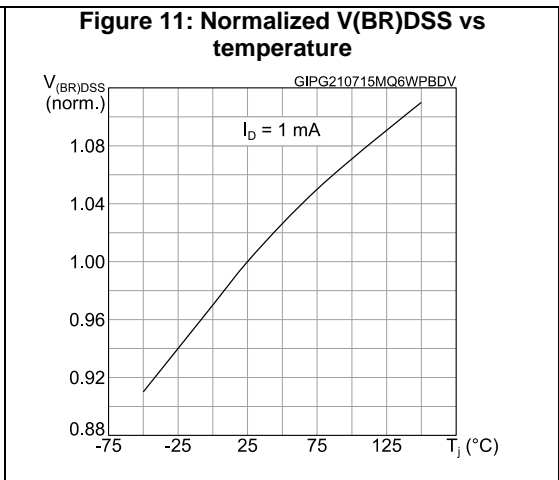
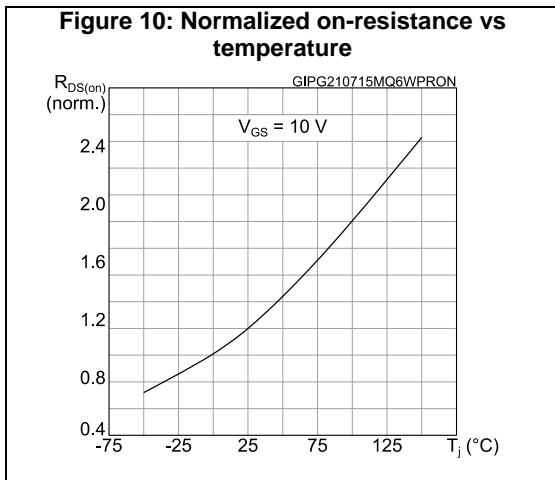
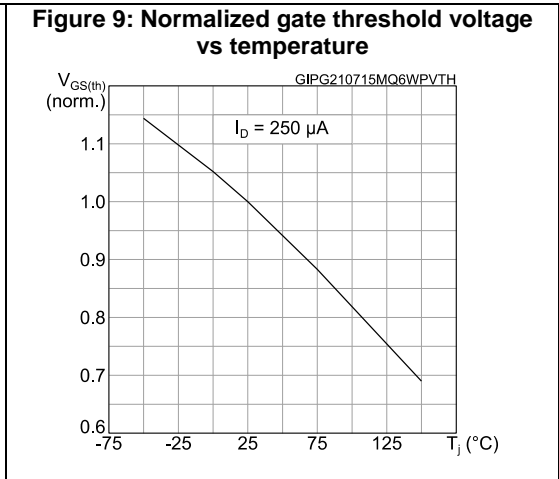
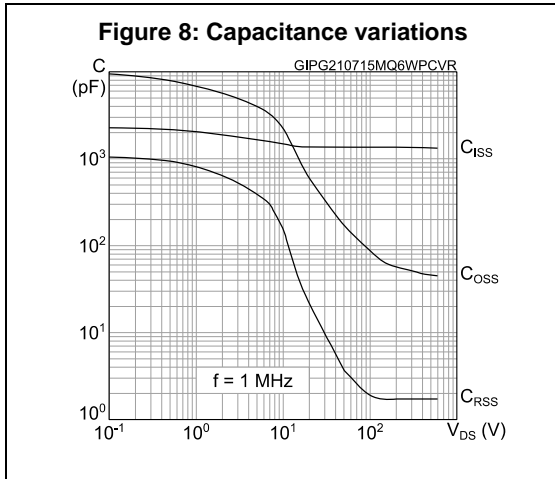
Notes:

(1) Pulse width is limited by safe operating area.

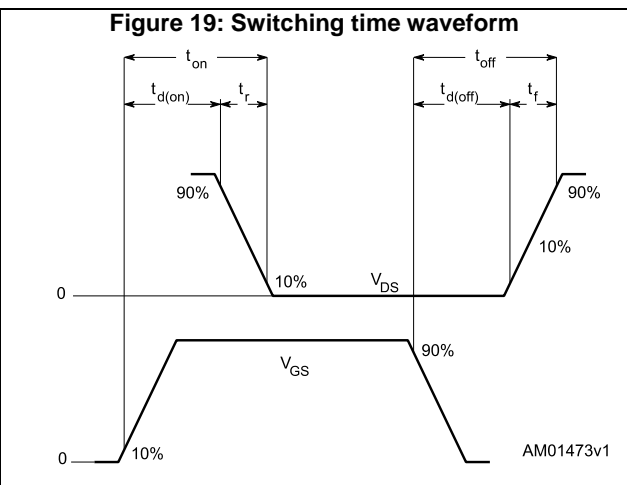
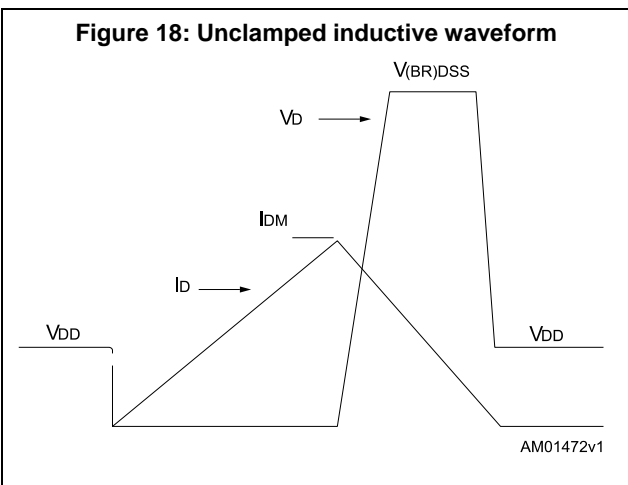
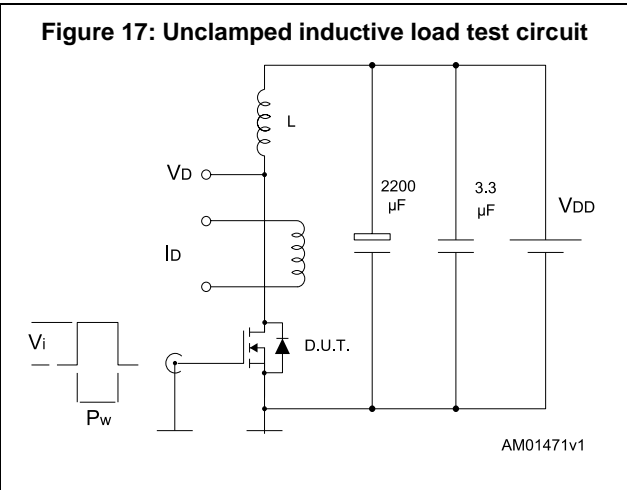
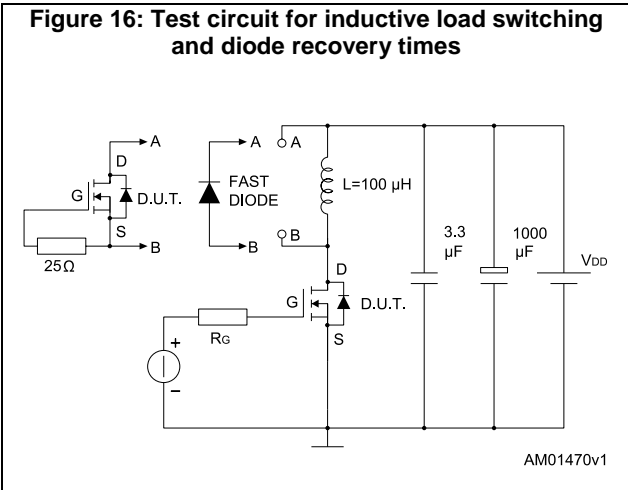
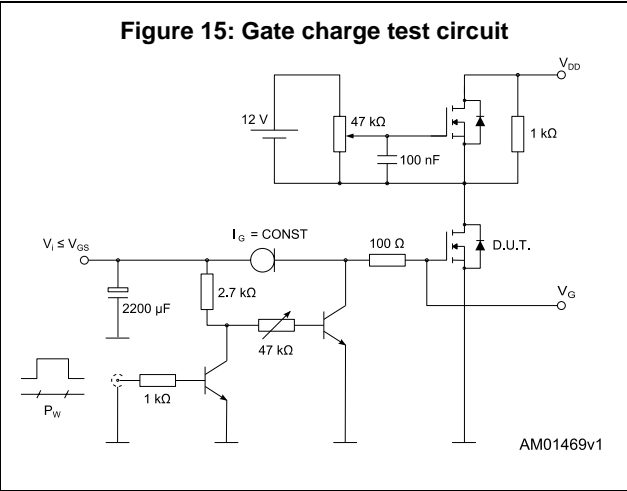
(2) Pulse test: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)





3 Test circuits

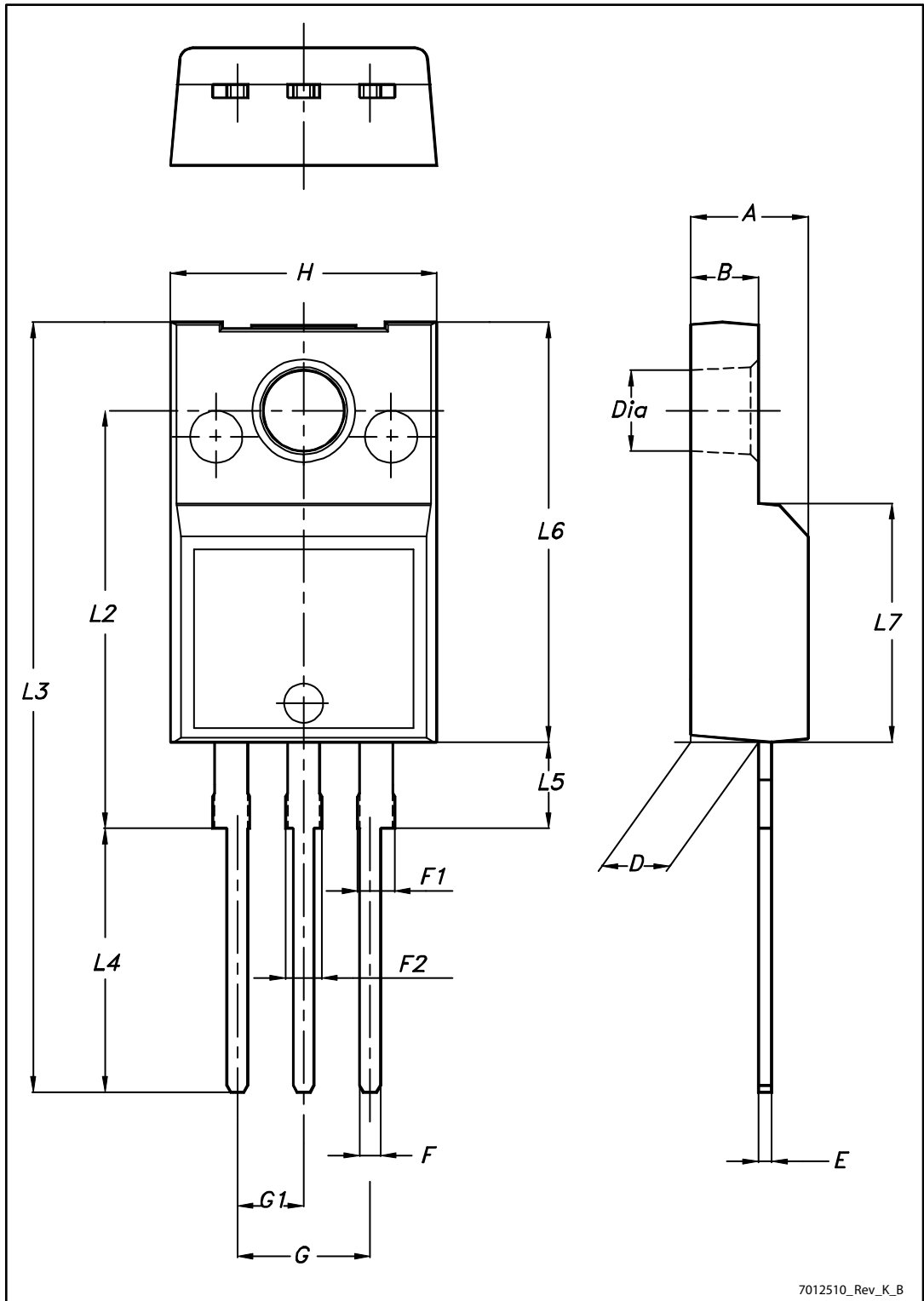


4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

4.1 TO-220FP package information

Figure 20: TO-220FP package outline



7012510_Rev_K_B

Table 9: TO-220FP package mechanical data

| Dim. | mm | | |
|------|------|------|------|
| | Min. | Typ. | Max. |
| A | 4.4 | | 4.6 |
| B | 2.5 | | 2.7 |
| D | 2.5 | | 2.75 |
| E | 0.45 | | 0.7 |
| F | 0.75 | | 1 |
| F1 | 1.15 | | 1.70 |
| F2 | 1.15 | | 1.70 |
| G | 4.95 | | 5.2 |
| G1 | 2.4 | | 2.7 |
| H | 10 | | 10.4 |
| L2 | | 16 | |
| L3 | 28.6 | | 30.6 |
| L4 | 9.8 | | 10.6 |
| L5 | 2.9 | | 3.6 |
| L6 | 15.9 | | 16.4 |
| L7 | 9 | | 9.3 |
| Dia | 3 | | 3.2 |

4.2 I²PAKFP (TO-281) package information

Figure 21: I²PAKFP (TO-281) package outline

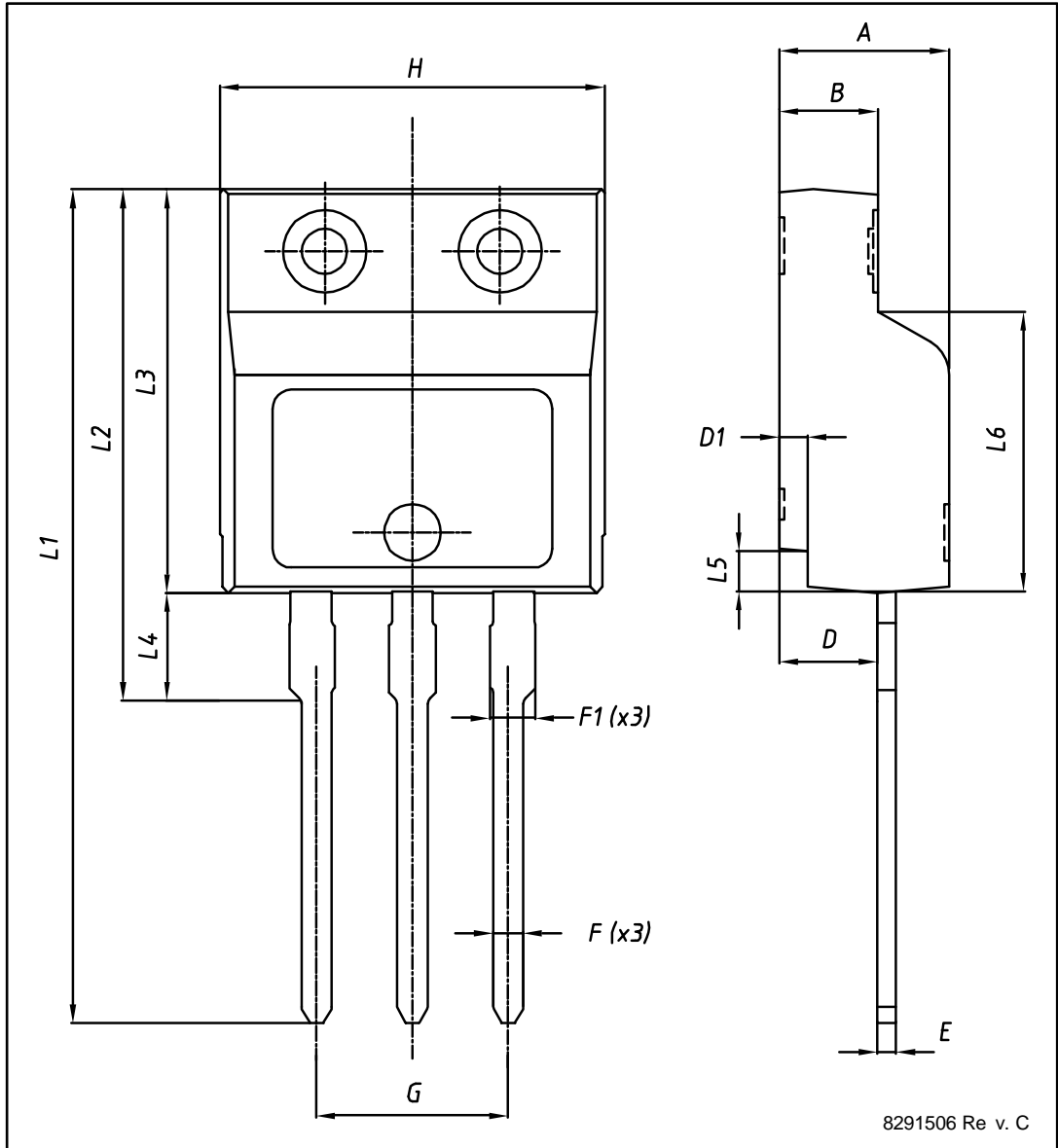


Table 10: I²PAKFP (TO-281) mechanical data

| Dim. | mm | | |
|------|-------|------|-------|
| | Min. | Typ. | Max. |
| A | 4.40 | - | 4.60 |
| B | 2.50 | | 2.70 |
| D | 2.50 | | 2.75 |
| D1 | 0.65 | | 0.85 |
| E | 0.45 | | 0.70 |
| F | 0.75 | | 1.00 |
| F1 | | | 1.20 |
| G | 4.95 | | 5.20 |
| H | 10.00 | | 10.40 |
| L1 | 21.00 | | 23.00 |
| L2 | 13.20 | | 14.10 |
| L3 | 10.55 | | 10.85 |
| L4 | 2.70 | | 3.20 |
| L5 | 0.85 | | 1.25 |
| L6 | 7.50 | 7.60 | 7.70 |

5 Revision history

Table 11: Document revision history

| Date | Revision | Changes |
|--------------|----------|--|
| 05-Mar-2015 | 1 | First release. |
| 30-July-2015 | 2 | Text and formatting changes throughout document Datasheet promoted from preliminary data to production data In Section <i>Electrical characteristics</i> : - updated and renamed table <i>Static</i> (was On/off states) - updated table <i>Dynamic</i> , <i>Switching times</i> and <i>Source-drain diode</i> - added section <i>Electrical characteristics (curves)</i> |

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