

## N-channel 650 V, 0.35 $\Omega$ typ., 12 A MDmesh™ II Power MOSFETs in TO-220FP and I<sup>2</sup>PAKFP packages

Datasheet - production data

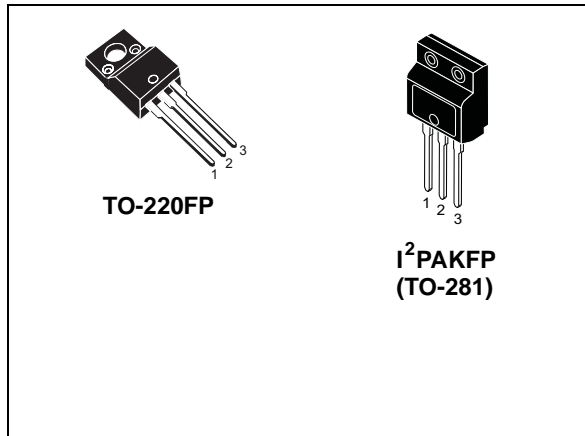
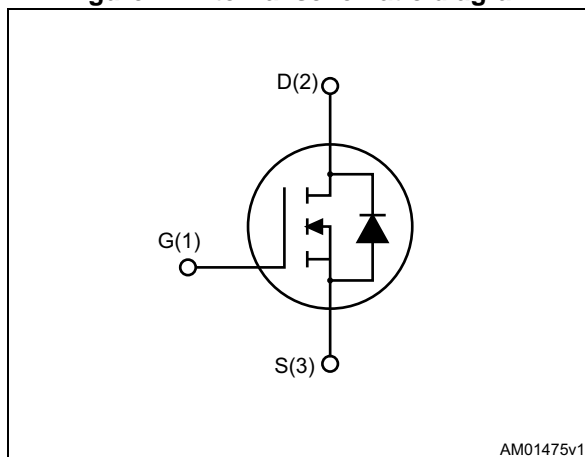


Figure 1. Internal schematic diagram



### Features

Order code	$V_{DSS}$ @ $T_{jmax}$	$R_{DS(on)}$ max.	$I_D$
STF15NM65N	710 V	0.38 $\Omega$	12 A
STFI15NM65N			

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

### Applications

- Switching applications

### Description

These devices are N-channel Power MOSFETs developed using the second generation of MDmesh™ technology. This revolutionary Power MOSFETs associates a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

Table 1. Device summary

Order code	Marking	Packages	Packing
STF15NM65N	15NM65N	TO-220FP	Tube
STFI15NM65N		I <sup>2</sup> PAKFP (TO-281)	

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value		Unit
		TO-220FP	I <sup>2</sup> PAKFP	
V <sub>DS</sub>	Drain source voltage	650		V
V <sub>GS</sub>	Gate source voltage	± 25		V
I <sub>D</sub>	Drain current continuous T <sub>C</sub> = 25 °C	12 <sup>(1)</sup>		A
I <sub>D</sub>	Drain current continuous T <sub>C</sub> = 100 °C	7.56		A
I <sub>DM</sub> <sup>(2)</sup>	Drain current pulsed	48		A
P <sub>TOT</sub>	Total dissipation at T <sub>C</sub> = 25 °C	30		W
dv/dt <sup>(3)</sup>	Peak diode recovery voltage slope	15		V/ns
V <sub>ISO</sub>	Insulation withstand voltage (RMS from all three leads to external heatsink (t = 1 s; T <sub>C</sub> = 25 °C)	2500		V
T <sub>J</sub>	Operating junction temperature range	-55 to 150		°C
T <sub>stg</sub>	Storage temperature range			

1. Limited by maximum junction temperature.

2. Pulse width limited by safe operating area.

3. ISD ≤ 12 A, di/dt ≤ 400 A/μs, V<sub>D</sub>Speak ≤ V<sub>(BR)DSS</sub>, V<sub>DD</sub> = 80 % V<sub>(BR)DSS</sub>

**Table 3. Thermal data**

Symbol	Parameters	Value		Unit
		TO-220FP	I <sup>2</sup> PAKFP	
R <sub>thjc</sub>	Thermal resistance junction-case	4.17		°C/W
R <sub>thj-amb</sub>	Thermal resistance junction-ambient	62.5		°C/W

**Table 4. Avalanche characteristics**

Symbol	Parameters	Value	Unit
I <sub>AS</sub>	Avalanche current, repetitive or not-repetitive (pulse width limited by T <sub>Jmax</sub> )	3	A
E <sub>AS</sub>	Single pulse avalanche energy (starting T <sub>J</sub> = 25 °C, I <sub>D</sub> = I <sub>AR</sub> , V <sub>DD</sub> = 50 V)	187	mJ

## 2 Electrical characteristics

( $T_{CASE} = 25\text{ °C}$  unless otherwise specified).

**Table 5. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0, I_D = 1\text{ mA}$	650			V
$I_{DSS}$	Zero gate voltage drain current	$V_{DD} = 650\text{ V}, V_{GS} = 0$			1	$\mu\text{A}$
		$V_{DD} = 650\text{ V}, V_{GS} = 0$ $T_C = 125\text{ °C}^{(1)}$			100	$\mu\text{A}$
$I_{GSS}$	Gate body leakage	$V_{GS} = \pm 25\text{ V}, V_{DS} = 0\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$I_D = 250\text{ }\mu\text{A}, V_{GS} = V_{DS}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	$I_D = 6\text{ A}, V_{GS} = 10\text{ V}$		0.35	0.38	$\Omega$

1. Defined by design, not subject to production test

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Ma.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 50\text{ V}, f = 1\text{ MHz},$ $V_{GS} = 0\text{ V}$	-	983	-	pF
$C_{oss}$	Output capacitance		-	57	-	pF
$C_{rss}$	Reverse capacitance		-	4.5	-	pF
$C_{osseq}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ V to } 520\text{ V}, V_{GS} = 0\text{ V}$	-	146	-	pF
$R_g$	Intrinsic gate resistance	$f = 1\text{ MHz } I_D = 0\text{ A}$	-	4.6	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 520\text{ V}, I_D = 12\text{ A},$ $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 13: Gate charge test circuit</a> )	-	33.3	-	nC
$Q_{gs}$	Gate source charge		-	5.7	-	nC
$Q_{gd}$	Gate-drain charge		-	17	-	nC

1. Cross eq: defined as a constant equivalent capacitance giving the same charging time as  $C_{OSS}$  when  $V_{DS}$  increases from 0 to 80 %  $V_{DSS}$ .

**Table 7. Switching times**

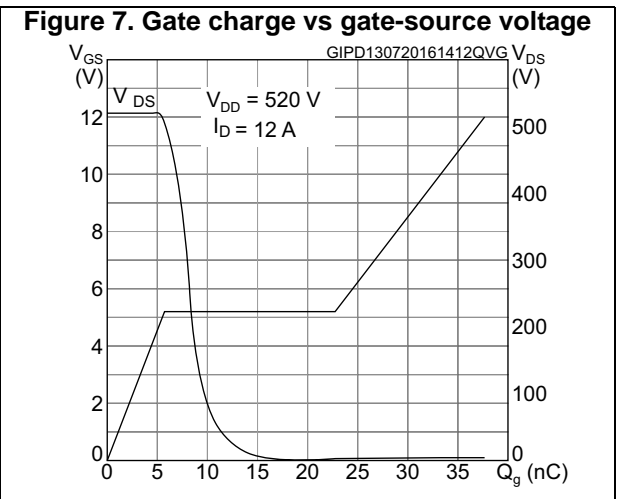
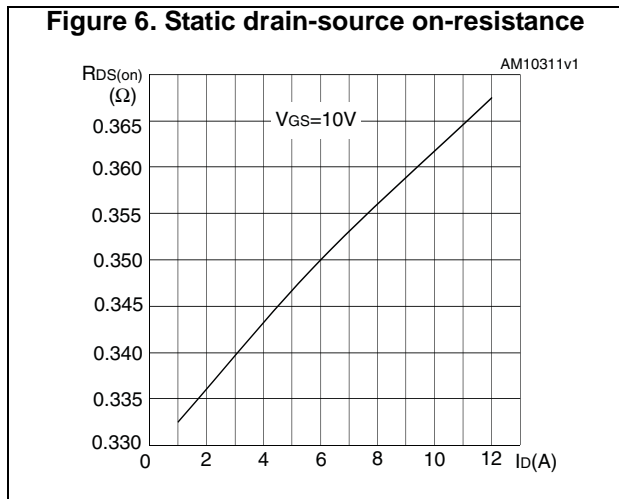
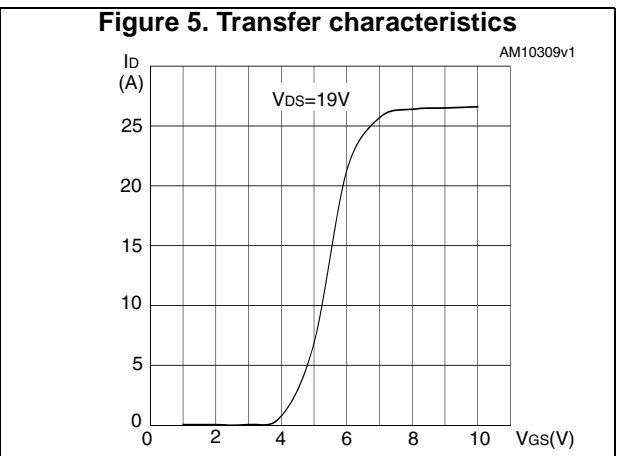
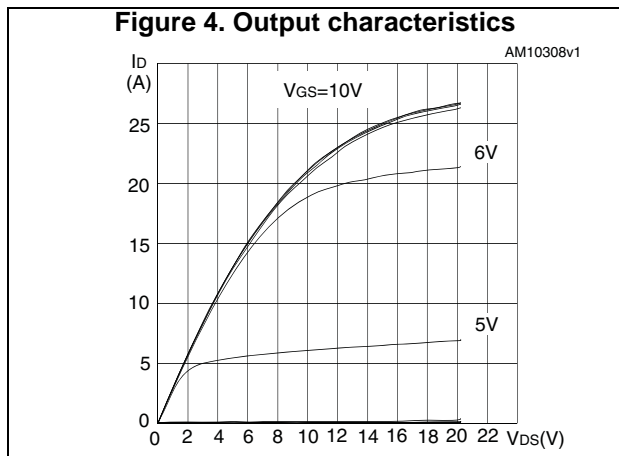
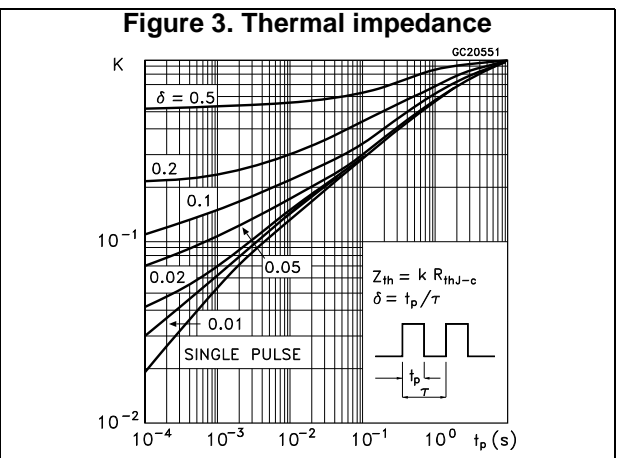
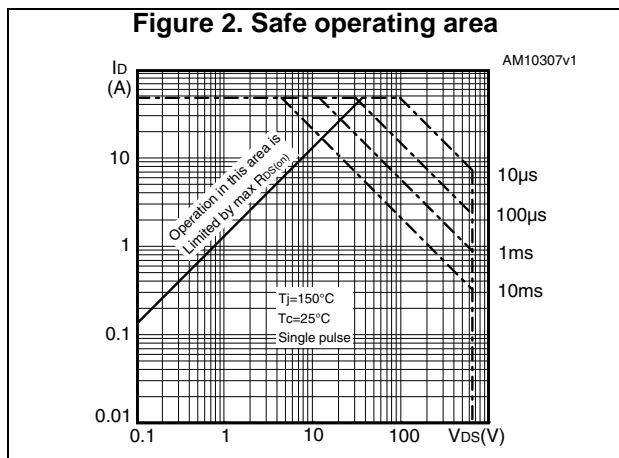
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 325\text{ V}, I_D = 6\text{ A}$ $R_g = 4.7\text{ }\Omega, V_{GS} = 10\text{ V}$ (see <a href="#">Figure 12: Switching times test circuit for resistive load</a> and <a href="#">Figure 17: Switching time waveform</a> )	-	55.5	-	ns
$t_r$	Rise time		-	8.5	-	ns
$t_{d(off)}$	Turn-off-delay time		-	14	-	ns
$t_f$	Fall time		-	11.4	-	ns

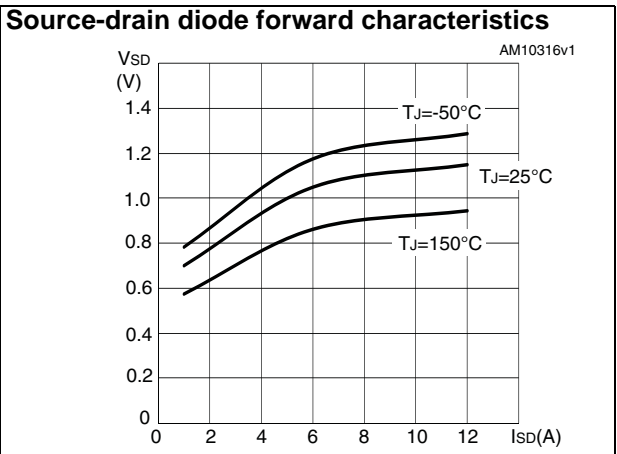
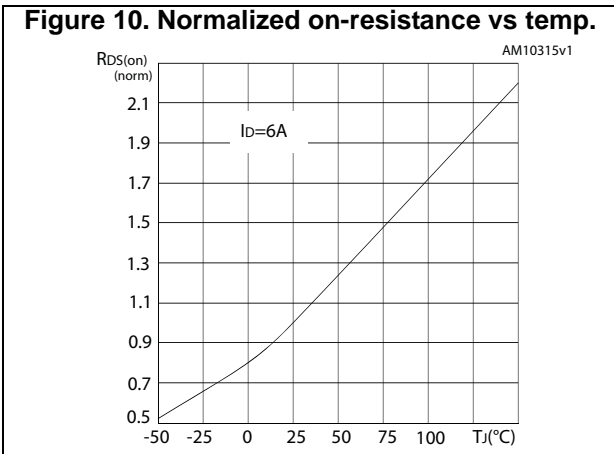
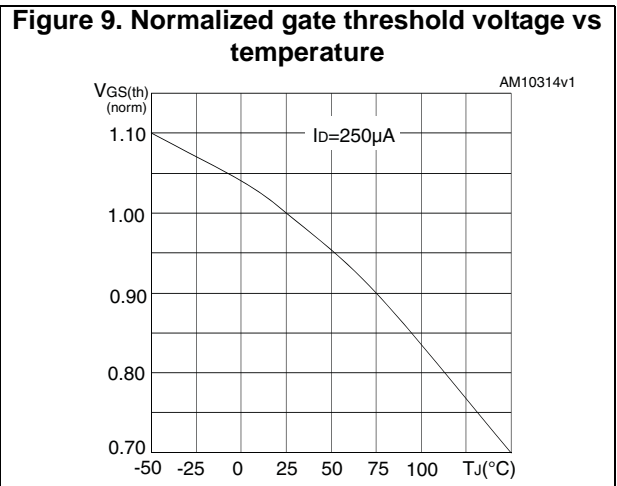
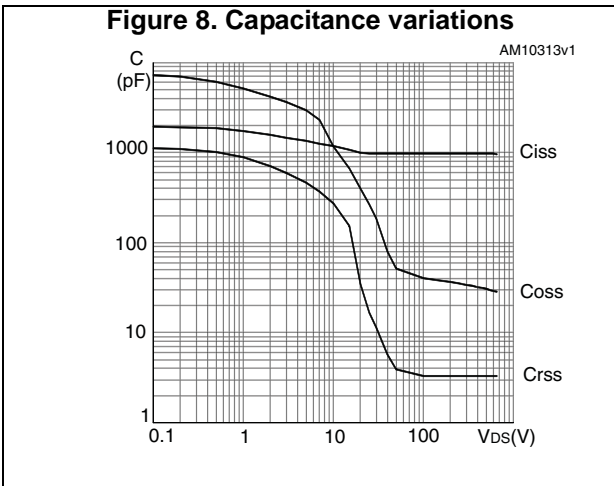
Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source drain current		-		12	A
$I_{SDM}^{(1)}$	Source drain current (pulsed)		-		48	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 12 \text{ A}$ , $V_{GS} = 0 \text{ V}$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 12 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}$ (see <a href="#">Figure 14: Test circuit for inductive load switching and diode recovery times</a> )	-	428		ns
$Q_{rr}$	Reverse recovery charge		-	4.7		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	21.5		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 12 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}$ , $T_j = 150 \text{ }^\circ\text{C}$ (see <a href="#">Figure 14: Test circuit for inductive load switching and diode recovery times</a> )	-	570		ns
$Q_{rr}$	Reverse recovery charge		-	6.2		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	22		A

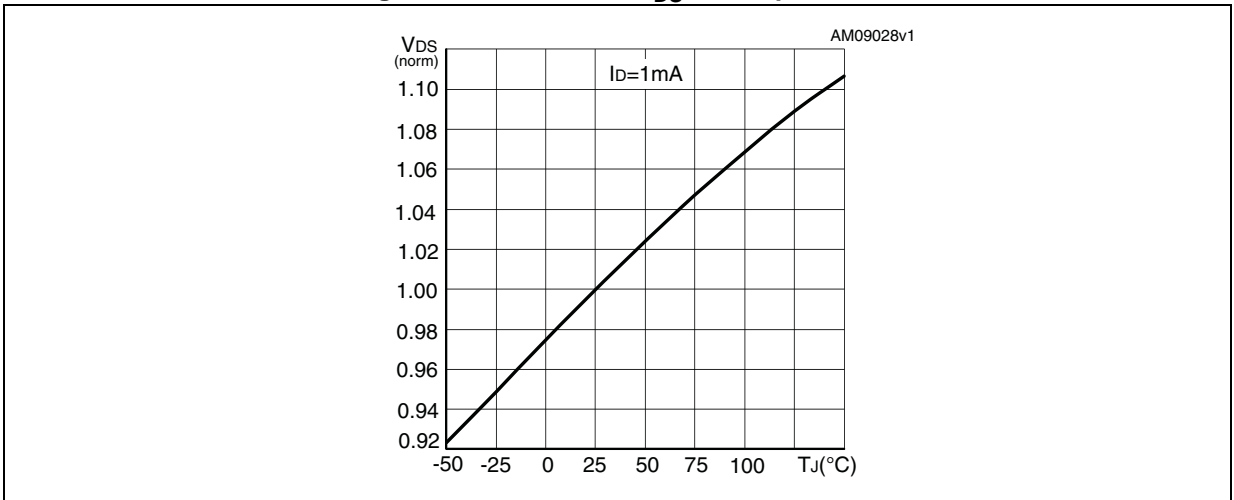
1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %

## 2.1 Electrical characteristics (curves)





**Figure 11. Normalized  $V_{DS}$  vs temperature**



### 3 Test circuits

Figure 12. Switching times test circuit for resistive load

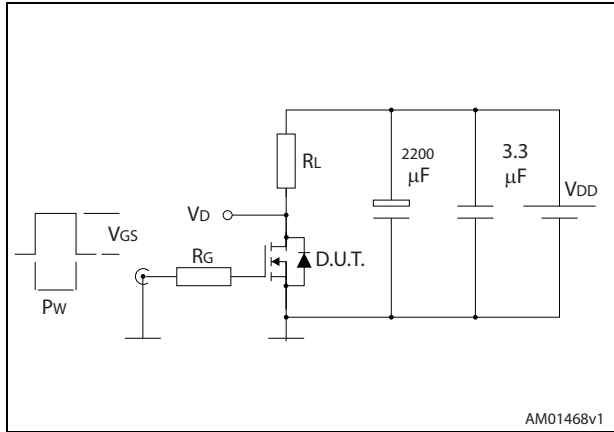


Figure 13. Gate charge test circuit

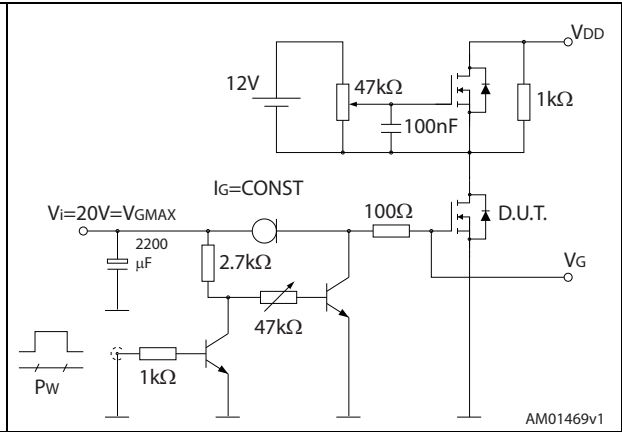


Figure 14. Test circuit for inductive load switching and diode recovery times



Figure 15. Unclamped inductive load test circuit



Figure 16. Unclamped inductive waveform



Figure 17. Switching time waveform



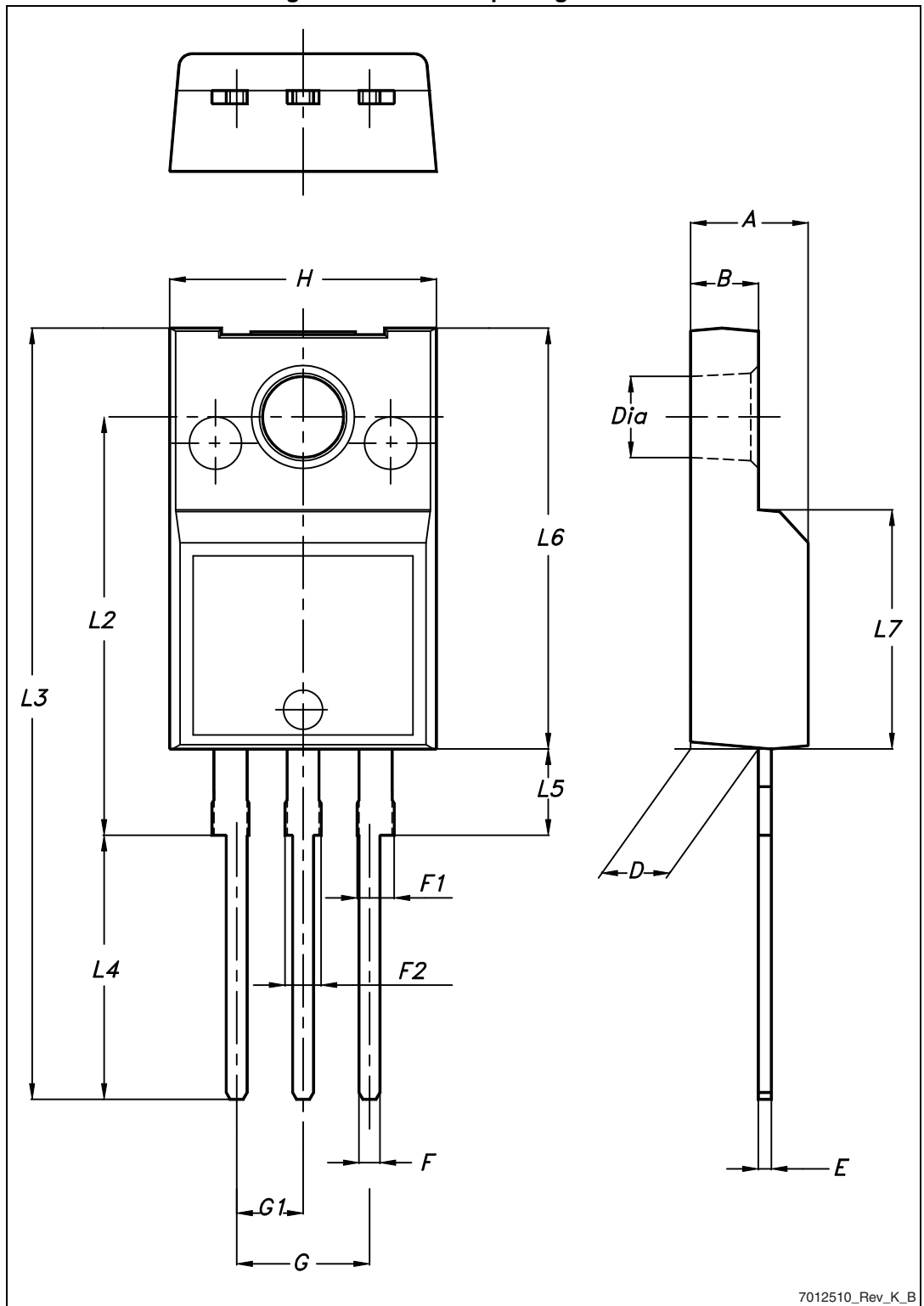


## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

### 4.1 TO-220FP package information

Figure 18. TO-220FP package outline



7012510\_Rev\_K\_B

Table 9. TO-220FP package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

### 4.2 I<sup>2</sup>PAKFP (TO-281) package information

Figure 19. I<sup>2</sup>PAKFP (TO-281) package outline

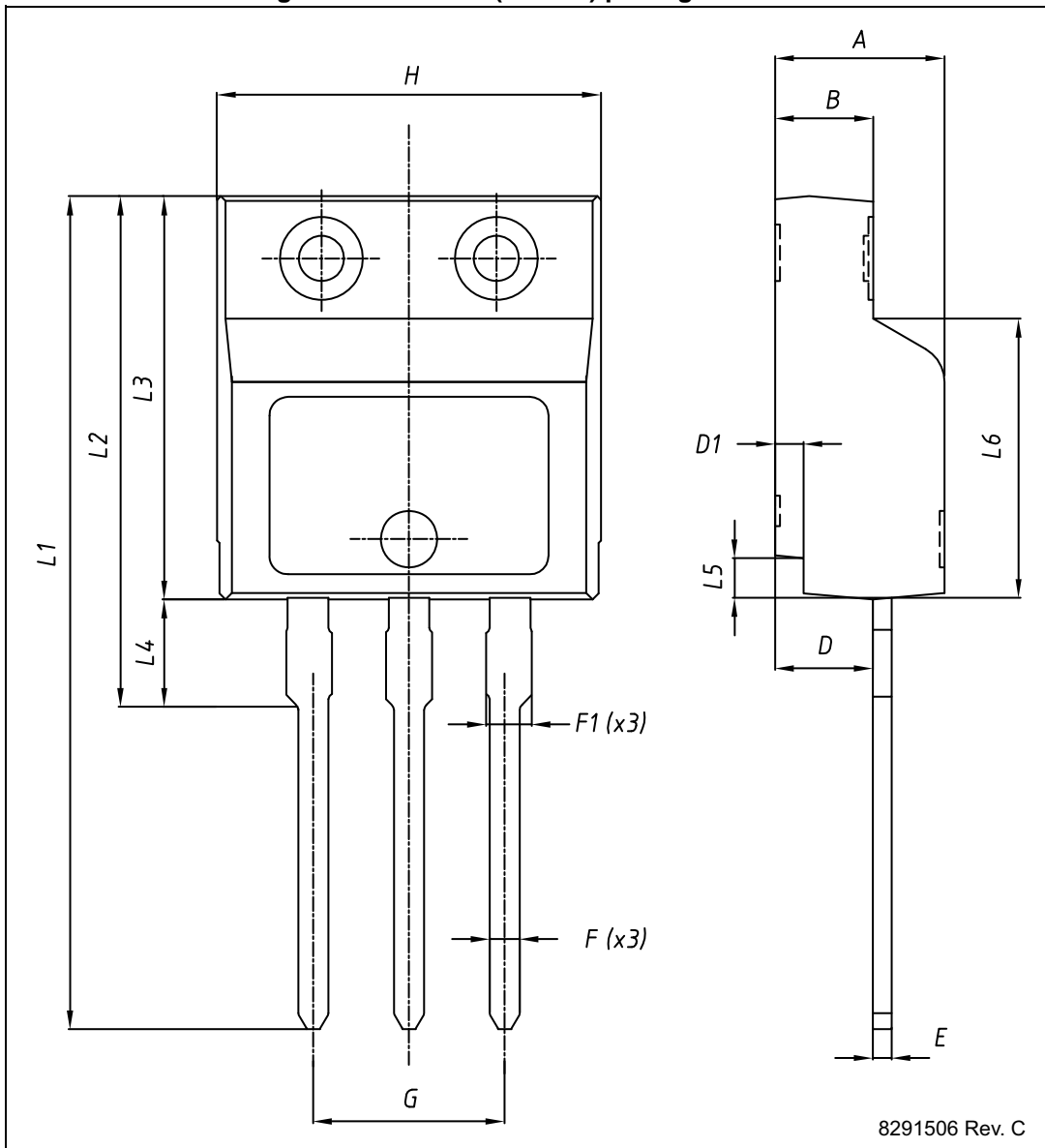


Table 10. I<sup>2</sup>PAKFP (TO-281) package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
D1	0.65		0.85
E	0.45		0.70
F	0.75		1.00
F1			1.20
G	4.95		5.20
H	10.00		10.40
L1	21.00		23.00
L2	13.20		14.10
L3	10.55		10.85
L4	2.70		3.20
L5	0.85		1.25
L6	7.50	7.60	7.70

## 5 Revision history

Table 11. Document revision history

Date	Revision	Changes
11-May-2011	1	Initial release.
21-Jun-2011	2	Document status promoted from preliminary data to datasheet, added Section 2.1: Electrical characteristics (curves).
17-Jul-2013	3	<ul style="list-style-type: none"><li>– Added: I<sup>2</sup>PAKFP package</li><li>– Added: <i>Table 10</i> and <i>Figure 22</i></li><li>– Updated: <i>Section 4: Package information</i></li><li>– Minor text changes.</li></ul>
25-Jul-2016	4	The part number STF15NM65N has been moved to a separate datasheet. Minor text changes.

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