

## Bidirectional Transil™ array for data line protection

### Features

- High surge capability Transil array:  
 $I_{PP} = 40 \text{ A (8/20 } \mu\text{s)}$
- Peak pulse power: 300 W (8/20  $\mu\text{s}$ )
- Up to 5 bidirectional Transil functions
- Low clamping factor ( $V_{CL} / V_{BR}$ ) at high current level
- Low leakage current
- ESD protection up to 15 kV

### Complies with the following standards

- IEC 61000-4-2 level 4
  - 15 kV (air discharge)
  - 8 kV (contact discharge)
- MIL STD 883G- Method 3015-7: class 3B
  - 25 kV (human body model)

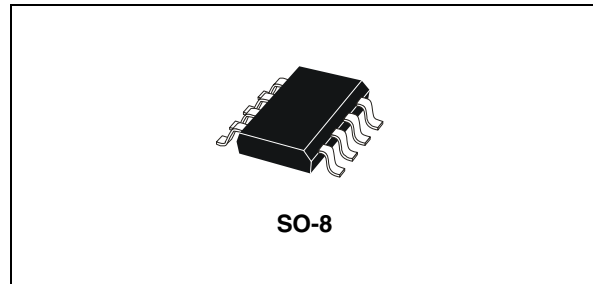
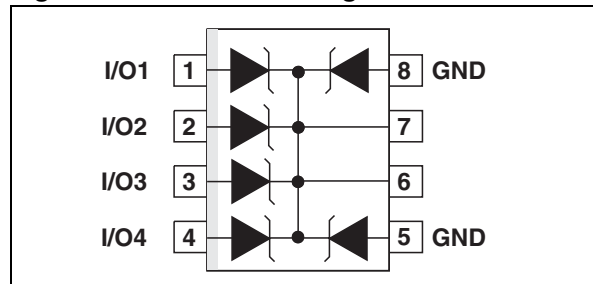


Figure 1. Functional diagram



### Applications

Differential data transmission line protection, such as:

- RS-232
- RS-423
- RS-422
- RS-485

### Description

Transil diode arrays provide high overvoltage protection by clamping action. Their instantaneous response to transient overvoltages makes them particularly suited to protect voltage sensitive devices such as MOS technology and low voltage supplied IC's.

The ITA series combines high surge capability against energetic pulses with high voltage performance against ESD.

TM: Transil is a trademark of STMicroelectronics

# 1 Characteristics

**Table 1. Absolute ratings ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ )**

Symbol	Parameter		Value	Unit
$P_{PP}$	Peak pulse power (8/20 $\mu\text{s}$ ) <sup>(1)</sup>	$T_j$ initial = $T_{amb}$	300	W
$I_{PP}$	Peak pulse current (8/20 $\mu\text{s}$ ) <sup>(1)</sup>	$T_j$ initial = $T_{amb}$	40	A
$I^2t$	Wire $I^2t$ value <sup>(1)</sup>		0.6	$\text{A}^2\text{s}$
$T_j$	Maximum operating junction temperature		125	$^{\circ}\text{C}$
$T_{stg}$	Storage temperature range		-55 to +150	$^{\circ}\text{C}$
$T_L$	Maximum lead temperature for soldering during 10 s at 5 mm for case		260	$^{\circ}\text{C}$

1. For surges greater than the specified maximum value, the I/O will first present a short-circuit and after an open circuit caused by the wire melting.

**Table 2. Electrical characteristics ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ )**

Symbol	Parameter									
$V_{RM}$	Stand-off voltage									
$V_{BR}$	Breakdown voltage									
$V_{CL}$	Clamping voltage									
$I_{RM}$	Leakage current									
$I_{PP}$	Peak pulse current									
$\alpha T$	Voltage temperature coefficient									
C	Capacitance									
Order code	$V_{BR}$ @ $I_R$		$I_{RM}$ @ $V_{RM}$		$V_{CL}$ @ $I_{PP}$		$V_{CL}$ @ $I_{PP}$		$\alpha T$	C
	min.		max.		8/20 $\mu\text{s}$		max. 8/20 $\mu\text{s}$		max.	max.
	(1)		$\mu\text{A}$	V	(1)	A	(1)	A	$10^{-4}/^{\circ}\text{C}$	(2)
	V	mA	$\mu\text{A}$	V	V	A	V	A	$10^{-4}/^{\circ}\text{C}$	pF
ITA6V5B1	6.5	1	10	5	10	10	12	25	4	750
ITA10B1	10	1	4	8	15	10	19	25	8	570
ITA18B1	18	1	4	15	25	10	28	25	9	350
ITA25B1	25	1	4	24	33	10	38	25	12	300

1. Between I/O pin and ground.
2. Between two input pins at 0 V Bias, F = 1 MHz.

Figure 2. Pulse waveform

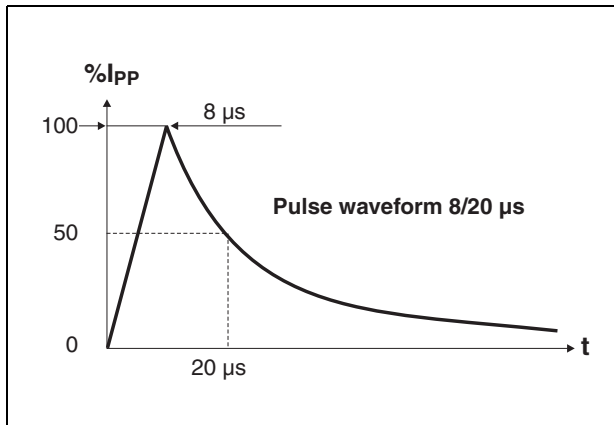


Figure 3. Typical peak pulse power versus exponential pulse duration

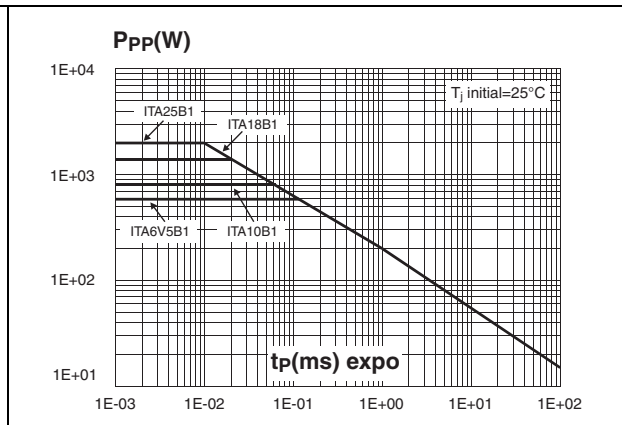


Figure 4. Clamping voltage versus peak pulse current (exponential waveform 8/20 μs)

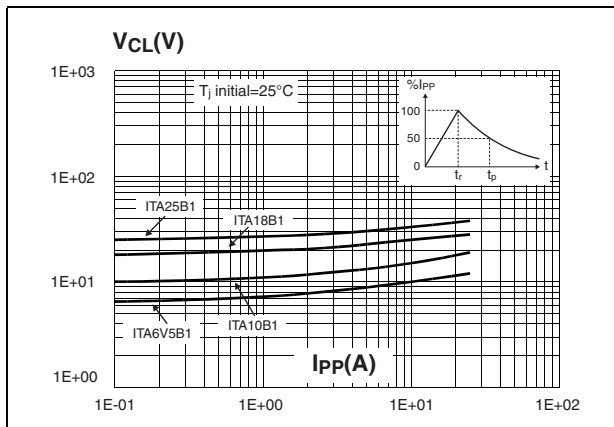


Figure 5. Peak current Idc inducing open circuit of the wire for one input/output versus pulse duration (typical values)

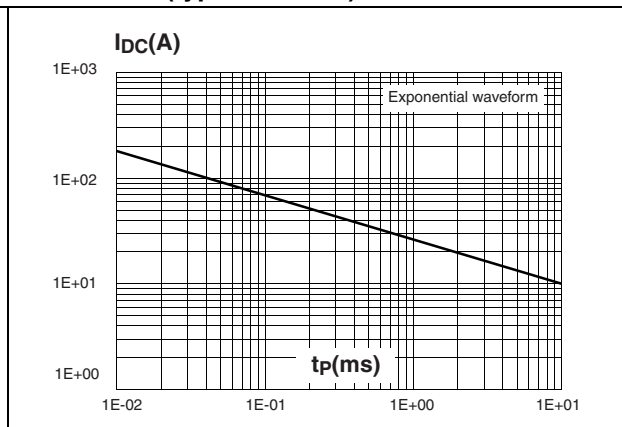


Figure 6. Junction capacitance versus reverse applied voltage for one input/output (typical values)

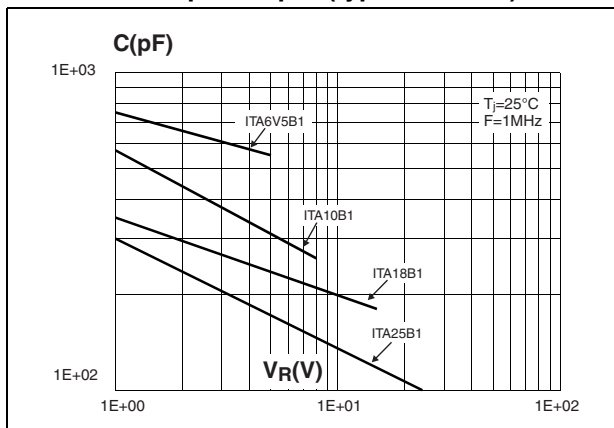
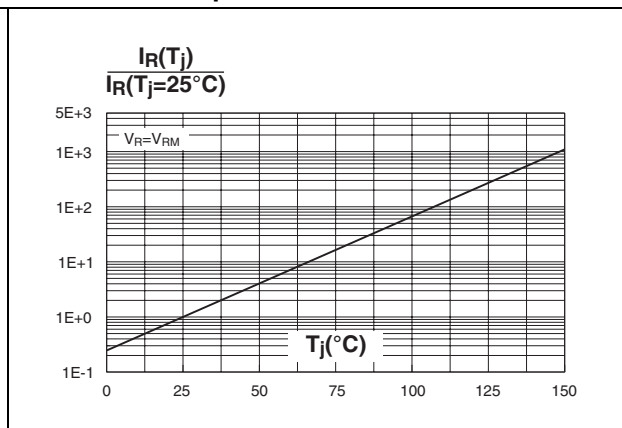


Figure 7. Relative variation of leakage current versus junction temperature



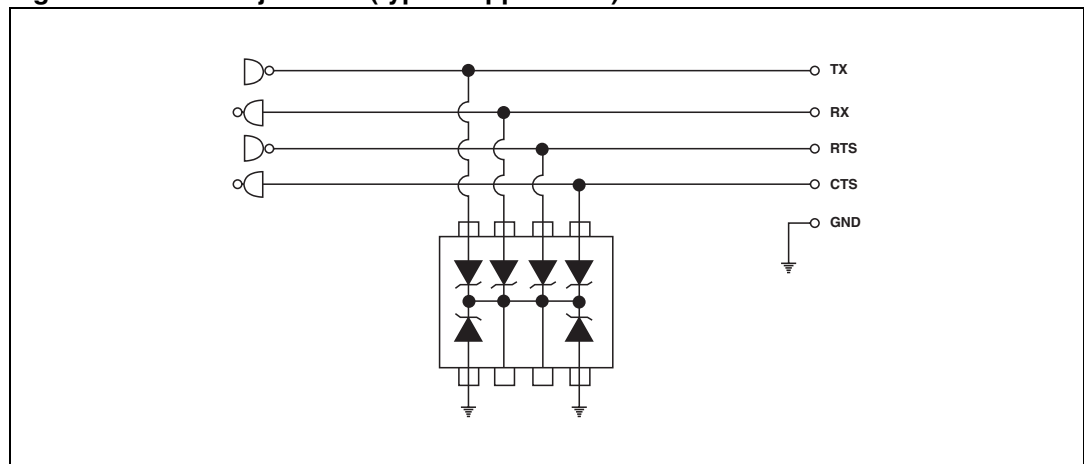
## 2 Application information

This monolithic Transil Array is based on 6 unidirectional Transils with a common cathode and can be configured to offer up to 5 bidirectional functions. This imposes a maximum differential voltage between 2 input pins (see [Table 3](#)).

**Table 3. Maximum differential voltages**

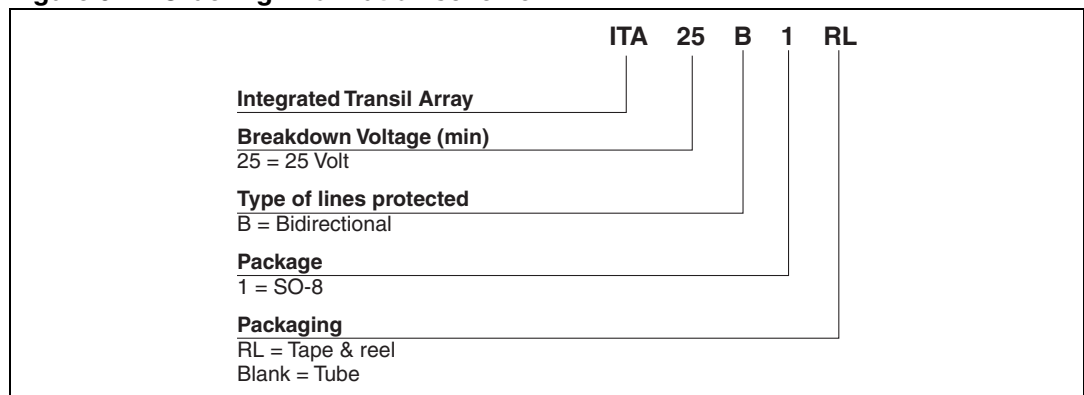
Order code	Maximum differential voltage between two input pins at 25 °C
ITA6V5B1	± 3.5 V
ITA10B1	± 5.0 V
ITA18B1	± 9.0 V
ITA25B1	± 12.5 V

**Figure 8. RS-232 junction (typical application)**



## 3 Ordering information scheme

**Figure 9. Ordering information scheme**



## 4 Package information

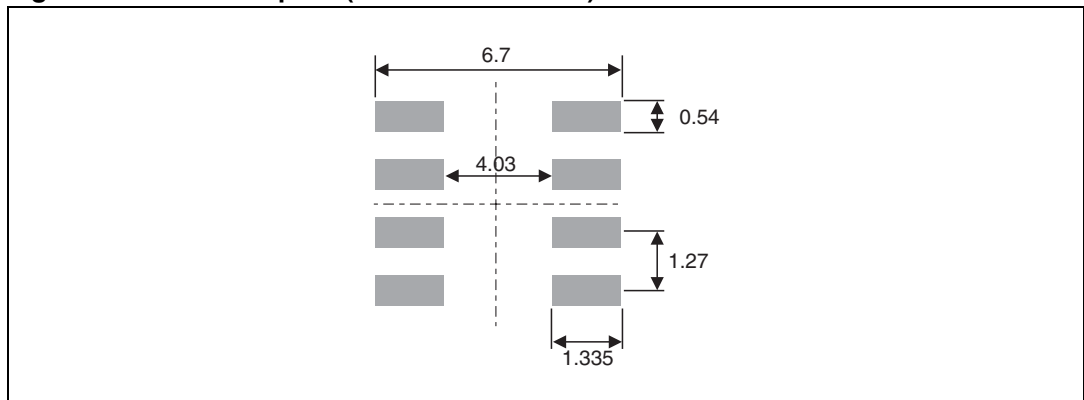
- Epoxy meets UL94, V0

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com).

**Table 4. SO-8 dimensions**

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.1		0.25	0.004		0.010
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
C	0.17		0.23	0.007		0.009
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
L1		1.04			0.041	
k°	0		8	0		8
ccc			0.10			0.004

**Figure 10. SO-8 footprint (dimensions in mm)**



## 5 Ordering Information

**Table 5. Ordering information**

Order code	Marking	Package	Weight	Base qty	Delivery mode
ITA6V5B1	6V5B1	SO-8	0.08 g	2000	Ammopack
ITA6V5B1RL	6V5B1			2500	Tape and reel
ITA10B1	10B1			2000	Ammopack
ITA18B1	18B1			2000	Ammopack
ITA18B1RL	18B1			2500	Tape and reel
ITA25B1	25B1			2000	Ammopack
ITA25B1RL	25B1			2500	Tape and reel

## 6 Revision history

**Table 6. Document revision history**

Date	Revision	Description of changes
13-Dec-2004	1	First issue.
15-Nov-2007	2	Reformatted to current standards. SO-8 package dimensions update. Updated pulse waveform parameters in <a href="#">Figure 2</a> .

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