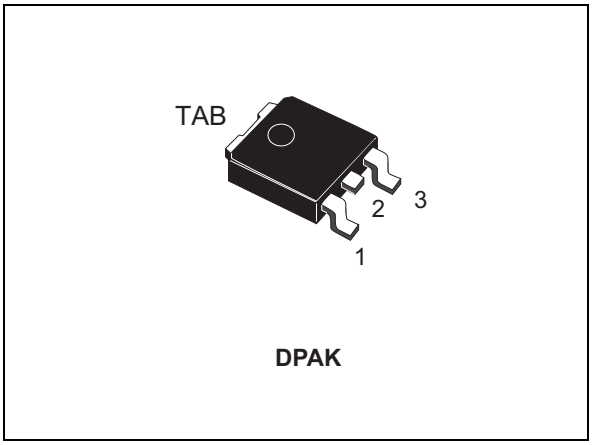
STD13N65M2

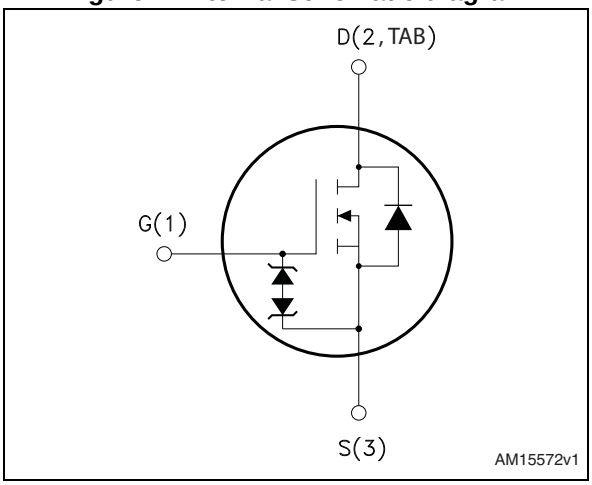
N-channel 650 V, 0.37 Ω typ., 10 A MDmesh M2 Power MOSFET in a DPAK package

Datasheet – production data



DPAK

Figure 1. Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max	I_D
STD13N65M2	650 V	0.43 Ω	10 A

- Extremely low gate charge
- Excellent output capacitance (C_{oss}) profile
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using MDmesh™ M2 technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance and optimized switching characteristics, rendering it suitable for the most demanding high efficiency converters.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STD13N65M2	13N65M2	DPAK	Tape and reel

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at T_C = 25 °C	10	A
I_D	Drain current (continuous) at T_C = 100 °C	6.3	A
I_{DM} (1)	Drain current (pulsed)	40	A
P_{TOT}	Total dissipation at T_C = 25 °C	110	W
dv/dt (2)	Peak diode recovery voltage slope	15	V/ns
dv/dt (3)	MOSFET dv/dt ruggedness	50	V/ns
T_{stg}	Storage temperature	- 55 to 150	°C
T_j	Max. operating junction temperature	150	

1. Pulse width limited by safe operating area.
2. I_{SD} ≤ 10 A, di/dt ≤ 400 A/µs; $V_{DS\ peak} < V_{(BR)DSS}$, V_{DD}=400 V.
3. V_{DS} ≤ 520 V

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	1.14	°C/W
$R_{thj\text{-}pcb}$	Thermal resistance junction-pcb max(1)	50	°C/W

1. When mounted on 1 inch² FR-4, 2 Oz copper board

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	1.8	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}; V_{DD} = 50 V)	350	mJ

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 5. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	650			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 650 V			1	µA
		V_{GS} = 0 V, V_{DS} = 650 V, T_C=125 °C			100	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ± 25 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 5 A		0.37	0.43	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = 100 V, f = 1 MHz	-	590	-	pF
C_{oss}	Output capacitance		-	27.5	-	pF
C_{rss}	Reverse transfer capacitance		-	1.1	-	pF
$C_{oss\ eq.}$ (1)	Equivalent output capacitance	V_{GS} = 0 V, V_{DS} = 0 to 520 V	-	168.5	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	6.5	-	Ω
Q_g	Total gate charge	V_{DD} = 520 V, I_D = 10 A, V_{GS} = 10 V (see *Figure 15*)	-	17	-	nC
Q_{gs}	Gate-source charge		-	3.3	-	nC
Q_{gd}	Gate-drain charge		-	7	-	nC

1. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 325 V, I_D = 5 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 14* and *19*)	-	11	-	ns
t_r	Rise time		-	7.8	-	ns
$t_{d(off)}$	Turn-off delay time		-	38	-	ns
t_f	Fall time		-	12	-	ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		10	A
I_{SDM} (1)	Source-drain current (pulsed)		-		40	A
V_{SD} (2)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 10 A	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 10 A, di/dt = 100 A/µs V_{DD} = 60 V (see *Figure 16*)	-	312		ns
Q_{rr}	Reverse recovery charge		-	2.7		µC
I_{RRM}	Reverse recovery current		-	17.5		A
t_{rr}	Reverse recovery time	I_{SD} = 10 A, di/dt = 100 A/µs V_{DD} = 60 V, T_j = 150 °C (see *Figure 16*)	-	464		ns
Q_{rr}	Reverse recovery charge		-	4.1		µC
I_{RRM}	Reverse recovery current		-	17.5		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

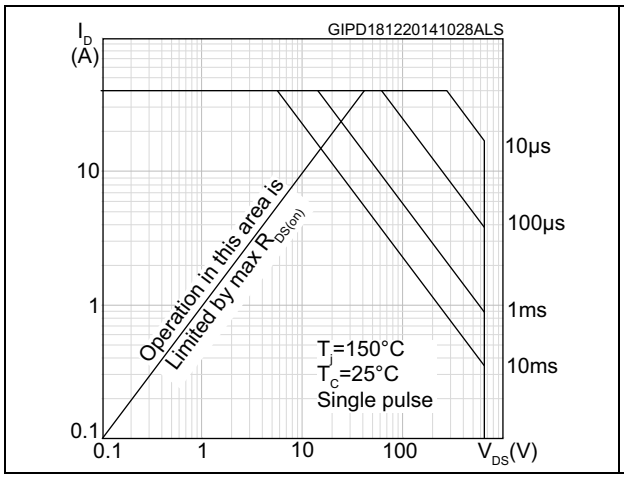


Figure 3. Thermal impedance

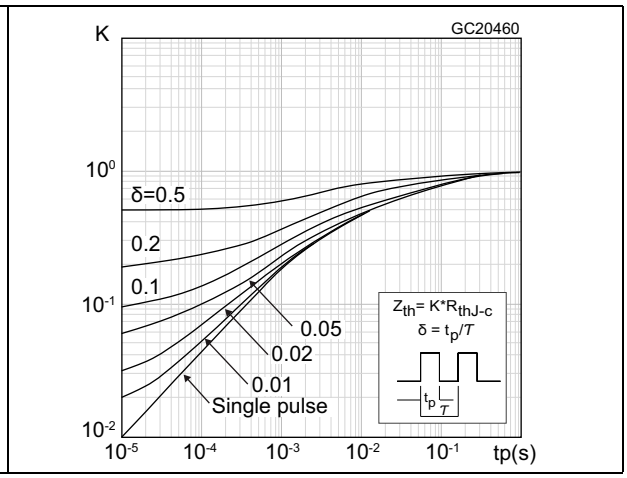


Figure 4. Output characteristics

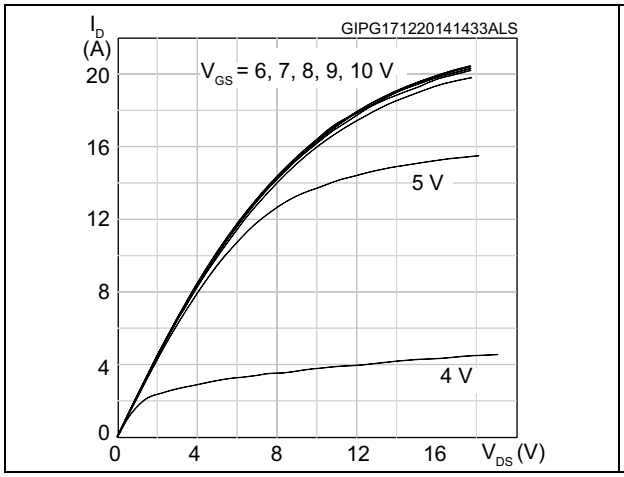


Figure 5. Transfer characteristics

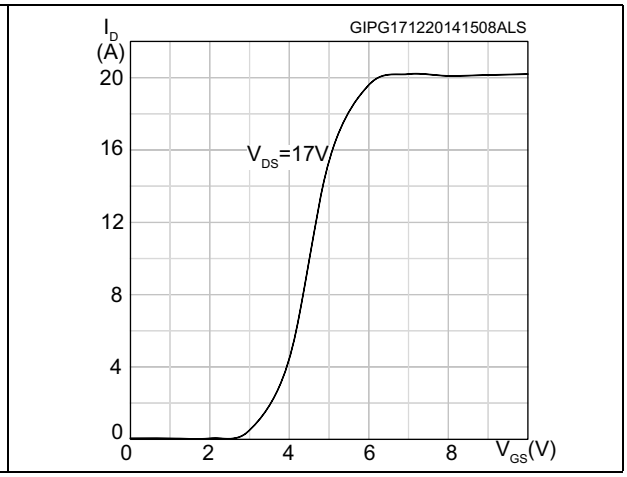


Figure 6. Normalized gate threshold voltage vs. temperature

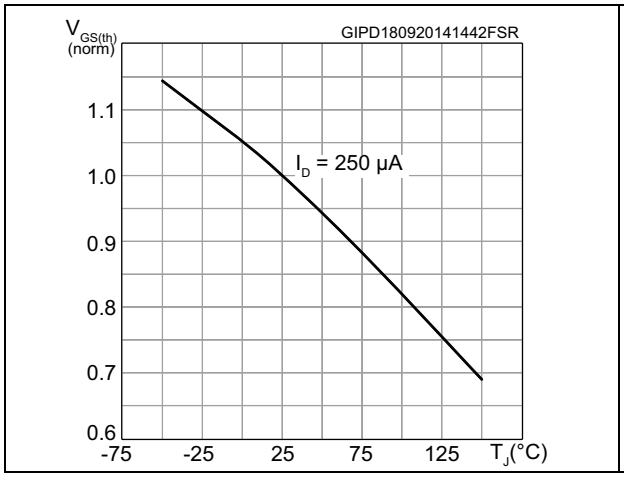


Figure 7. Normalized $V_{(BR)DSS}$ vs. temperature

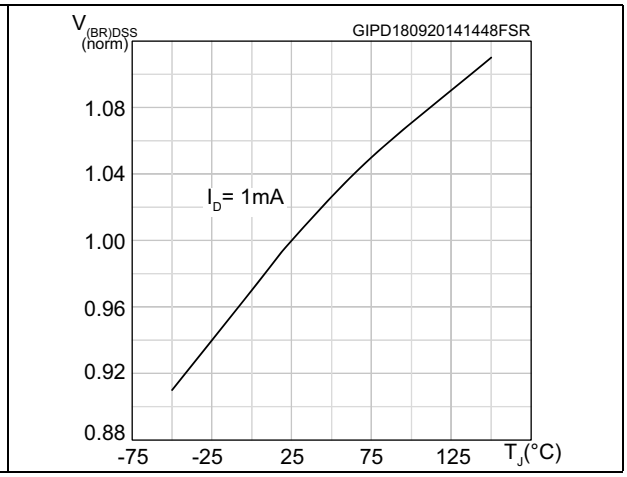


Figure 8. Static drain-source on-resistance

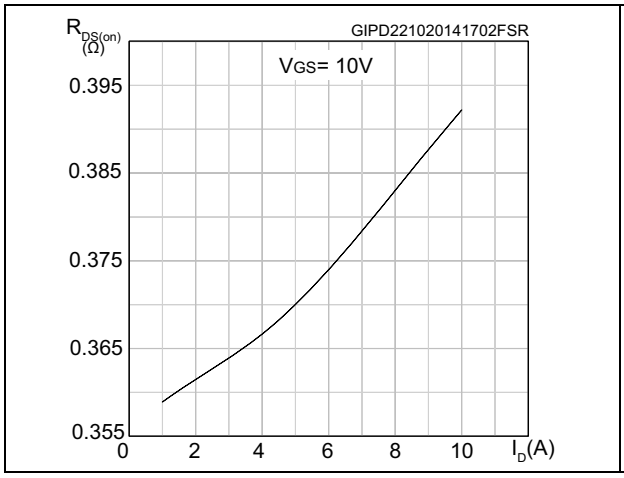


Figure 9. Normalized on-resistance vs. temperature

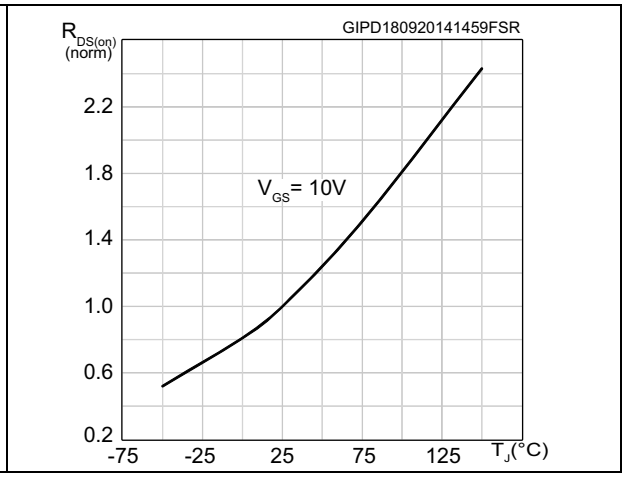


Figure 10. Gate charge vs. gate-source voltage

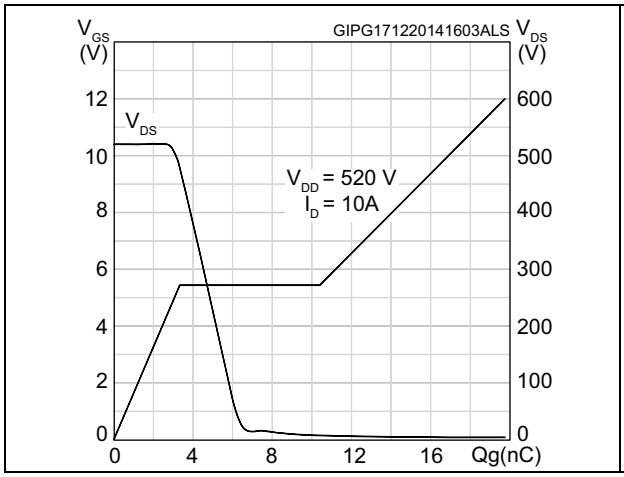


Figure 11. Capacitance variations

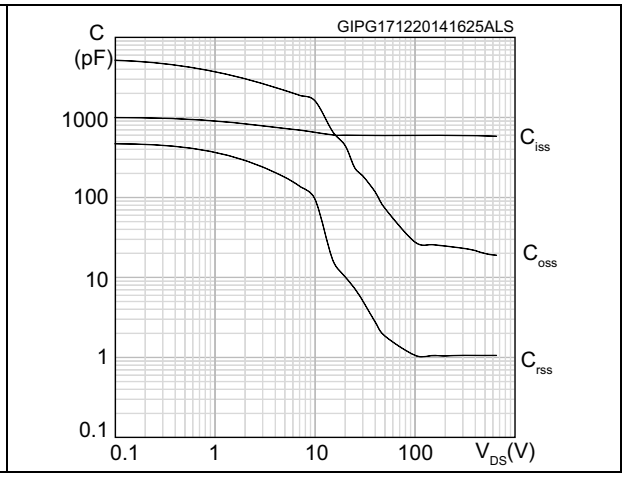


Figure 12. Output capacitance stored energy

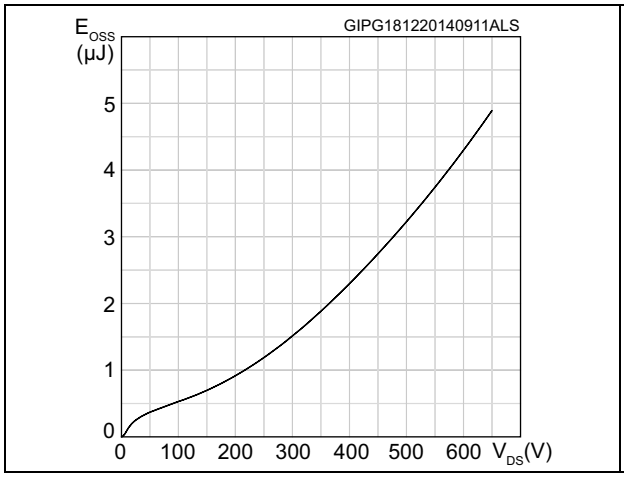
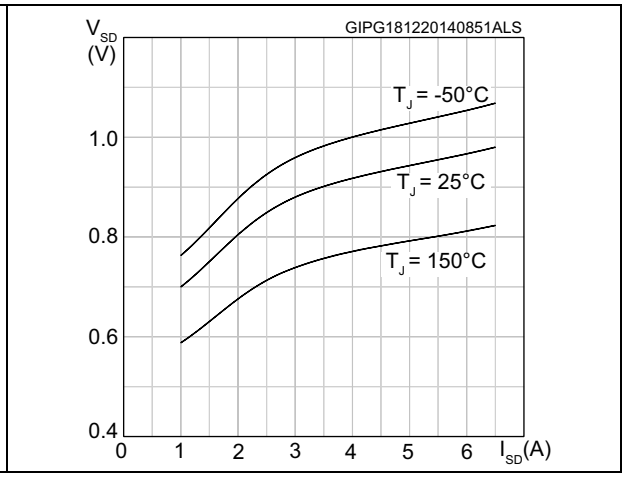


Figure 13. Source-drain diode forward characteristics



3 Test circuits

Figure 14. Switching times test circuit for resistive load

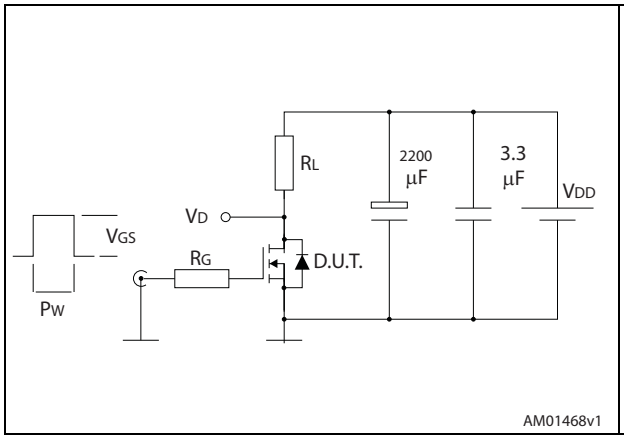


Figure 15. Gate charge test circuit

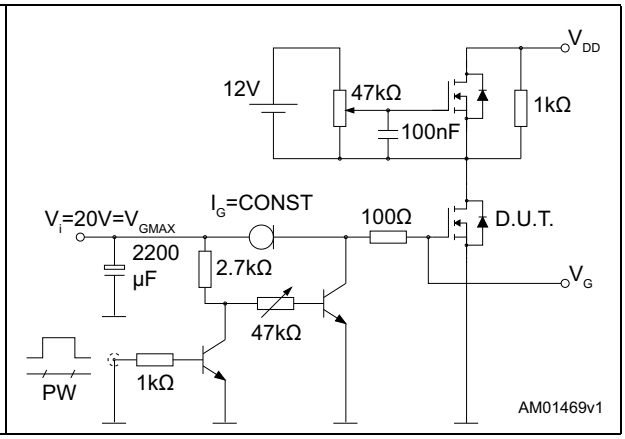


Figure 16. Test circuit for inductive load switching and diode recovery times

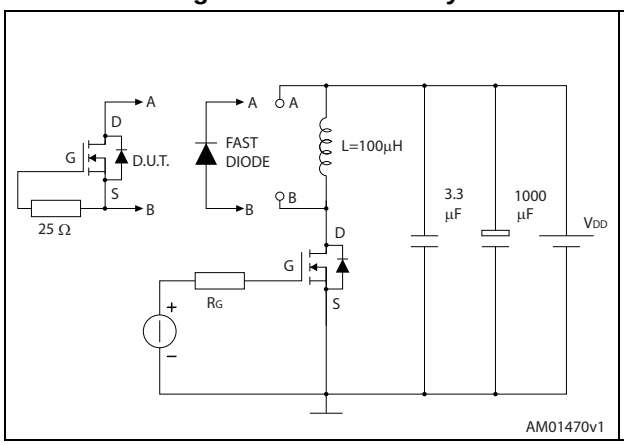


Figure 17. Unclamped inductive load test circuit

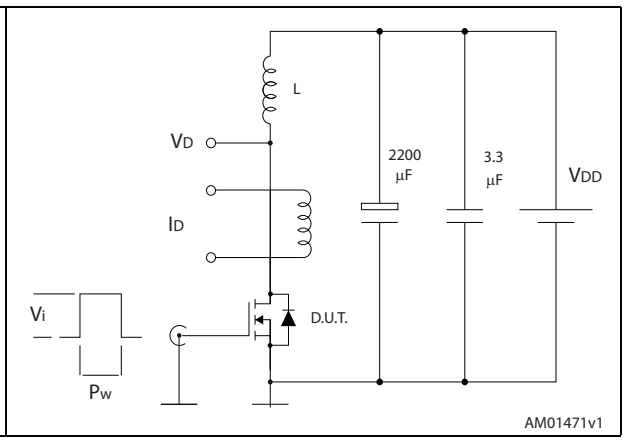


Figure 18. Unclamped inductive waveform

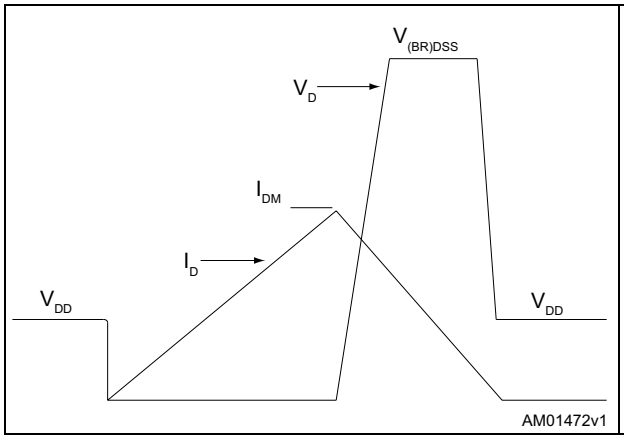
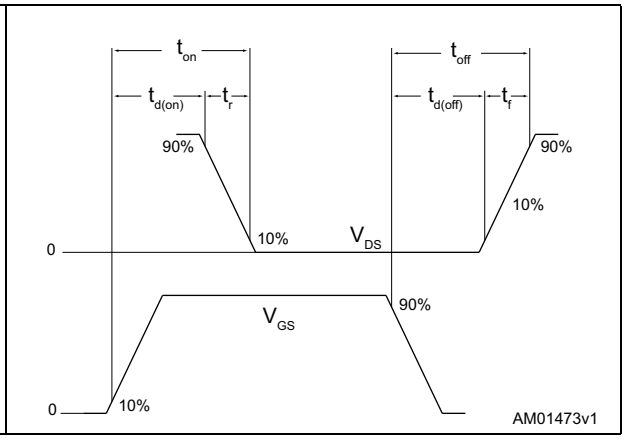


Figure 19. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 20. DPAK (TO-252) type A drawing

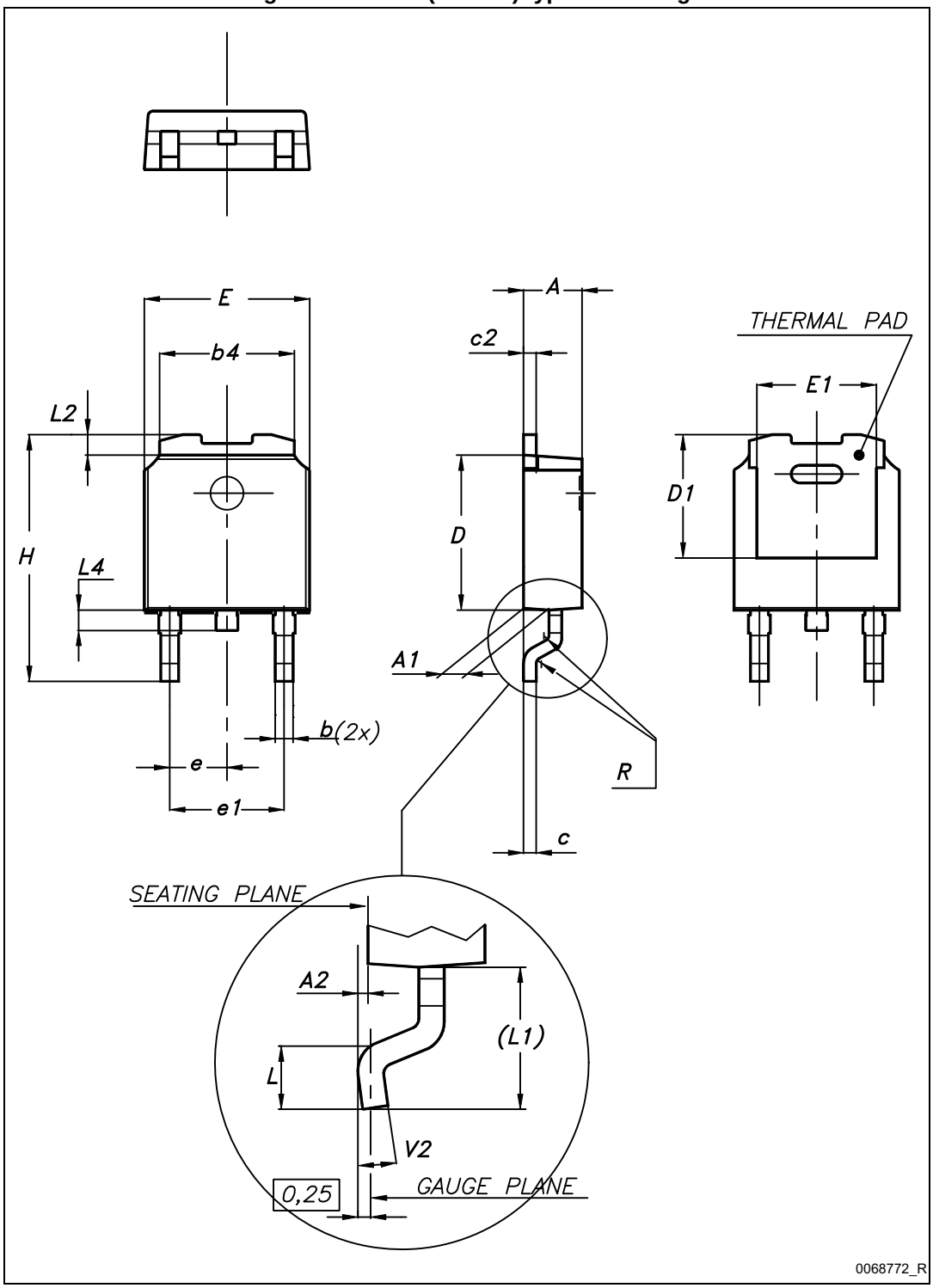
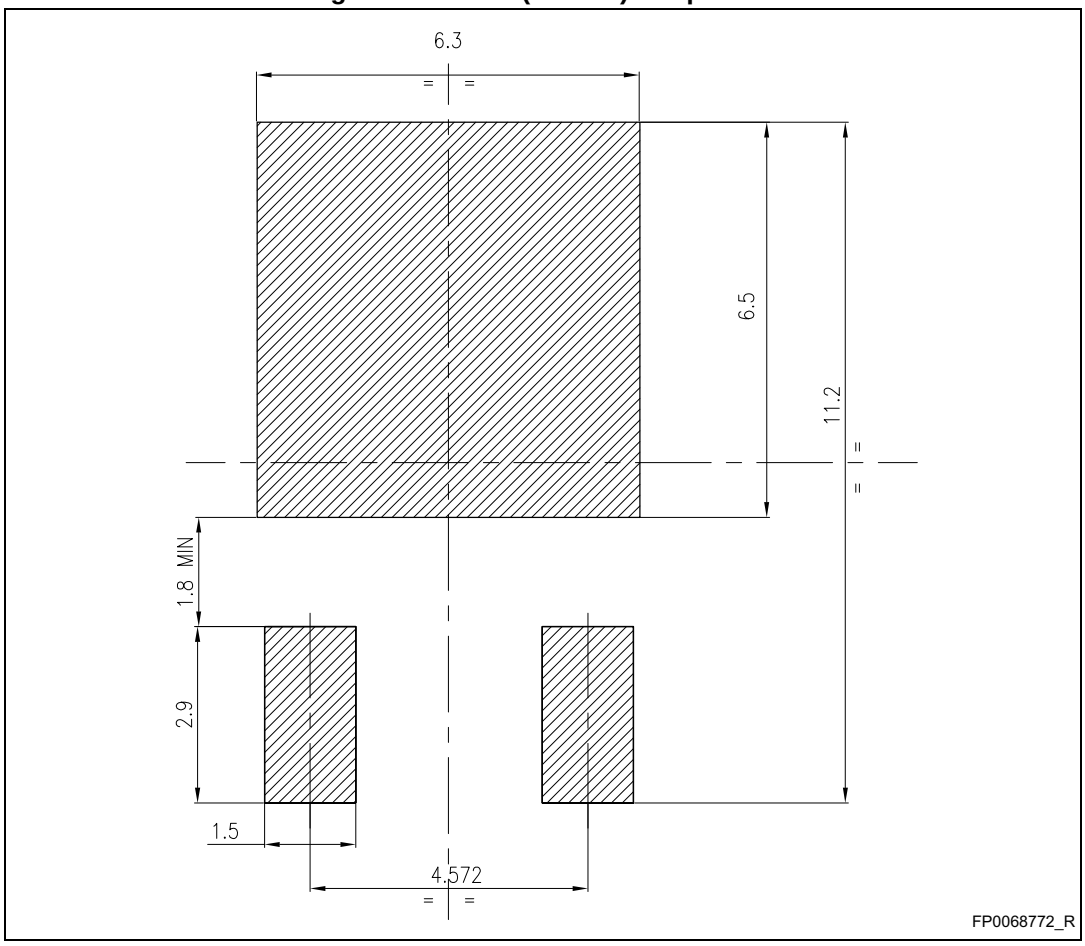


Table 9. DPAK (TO-252) type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
L1		2.80	
L2		0.80	
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 21. DPAK (TO-252) footprint [a]



a. All dimensions are in millimeters

5 Packaging mechanical data

Figure 22. TapeTape for DPAK (TO-252)

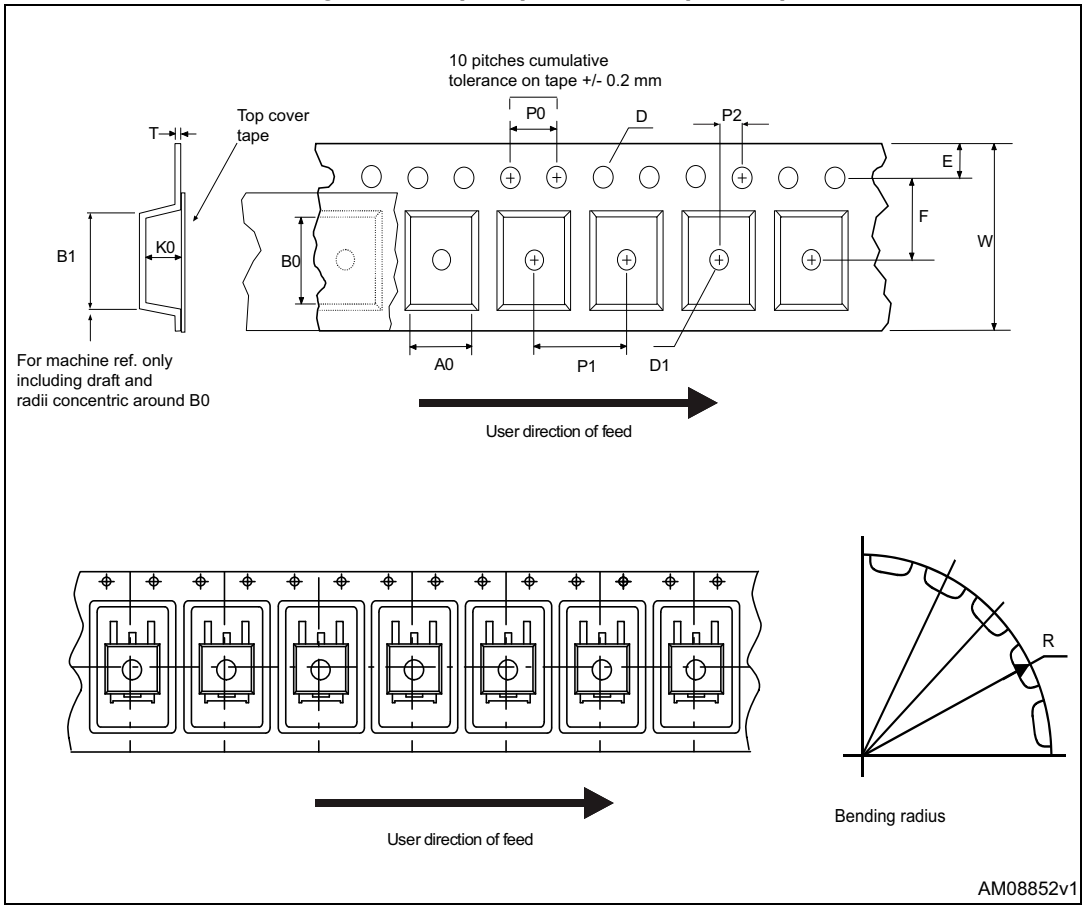


Figure 23. Reel for DPAK (TO-252)

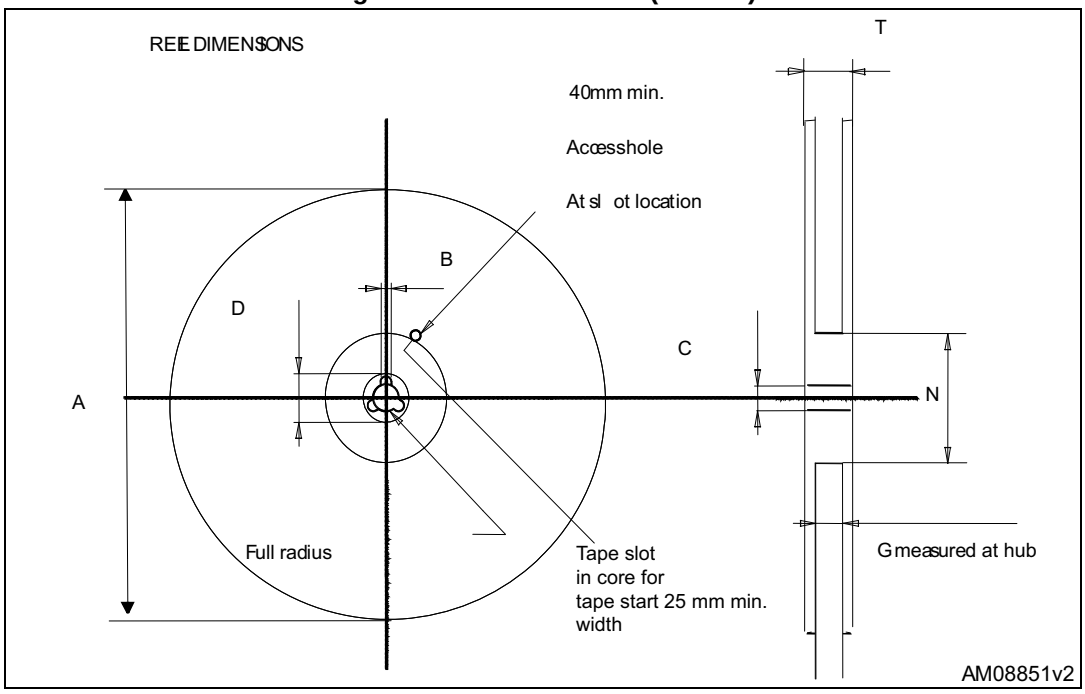


Table 10. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Figure 24. Revision history

Table 11. Document revision history

Date	Revision	Changes
18-Dec-2014	1	First release.

单击下面可查看定价，库存，交付和生命周期等信息

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