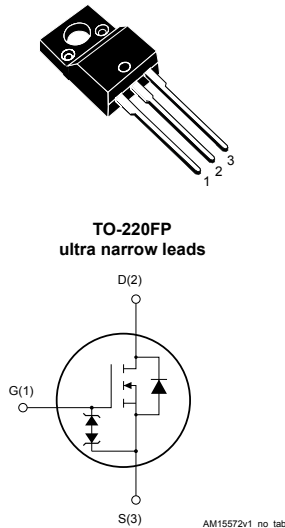


N-channel 800 V, 300 mΩ typ., 14 A MDmesh K5 Power MOSFET in a TO-220FP ultra narrow leads package



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STFU15N80K5	800 V	375 mΩ	14 A

- Industry's lowest $R_{DS(on)}$ x area
- Industry's best FoM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This very high voltage N-channel Power MOSFET is designed using MDmesh K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.



Product status link

[STFU15N80K5](#)

Product summary

Order code	STFU15N80K5
Marking	15N80K5
Package	TO-220FP ultra narrow leads
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 30	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	14	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	8.8	A
$I_{DM}^{(2)}$	Drain current (pulsed)	56	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	35	W
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink ($t=1\text{ s}$; $T_C=25\text{ }^\circ\text{C}$)	2500	V
$dv/dt^{(3)}$	Peak diode recovery voltage slope	4.5	V/ns
T_{stg}	Storage temperature range	- 55 to 150	$^\circ\text{C}$
T_J	Operating junction temperature range		

1. Limited by package.
2. Pulse width limited by safe operating area.
3. $I_{SD} \leq 14\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$; $V_{DS}(\text{peak}) < V_{(BR)DSS}$.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	4.17	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient	62.5	$^\circ\text{C}/\text{W}$

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	4	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	150	mJ

2 Electrical characteristics

$T_C = 25\text{ °C}$ unless otherwise specified.

Table 4. On/off-state

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	800			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}, V_{DS} = 800\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}, V_{DS} = 800\text{ V}$ $T_C = 125\text{ °C}^{(1)}$			50	μA
I_{GSS}	Gate body leakage current	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 100\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 7\text{ A}$		300	375	m Ω

1. Defined by design, not subject to production test.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}, f = 1\text{ MHz}, V_{GS} = 0\text{ V}$	-	1100	-	pF
C_{oss}	Output capacitance		-	85	-	pF
C_{rss}	Reverse transfer capacitance		-	1.5	-	pF
$C_{o(tr)}^{(1)}$	Equivalent capacitance time related	$V_{DS} = 0\text{ to }640\text{ V}, V_{GS} = 0\text{ V}$	-	113	-	pF
$C_{o(er)}^{(2)}$	Equivalent capacitance energy related		-	49	-	pF
R_g	Intrinsic gate resistance	$f = 1\text{ MHz}, I_D = 0\text{ A}$	-	4.5	-	Ω
Q_g	Total gate charge	$V_{DD} = 640\text{ V}, I_D = 12\text{ A}$	-	32	-	nC
Q_{gs}	Gate-source charge	$V_{GS} = 0\text{ to }10\text{ V}$	-	6	-	nC
Q_{gd}	Gate-drain charge	(see Figure 15. Test circuit for gate charge behavior)	-	22	-	nC

- Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}
- Energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 400\text{ V}, I_D = 7\text{ A}, R_G = 4.7\text{ }\Omega$	-	19	-	ns
t_r	Rise time	$V_{GS} = 10\text{ V}$	-	17.6	-	ns
$t_{d(off)}$	Turn-off delay time	see (Figure 14. Test circuit for resistive load switching times and Figure 19. Switching time waveform)	-	44	-	ns
t_f	Fall time		-	10	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		14	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		56	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 14\text{ A}$, $V_{GS} = 0\text{ V}$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 14\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$ (see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	445		ns
Q_{rr}	Reverse recovery charge		-	8.2		μC
I_{RRM}	Reverse recovery current		-	37		A
t_{rr}	Reverse recovery time	$I_{SD} = 14\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	580		ns
Q_{rr}	Reverse recovery charge		-	10		μC
I_{RRM}	Reverse recovery current		-	35		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1\text{ mA}$, $I_D = 0\text{ A}$	30	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

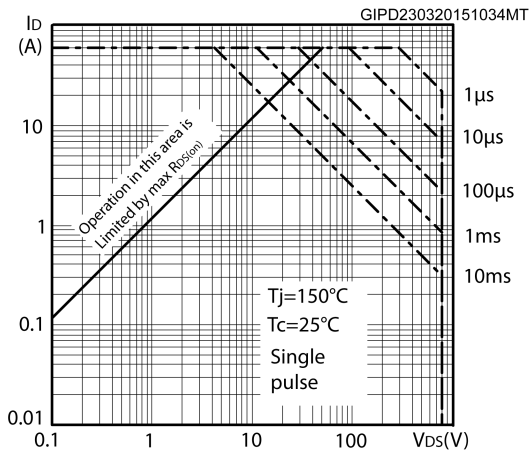


Figure 2. Thermal impedance

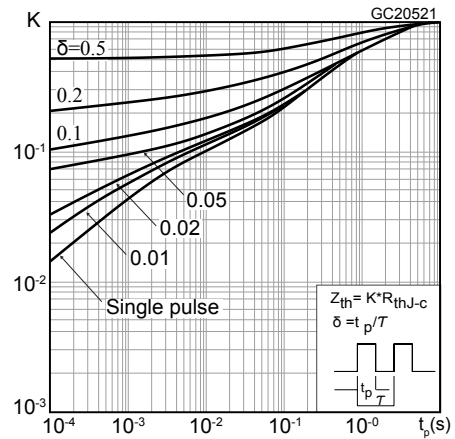


Figure 3. Output characteristics

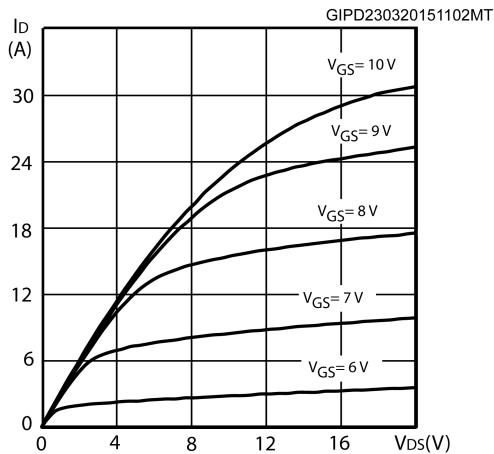


Figure 4. Transfer characteristics

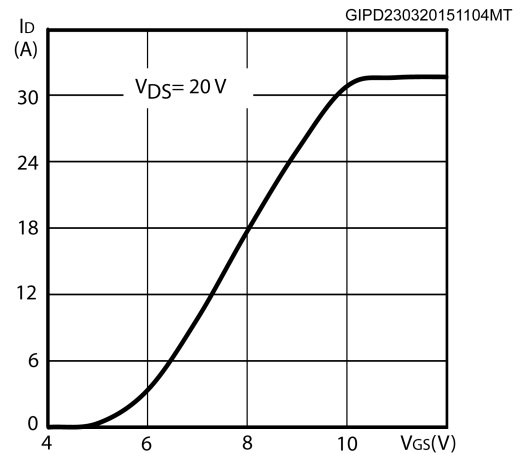


Figure 5. Gate charge vs gate-source voltage

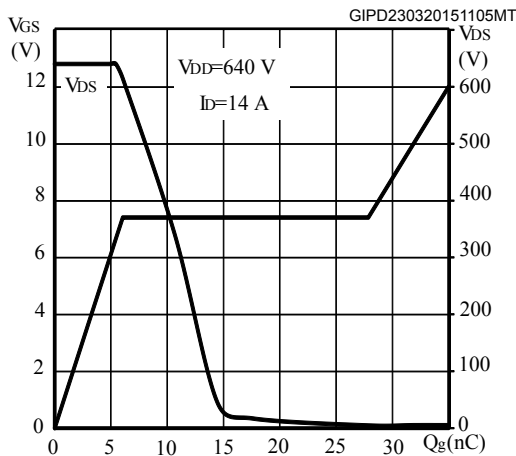


Figure 6. Static drain-source on-resistance

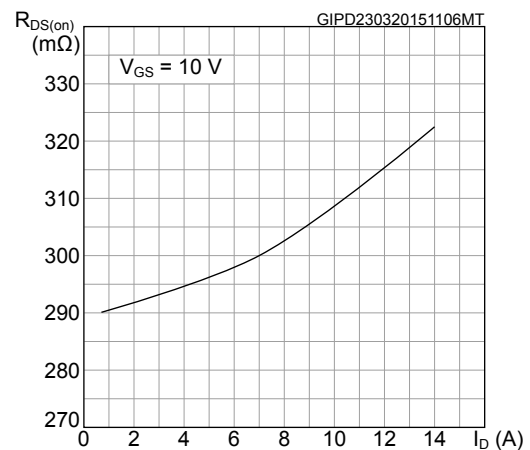


Figure 7. Capacitance variations

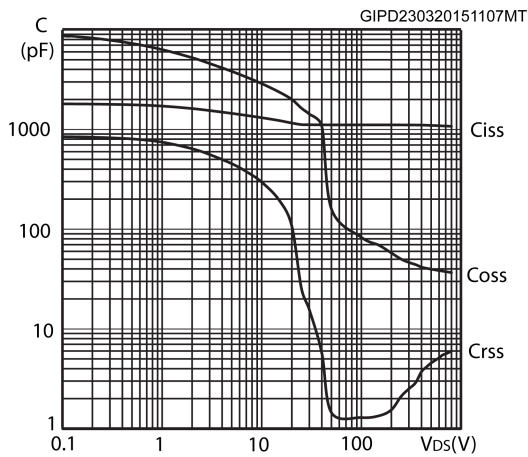


Figure 8. Source-drain diode forward characteristics

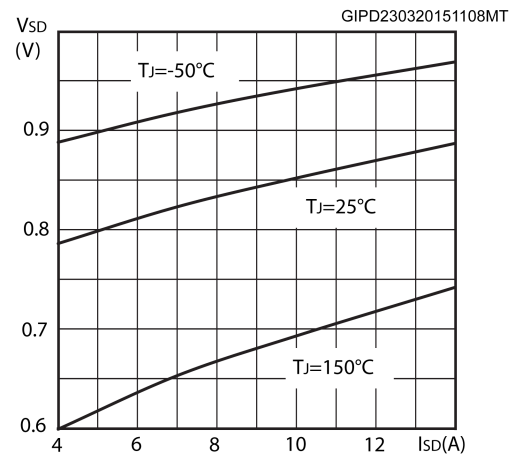


Figure 9. Normalized gate threshold voltage vs temperature

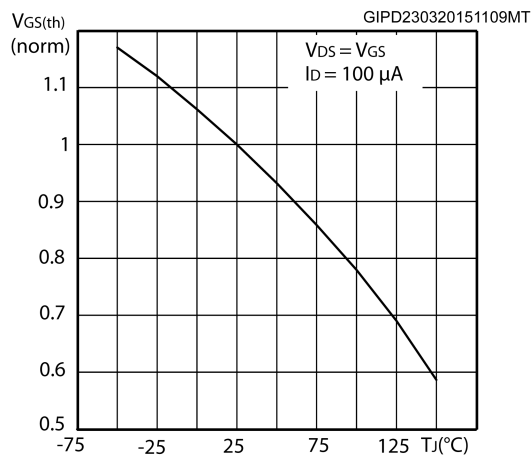


Figure 10. Normalized on-resistance vs temperature

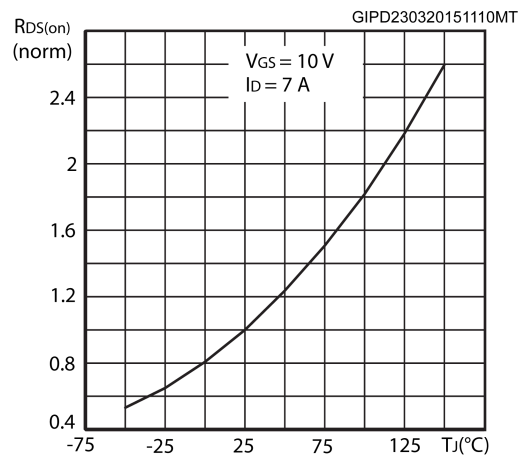


Figure 11. Output capacitance stored energy

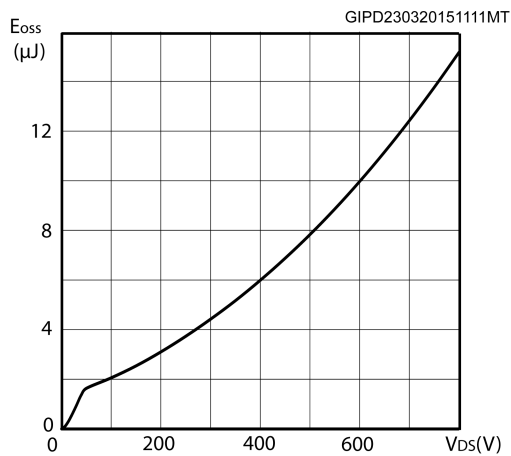


Figure 12. Normalized V_{DS} vs temperature

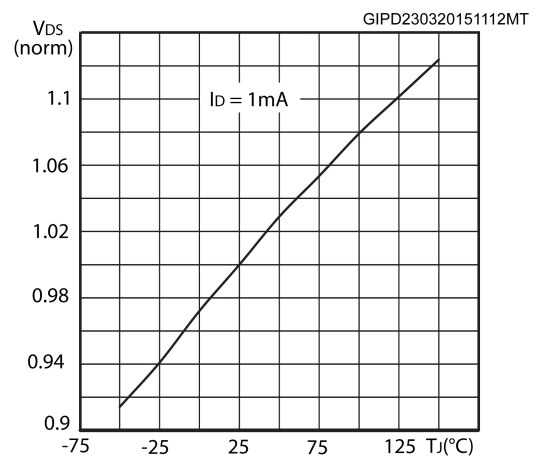
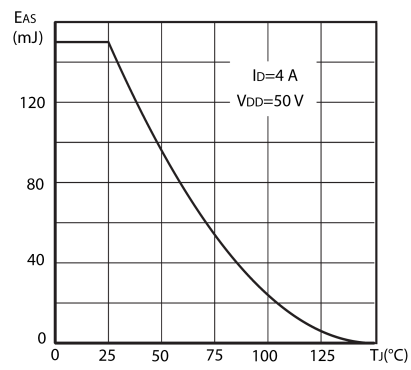
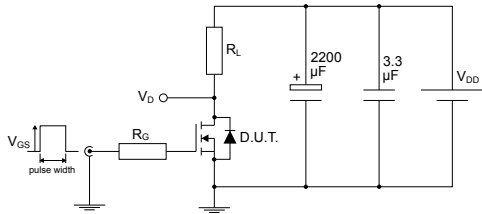


Figure 13. Maximum avalanche energy vs temperature

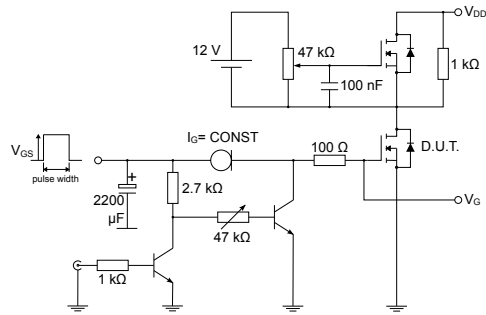


GIPD230320151113MT

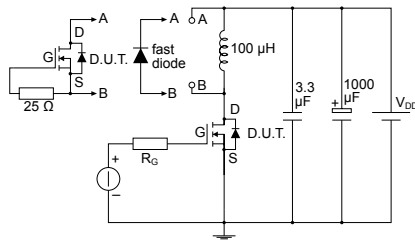
3 Test circuits

Figure 14. Test circuit for resistive load switching times


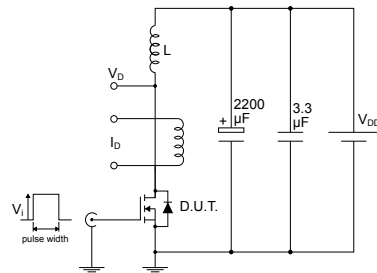
AM01468v1

Figure 15. Test circuit for gate charge behavior


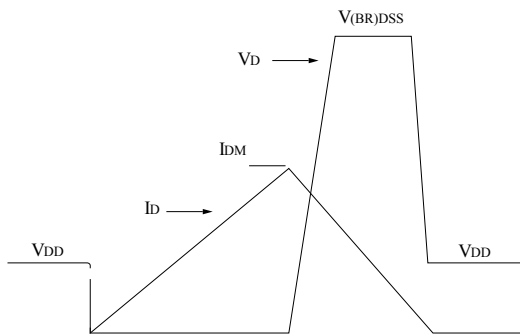
AM01469v1

Figure 16. Test circuit for inductive load switching and diode recovery times


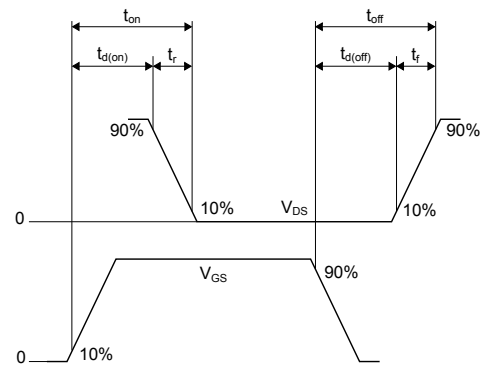
AM01470v1

Figure 17. Unclamped inductive load test circuit


AM01471v1

Figure 18. Unclamped inductive waveform


AM01472v1

Figure 19. Switching time waveform


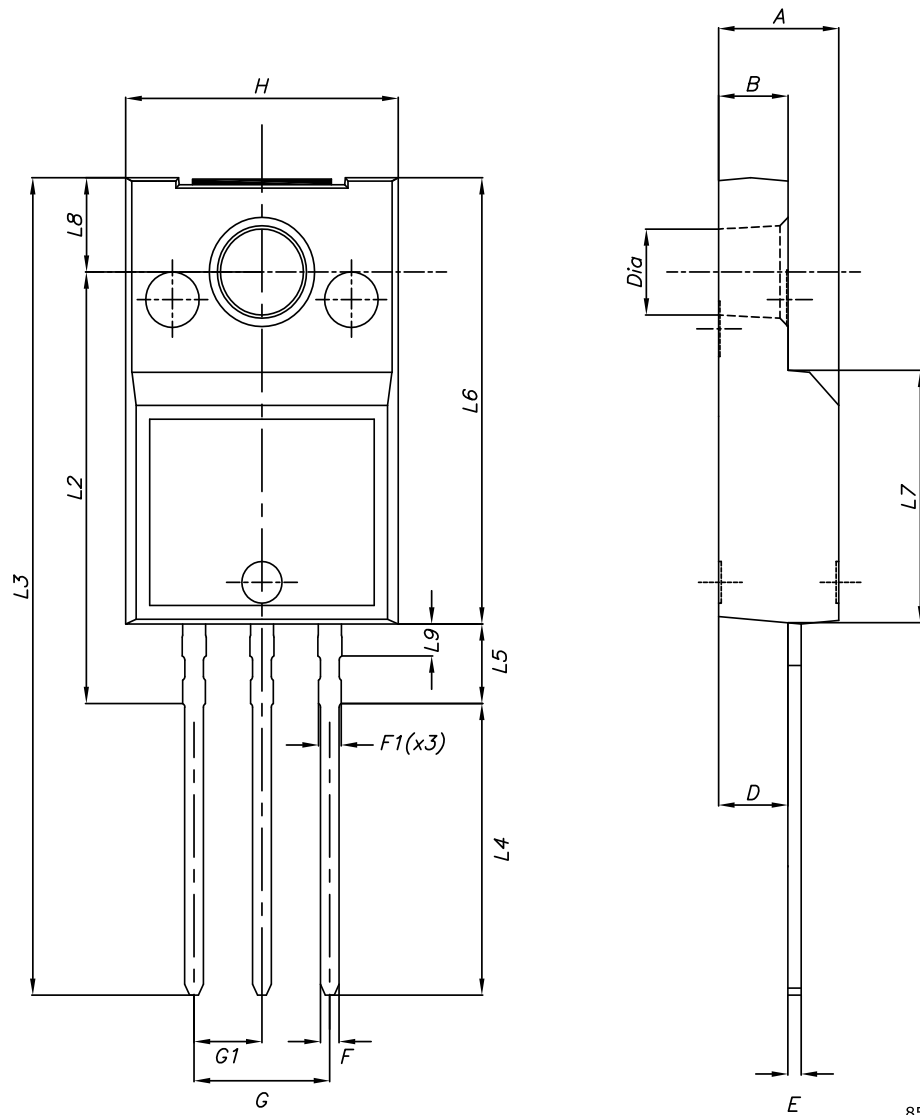
AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-220FP ultra narrow leads package information

Figure 20. TO-220FP ultra narrow leads package outline



8576148_2

Table 9. TO-220FP ultra narrow leads mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
E	0.45		0.60
F	0.65		0.75
F1	-		0.90
G	4.95		5.20
G1	2.40	2.54	2.70
H	10.00		10.40
L2	15.10		15.90
L3	28.50		30.50
L4	10.20		11.00
L5	2.50		3.10
L6	15.60		16.40
L7	9.00		9.30
L8	3.20		3.60
L9	-		1.30
Dia.	3.00		3.20

Revision history

Table 10. Document revision history

Date	Revision	Changes
13-Apr-2015	1	Initial release.
09-Sep-2015	2	Text and formatting changes throughout document Datasheet status promoted from preliminary to production data
15-May-2020	3	Updated internal schematic diagram on cover page. Modified Figure 6. Static drain-source on-resistance . Updated Section 4.1 TO-220FP ultra narrow leads package information . Minor text changes.

Contents

1	Electrical ratings	2
2	Electrical characteristics	3
2.1	Electrical characteristics (curves)	5
3	Test circuits	8
4	Package information	9
4.1	TO-220FP ultra narrow leads package information	9
	Revision history	11
	Contents	12

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, please refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2020 STMicroelectronics – All rights reserved

单击下面可查看定价，库存，交付和生命周期等信息

[>>STMicro\(意法半导体\)](#)