TSV521, TSV522, TSV524
TSV521A, TSV522A, TSV524A

Datasheet

High merit factor (1.15 MHz for 45 µA) rail-to-rail 5 V op amp


TSV521
SC70-5


TSV522
DFN8 2x2 mm


TSV522
MiniSO8


TSV524
QFN16 3x3


TSV524
TSSOP14

Maturity status link	Channel	Automotive	Enhanced V_{io}	Package
TSV521	1			SC70-5
TSV521A	1		•	SC70-5
TSV522	2			DFN8 2x2
		•		MiniSO8
TSV522A	2		•	DFN8 2x2
		•	•	MiniSO8
TSV524	4			QFN16 3x3
		•		TSSOP14
TSV524A	4		•	QFN16 3x3
		•	•	TSSOP14

Related products	
TSV631, TSV632, TSV634	Lower minimum supply voltage (1.5 V)
LMV821, LMV822, LMV824	Higher gain bandwidth products (5.5 MHz)

Features

- Gain bandwidth product: 1.15 MHz typ. at 5 V
- Low power consumption: 45 µA typ. at 5 V
- Rail-to-rail input and output
- Low input bias current: 1 pA typ.
- Supply voltage: 2.7 to 5.5 V
- Low offset voltage: 800 µV max.
- Unity gain stable on 100 pF capacitor
- AEC-Q100 qualified
- Benefits:
  - Increased lifetime in battery powered applications
  - Easy interfacing with high impedance sensors

Applications

- Battery powered applications
- Portable devices
- Automotive signal conditioning
- Active filtering
- Medical instrumentation

Description

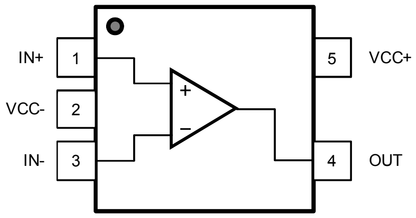
The TSV52x and TSV52xA series of operational amplifiers offer low voltage operation and rail-to rail input and output. The TSV521 device is the single version, the TSV522 device the dual version, and the TSV524 device the quad version, with pinouts compatible with industry standards.

The TSV52x and TSV52xA series offer an outstanding speed/power consumption ratio, 1.15 MHz gain bandwidth product while consuming only 45 µA at 5 V. The devices are housed in the smallest industrial packages.

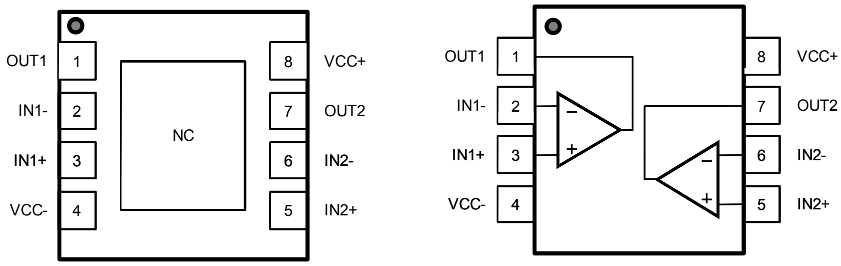
These features make the TSV52x, TSV52xA family ideal for sensor interfaces, battery supplied and portable applications. The wide temperature range and high ESD tolerance facilitate their use in harsh automotive applications.

1 Package pin connections

Figure 1. **Pin connections for each package (top view)**

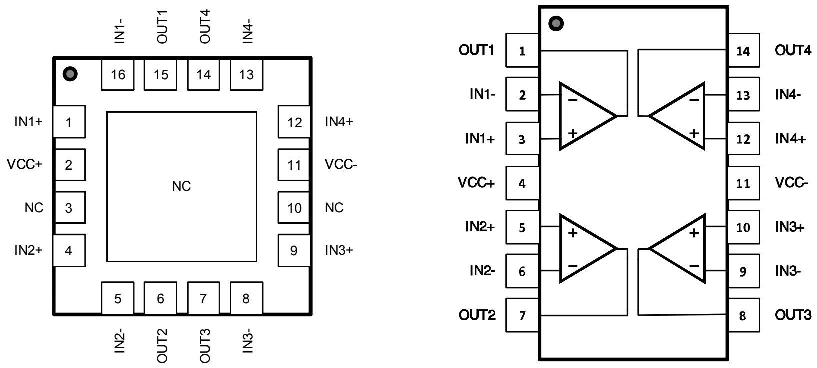


TSV521
SC70-5



TSV522
DFN8

TSV522
MiniSO8



TSV524
QFN16

TSV524
TSSOP14

Note: The exposed pads of the DFN8 (2x2) and QFN16 (3x3) can be connected to VCC- or left floating.

2 Absolute maximum ratings and operating conditions

Table 1. **Absolute maximum ratings**

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage (1)	6	V
V_{id}	Input voltage differential (2)	$\pm V_{CC}$	V
V_{in}	Input voltage (3)	(V_{CC-}) - 0.2 to (V_{CC+}) + 0.2	V
I_{in}	Input current (4)	10	mA
T_{stg}	Storage temperature	-65 to +150	°C
R_{thja}	Thermal resistance junction-to-ambient (5)(6)		°C / W
	SC70-5	205	
	DFN8 2x2	57	
	QFN16 3x3	45	
	MiniSO8	190	
	TSSOP14	100	
T_j	Maximum junction temperature	150	°C
ESD	HBM: human body model (7)	4	kV
	MM: machine model (8)	300	V
	CDM: charged device model (9) (all packages except SC70-5 and DFN8)	1.5	kV
	CDM: charged device model (SC70-5 and DFN8) (9)	1.3	
	Latch-up immunity	200	mA

1. *All voltage values, except differential voltages are with respect to network ground terminal.*
2. *Differential voltages are the non inverting input terminal with respect to the inverting input terminal.*
3. V_{CC} -V_{in} *must not exceed 6 V,* V_{in} *must not exceed 6 V.*
4. *Input current must be limited by a resistor in series with the inputs.*
5. *Short-circuits can cause excessive heating and destructive dissipation.*
6. R_{th} *are typical values.*
7. *Human body model: 100 pF discharged through a 1.5 kΩ resistor between two pins of the device, done for all couples of pin combinations with other pins floating.*
8. *Machine model: a 200 pF cap is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω), done for all couples of pin combinations with other pins floating.*
9. *Charged device model: all pins plus package are charged together to the specified voltage and then discharged directly to ground.*

Table 2. **Operating conditions**

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	2.7 to 5.5	V
V_{icm}	Common mode input voltage range	V_{CC-} – 0.1 to V_{CC+} + 0.1	V
T_{oper}	Operating free air temperature range	-40 to +125	°C

3 Electrical characteristics

Table 3. Electrical characteristics at V_{CC+} = +2.7 V with V_{CC-} = 0 V, $V_{icm} = V_{CC}/2$, T = 25 °C, and R_L = 10 kΩ connected to $V_{CC}/2$ (unless otherwise specified).

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Offset voltage	TSV52xA, T = 25 °C			800	µV
		TSV52xA, -40 °C < T < 125 °C			2600	
		TSV52x, T = 25 °C			1.5	mV
		TSV52x, -40 °C < T < 125 °C			3.3	
$\Delta V_{io}/\Delta T$	Input offset voltage drift	-40 °C < T < 125 °C		3	18	µV/°C
I_{io}	Input offset current (3) ($V_{out} = V_{CC}/2$)	T = 25 °C		1	10	pA
		-40 °C < T < 125 °C		1	100	
I_{ib}	Input bias current (3) ($V_{out} = V_{CC}/2$)	T = 25 °C		1	10	
		-40 °C < T < 125 °C		1	100	
CMR	Common-mode rejection ratio 20 log ($\Delta V_{ic}/\Delta V_{io}$) V_{ic} = -0.1 V to V_{CC} + 0.1 V, $V_{out} = V_{CC}/2$, R_L = 1 MΩ	T = 25 °C	50	72		dB
		-40 °C < T < 125 °C	46			
A_{vd}	Large signal voltage gain V_{out} = 0.5 V to (V_{CC} -0.5 V), R_L = 1 MΩ	T = 25 °C	90	105		
		-40 °C < T < 125 °C	60			
V_{OH}	High level output voltage	T = 25 °C		3	35	mV
		-40 °C < T < 125 °C			50	
V_{OL}	Low level output voltage	T = 25 °C		6	35	
		-40 °C < T < 125 °C			50	
I_{out}	I_{sink}	$V_{out} = V_{CC}$, T = 25 °C	12	22		mA
		$V_{out} = V_{CC}$, -40 °C < T < 125 °C	8			
	I_{source}	V_{out} = 0 V, T = 25 °C	12	18		
		V_{out} = 0 V, -40 °C < T < 125 °C	8			
I_{CC}	Supply current (per channel) $V_{out} = V_{CC}/2$, R_L > 1 MΩ	T = 25 °C		30	51	µA
		-40 °C < T < 125 °C		30	51	
AC performance						
GBP	Gain bandwidth product	R_L = 10 kΩ, C_L = 100 pF	0.62	1		MHz
F_u	Unity gain frequency			900		kHz
ϕ_m	Phase margin			55		degrees
G_m	Gain margin			7		dB
SR	Slew rate	R_L = 10 kΩ, C_L = 100 pF, V_{out} = 0.5 V to V_{CC} -0.5 V		0.74		V/µs
e_n	Equivalent input noise voltage	f = 1 kHz		61		$\frac{nV}{\sqrt{Hz}}$
		f = 10 kHz		43		
THD+N	Total harmonic distortion + noise	Follower configuration, f_{in} = 1 kHz, R_L = 100 kΩ, $V_{icm} = V_{CC}/2$, BW = 22 kHz, V_{out} = 1 V_{pp}		0.003		%

Table 4. **Electrical characteristics at V_{CC+} = +3.3 V with V_{CC-} = 0 V, V_{icm} = $V_{CC}/2$, T = 25 °C, and R_L = 10 kΩ connected to $V_{CC}/2$ (unless otherwise specified).**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Offset voltage	TSV52xA, T = 25 °C			600	µV
		TSV52xA, -40 °C < T < 125 °C			2400	
		TSV52x, T = 25 °C			1.3	mV
		TSV52x, -40 °C < T < 125 °C			3.1	
$\Delta V_{io}/\Delta T$	Input offset voltage drift	-40 °C < T < 125 °C		3	18	µV/°C
ΔV_{io}	Long term input offset voltage drift [2]	T = 25 °C			0.3	$\frac{\mu V}{\sqrt{month}}$
I_{io}	Input offset current [3] (V_{out} = $V_{CC}/2$)	T = 25 °C		1	10	pA
		-40 °C < T < 125 °C		1	100	
I_{ib}	Input bias current [3] (V_{out} = $V_{CC}/2$)	T = 25 °C		1	10	
		-40 °C < T < 125 °C		1	100	
CMR	Common-mode rejection ratio 20 log ($\Delta V_{ic}/\Delta V_{io}$) V_{ic} = -0.1 V to V_{CC} + 0.1 V, V_{out} = $V_{CC}/2$, R_L = 1 MΩ	T = 25 °C	51	73		dB
		-40 °C < T < 125 °C	47			
A_{vd}	Large signal voltage gain V_{out} = 0.5 V to (V_{CC} -0.5 V), R_L = 1 MΩ	T = 25 °C	91	106		
		-40 °C < T < 125 °C	63			
V_{OH}	High level output voltage	T = 25 °C		3	35	mV
		-40 °C < T < 125 °C			50	
V_{OL}	Low level output voltage	T = 25 °C		7	35	
		-40 °C < T < 125 °C			50	
I_{out}	I_{sink}	V_{out} = V_{CC}, T = 25 °C	20	31		mA
		V_{out} = V_{CC}, -40 °C < T < 125 °C	17			
	I_{source}	V_{out} = 0 V, T = 25 °C	19	27		
		V_{out} = 0 V, -40 °C < T < 125 °C	17			
I_{CC}	Supply current (per channel) V_{out} = $V_{CC}/2$, R_L > 1 MΩ	T = 25 °C		32	55	µA
		-40 °C < T < 125 °C		32	55	
AC performance						
GBP	Gain bandwidth product	R_L = 10 kΩ, C_L = 100 pF	0.64	1		MHz
F_u	Unity gain frequency			900		kHz
ϕ_m	Phase margin			55		degrees
G_m	Gain margin			7		dB
SR	Slew rate	R_L = 10 kΩ, C_L = 100 pF, V_{out} = 0.5 V to V_{CC} -0.5 V		0.75		V/µs
e_n	Equivalent input noise voltage	f = 1 kHz		60		$\frac{nV}{\sqrt{Hz}}$
		f = 10 kHz		42		
THD+N	Total harmonic distortion + noise	Follower configuration, f_{in} = 1 kHz, R_L = 100 kΩ, V_{icm} = $V_{CC}/2$, BW = 22 kHz, V_{out} = 1 V_{pp}		0.003		%

Table 5. **Electrical characteristics at V_{CC+} = +5 V with V_{CC-} = 0 V, V_{icm} = $V_{CC}/2$, T = 25 °C, and R_L = 10 kΩ connected to $V_{CC}/2$ (unless otherwise specified).**

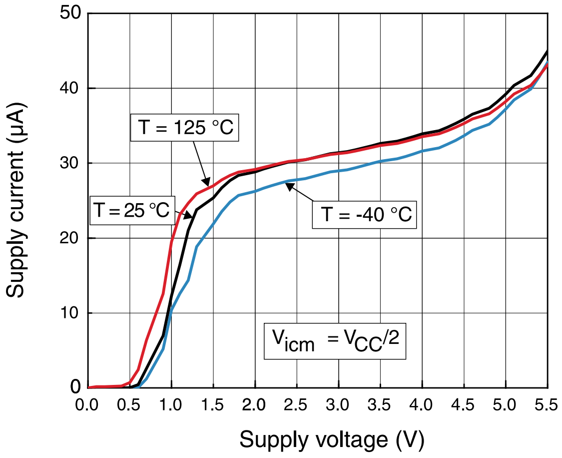
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Offset voltage	TSV52xA, T = 25 °C			600	µV
		TSV52xA, -40 °C < T < 125 °C			2400	
		TSV52x, T = 25 °C			1	mV
		TSV52x, -40 °C < T < 125 °C			2.8	
$\Delta V_{io}/\Delta T$	Input offset voltage drift (1)	-40 °C < T < 125 °C		3	18	µV/°C
ΔV_{io}	Long term input offset voltage drift (2)	T = 25 °C		0.7		$\frac{\mu V}{\sqrt{month}}$
I_{io}	Input offset current (3) (V_{out} = $V_{CC}/2$)	T = 25 °C		1	10	pA
		-40 °C < T < 125 °C		1	100	
I_{ib}	Input bias current (3) (V_{out} = $V_{CC}/2$)	T = 25 °C		1	10	
		-40 °C < T < 125 °C		1	100	
CMR1	Common-mode rejection ratio 20 log ($\Delta V_{ic}/\Delta V_{io}$) V_{ic} = -0.1 V to V_{CC} + 0.1 V, V_{out} = $V_{CC}/2$, R_L = 1 MΩ	T = 25 °C	54	76		dB
		-40 °C < T < 125 °C	50			
CMR2	Common-mode rejection ratio 20 log ($\Delta V_{ic}/\Delta V_{io}$) V_{ic} = -0.1 V to V_{CC} + 0.1 V, V_{out} = $V_{CC}/2$, R_L = 1 MΩ	T = 25 °C	63	84		
		-40 °C < T < 125 °C	58			
SVR	Supply voltage rejection ratio 20 log ($\Delta V_{CC}/\Delta V_{io}$) V_{CC} = 2.7 V to 5.5 V, V_{out} = $V_{CC}/2$	T = 25 °C	65	87		
		-40 °C < T < 125 °C	60			
A_{vd}	Large signal voltage gain V_{out} = 0.5 V to (V_{CC} -0.5 V), R_L = 1 MΩ	T = 25 °C	94	109		
		-40 °C < T < 125 °C	68			
V_{OH}	High level output voltage	T = 25 °C		5	35	mV
		-40 °C < T < 125 °C			50	
V_{OL}	Low level output voltage	T = 25 °C		9	35	
		-40 °C < T < 125 °C			50	
I_{out}	I_{sink}	V_{out} = V_{CC}, T = 25 °C	36	55		mA
		V_{out} = V_{CC}, -40 °C < T < 125 °C	27			
	I_{source}	V_{out} = 0 V, T = 25 °C	36	55		
		V_{out} = 0 V, -40 °C < T < 125 °C	27			
I_{CC}	Supply current (per channel) V_{out} = $V_{CC}/2$, R_L > 1 MΩ	T = 25 °C		45	60	µA
		-40 °C < T < 125 °C		45	60	
AC performance						
GBP	Gain bandwidth product	R_L = 10 kΩ, C_L = 100 pF	0.73	1.15		MHz
F_u	Unity gain frequency			900		kHz
ϕ_m	Phase margin			55		degrees
G_m	Gain margin			7		dB
SR	Slew rate	R_L = 10 kΩ, C_L = 100 pF, V_{out} = 0.5 V to V_{CC} -0.5 V		0.89		V/µs

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$\int e_n$	Low-frequency peak-to-peak input noise	Bandwidth: f = 0.1 to 10 Hz		14		µV_{pp}
e_n	Equivalent input noise voltage	f = 1 kHz		57		$\frac{nV}{\sqrt{Hz}}$
		f = 10 kHz		39		
THD+N	Total harmonic distortion + noise	Follower configuration, f_{in} = 1 kHz, R_L = 100 kΩ, V_{icm} = V_{CC}/2, BW = 22 kHz, V_{out} = 1 V_{pp}		0.002		%

1. *See Section 4.6: Input offset voltage drift over temperature.*
2. *Typical value is based on the V_{io} drift observed after 1000 h at 125 °C extrapolated to 25 °C using the Arrhenius law and assuming an activation energy of 0.7 eV. The operational amplifier is aged in follower mode configuration.*
3. *Guaranteed by design.*

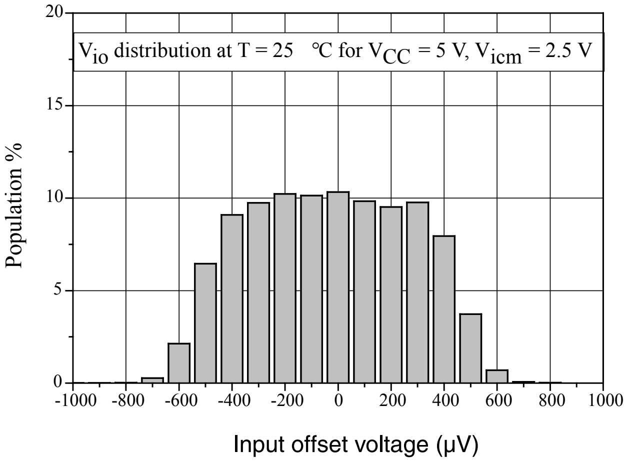
4 Typical performance characteristics

Figure 2. Supply current vs. supply voltage at $V_{icm} = V_{CC}/2$



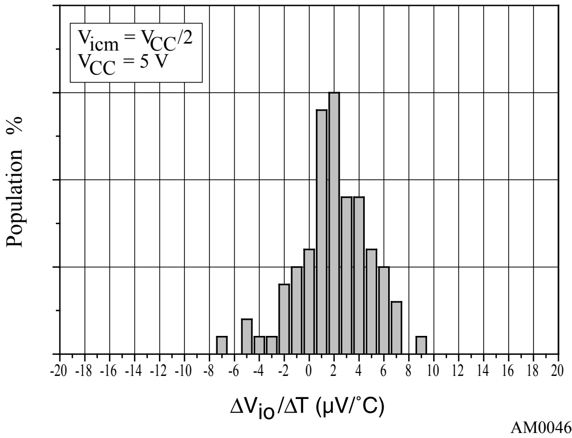
AM00460

Figure 3. Input offset voltage distribution at V_{CC} = 5 V, V_{icm} = 2.5 V



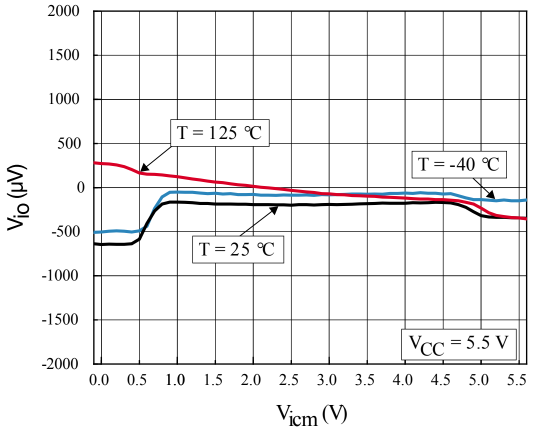
AM00461

Figure 4. Input offset voltage temperature coefficient distribution



AM00462

Figure 5. Input offset voltage vs. input common-mode voltage at V_{CC} = 5 V



AM00463

Figure 6. Input offset voltage vs. temperature at V_{CC} = 5 V

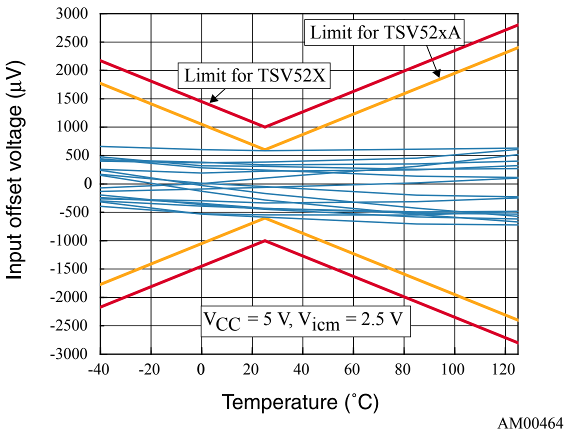


Figure 7. Output current vs. output voltage at V_{CC} = 2.7 V

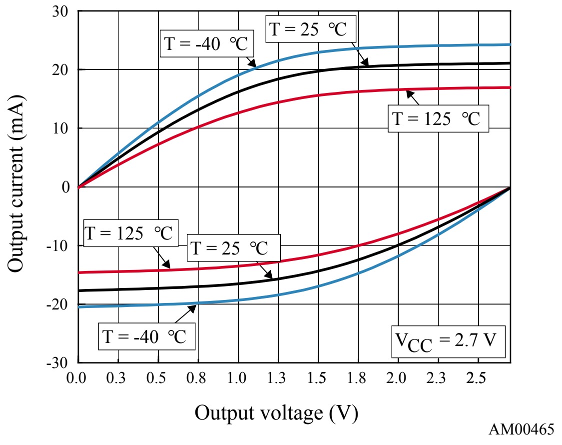


Figure 8. Output current vs. output voltage at V_{CC} = 5.5 V

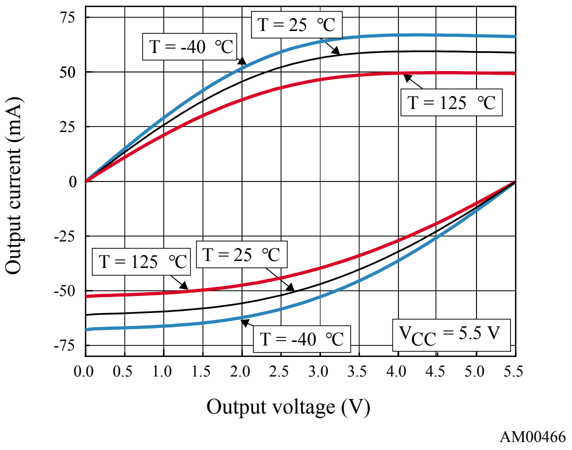


Figure 9. Bode diagram at V_{CC} = 2.7 V, R_L = 10 kΩ

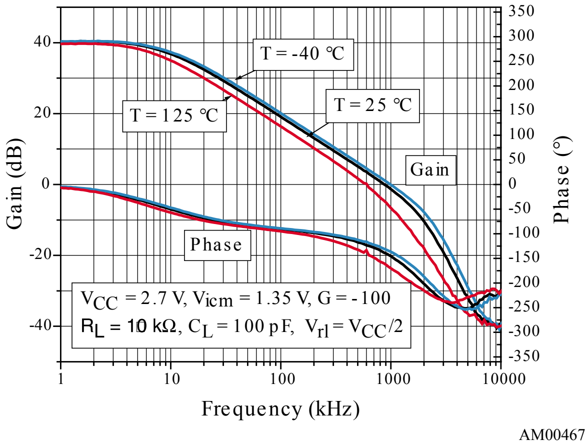


Figure 10. Bode diagram at V_{CC} = 2.7 V, R_L = 2 kΩ

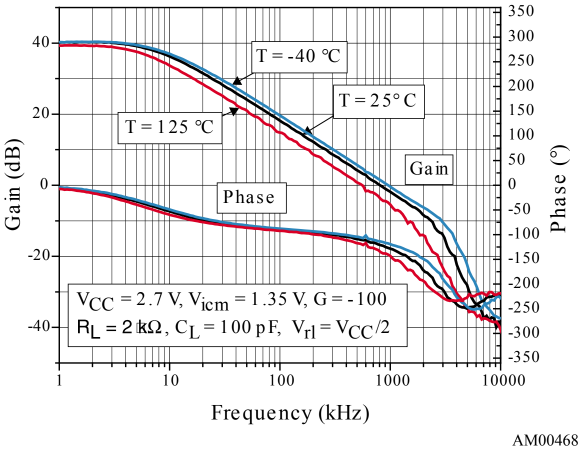


Figure 11. Bode diagram at V_{CC} = 5.5 V, R_L = 2 kΩ

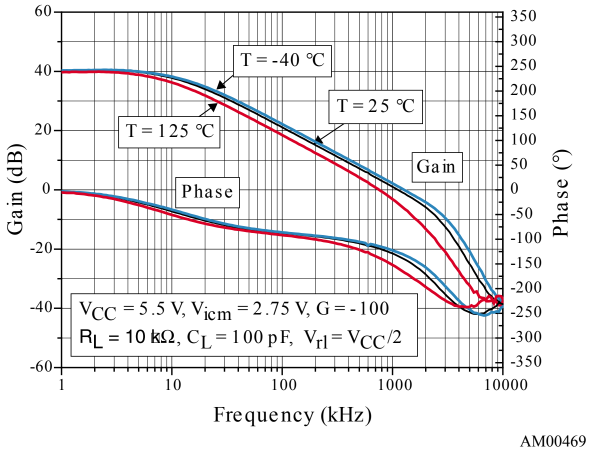


Figure 12. Bode diagram at V_{CC} = 5.5 V, R_L = 2 kΩ

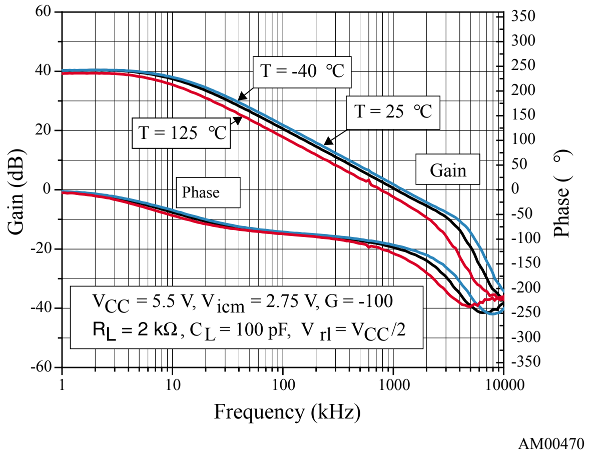


Figure 13. Noise vs. frequency

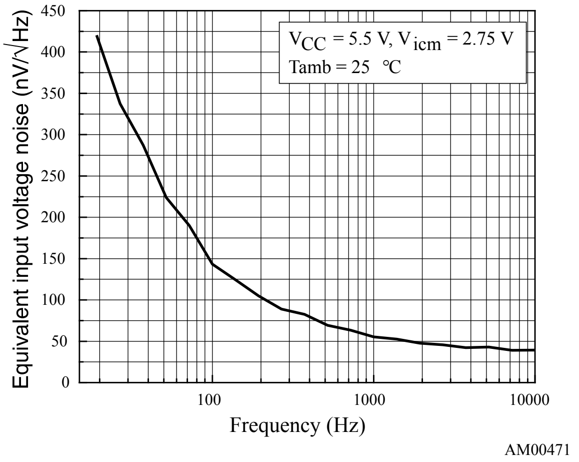


Figure 14. Positive slew rate vs. supply voltage

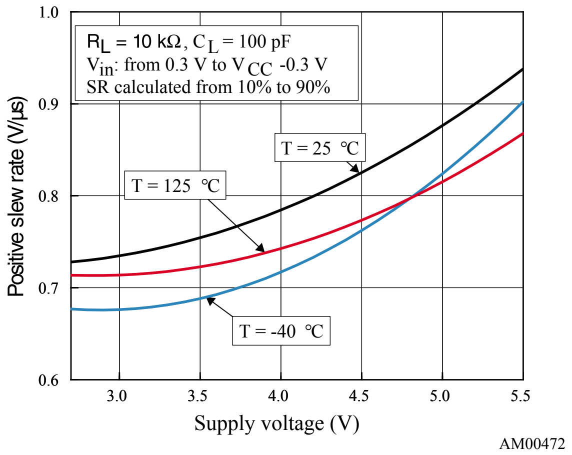


Figure 15. Negative slew rate vs. supply voltage

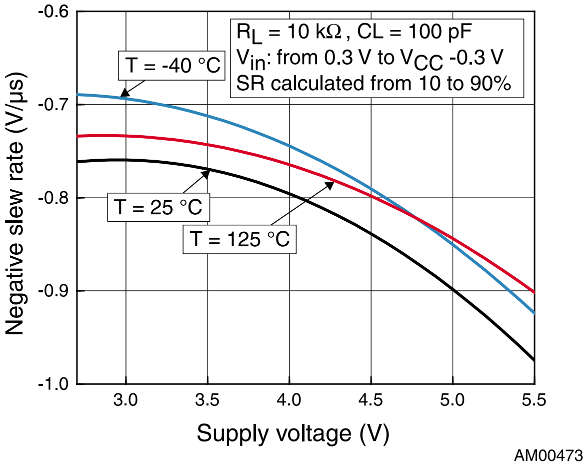


Figure 16. THD+N vs. frequency at V_{CC} = 2.7 V

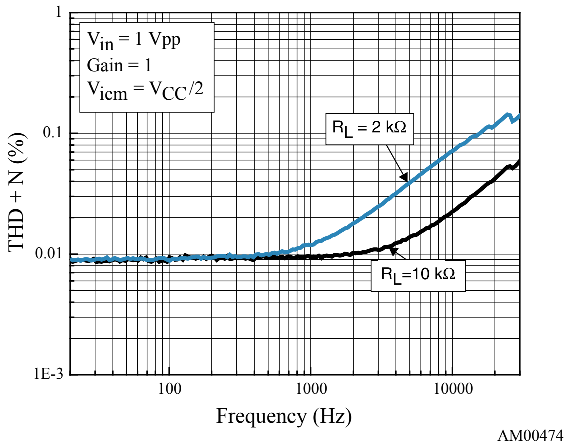


Figure 17. THD+N vs. frequency at V_{CC} = 5.5 V

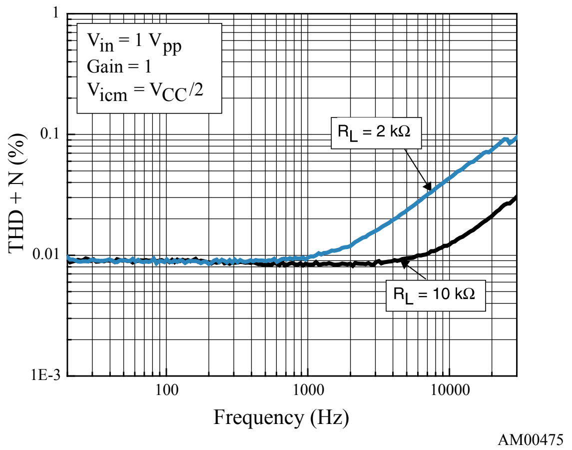


Figure 18. THD+N vs. output voltage at V_{CC} = 2.7 V

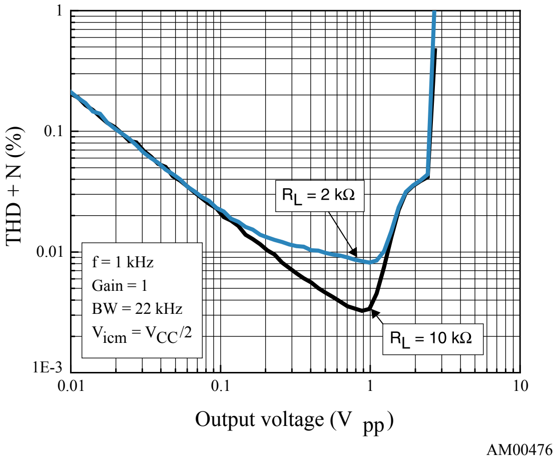


Figure 19. THD+N vs. output voltage at V_{CC} = 5.5 V

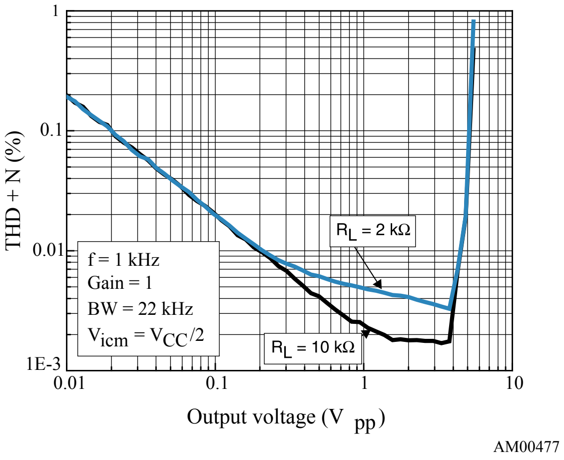


Figure 20. Output impedance versus frequency in closed-loop configuration

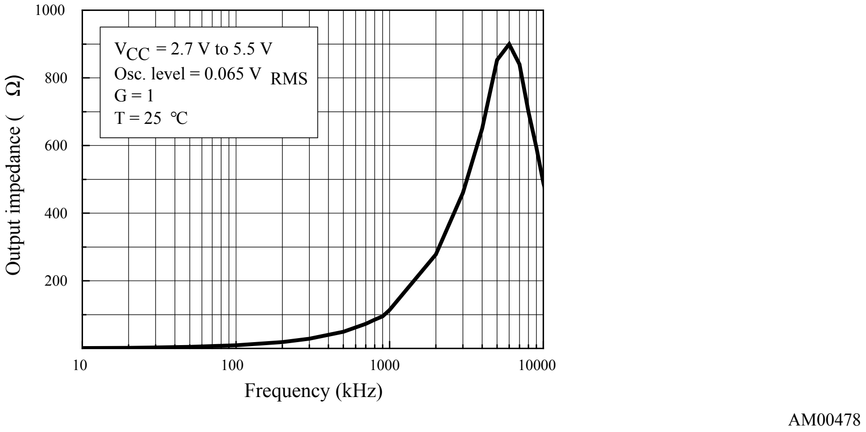


Figure 21. Response to a 100 mV input step for gain = 1 at V_{CC} = 5.5 V rising edge

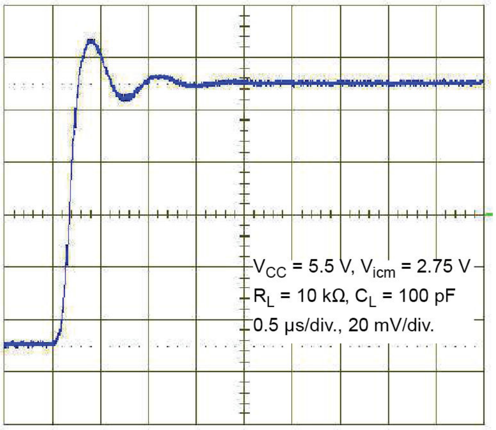


Figure 22. Response to a 100 mV input step for gain = 1 at V_{CC} = 5.5 V falling edge

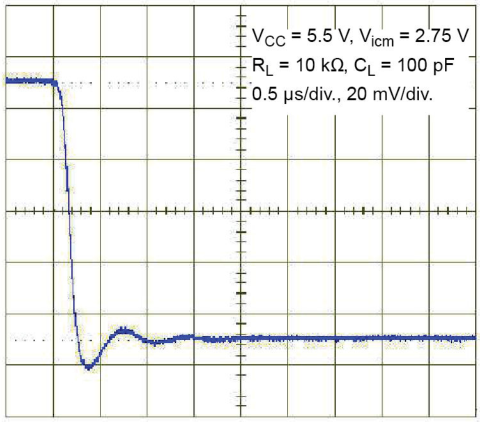


Figure 23. PSRR vs. frequency at V_{CC} = 2.7 V

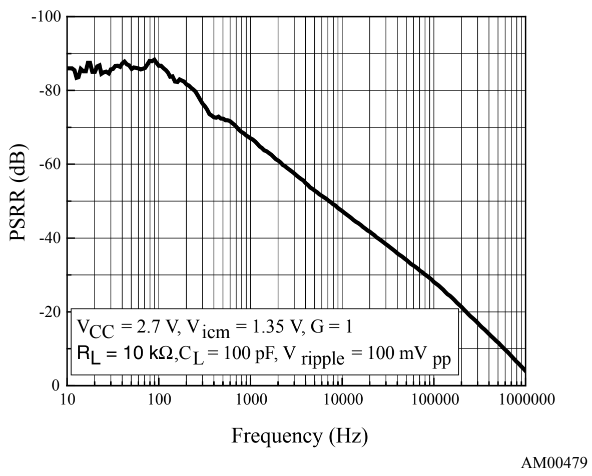
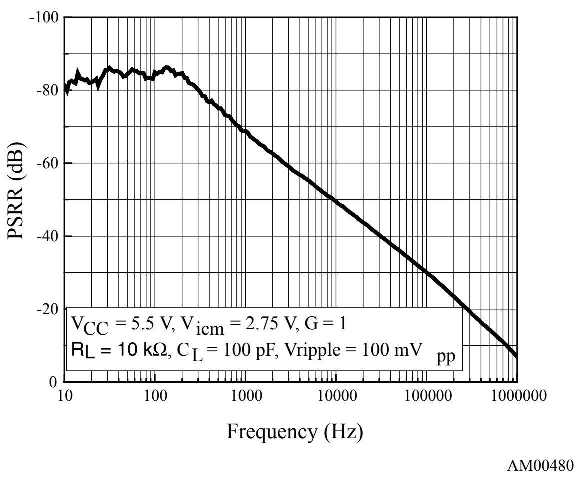


Figure 24. PSRR vs. frequency at V_{CC} = 5.5 V



5 Application information

5.1 Operating voltages

The amplifiers of the TSV52x, TSV52xA series can operate from 2.7 V to 5.5 V. Their parameters are fully specified for 2.7 V, 3.3 V and 5 V power supplies. However, the parameters are very stable in the full V_{CC} range, and several characterization curves show the TSV52x, TSV52xA device characteristics at 2.7 V. Additionally, the main specifications are guaranteed in extended temperature ranges from -40 to +125 °C.

5.2 Common-mode voltage range

The TSV52x, TSV52xA devices are built with two complementary PMOS and NMOS input differential pairs. The devices have a rail-to-rail input, and the input common-mode range is extended from V_{CC-} - 0.1 V to V_{CC+} + 0.1 V.

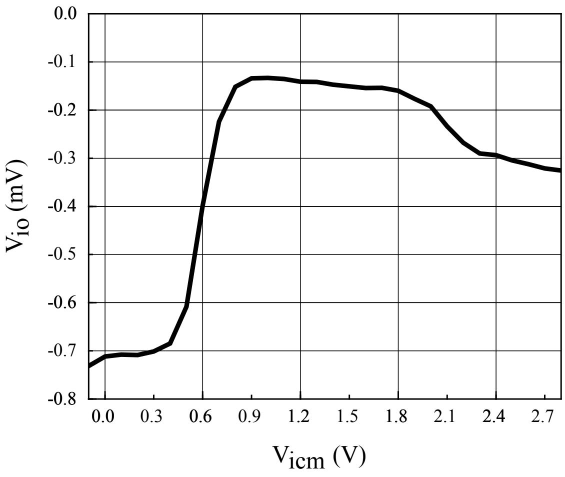
The N channel pair is active for input voltage close to the positive rail typically (V_{CC+} - 0.7 V) to 100 mv above the positive rail.

The P channel pair is active for input voltage close to the negative rail typically 100 mV below the negative rail to V_{CC-} + 0.7 V.

And between V_{CC-} + 0.7 V and V_{CC+} - 0.7 V both N and P pairs are active.

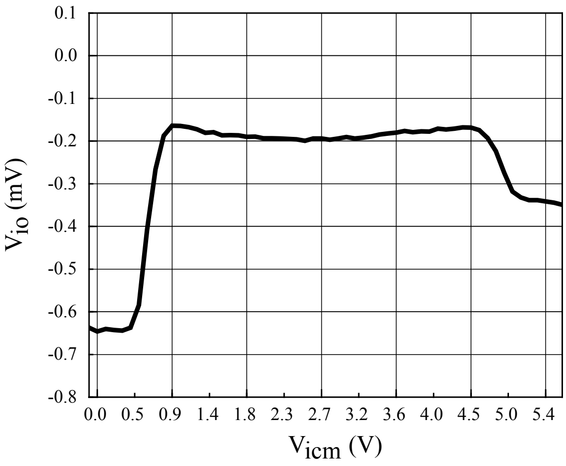
When both pairs work together it allows to increase the speed of the TSV52x, TSV52xA devices. This architecture improves the merit factor of the whole device. In the transition region, the performance of CMR, SVR, V_{io} (Figure 25 and Figure 26) and THD is slightly degraded.

Figure 25. Input offset voltage vs. input common-mode at V_{CC} = 2.7 V



AM00481

Figure 26. Input offset voltage vs. input common-mode at V_{CC} = 5.5 V



AM00482

5.3 Rail-to-rail input

The TSV52x, TSV52xA series are guaranteed without phase reversal as shown in Figure 28.

It is extremely important that the current flowing in the input pin does not exceed 10 mA. In order to limit this current, a serial resistor can be added on the V_{in} path.

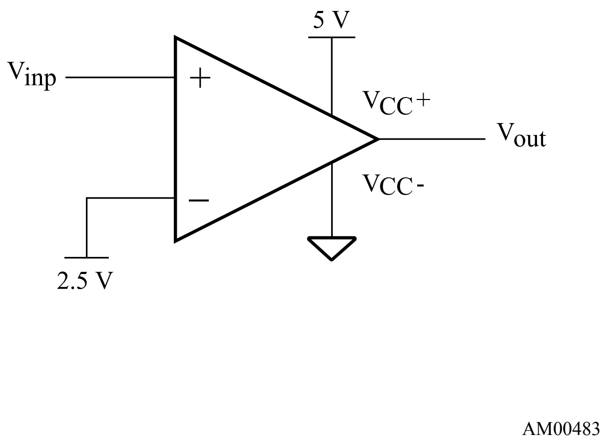


Figure 27. Phase reversal test schematic

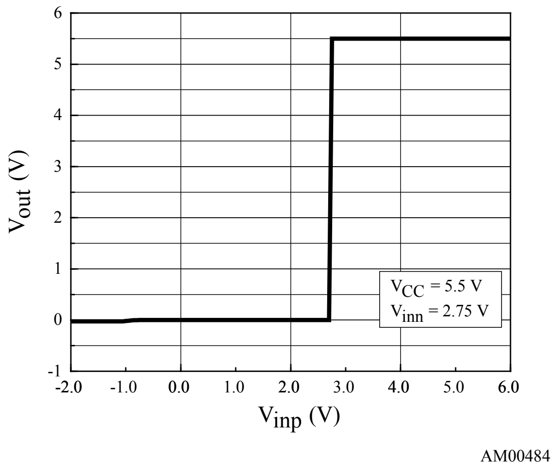


Figure 28. No phase reversal

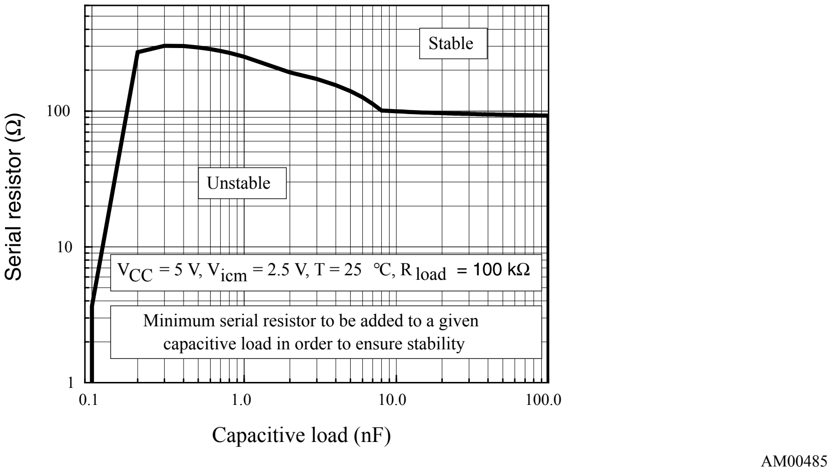
5.4 Rail-to-rail output

The operational amplifier output levels can go close to the rails: 35 mV maximum above and below the rail when connected to a 10 kΩ resistive load to $V_{CC}/2$.

5.5 Driving resistive and capacitive loads

To drive high capacitive loads, adding an in-series resistor at the output can improve the stability of the device (see Figure 29 for the recommended in series value). Once the in-series resistor has been selected, the stability of the circuit should be tested on the bench and simulated with simulation models. The R_{load} is placed in parallel with the capacitive load. The R_{load} and the in-series resistor create a voltage divider which introduces an error proportional to the ratio R_s/R_{load}. By keeping R_s as low as possible, this error is generally negligible.

Figure 29. In-series resistor versus capacitive load



5.6 Input offset voltage drift over the temperature

The maximum input voltage drift over the temperature variation is defined as the offset variation related to offset value measured at 25 °C. The operational amplifier is one of the main circuits of the signal conditioning chain, and the amplifier input offset is a major contributor to the chain accuracy. The signal chain accuracy at 25 °C can be compensated during production at application level. The maximum input voltage drift over temperature enables the system designer to anticipate the effect of temperature variations.

The maximum input voltage drift over temperature is computed using Equation 1.

$$\frac{\Delta V_{io}}{\Delta T} = max\left|\frac{V_{io}(T) - V_{io}(25°C)}{T - 25°C}\right|_{T\,=\,-40°C \; and \; T\,=\,125°C} \quad (1)$$

The datasheet maximum value is guaranteed by a measurement on a representative sample size ensuring a C_{pk} (process capability index) greater than 1.33.

5.7 Long term input offset voltage drift

To evaluate product reliability, two types of stress acceleration are used:

- Voltage acceleration, by changing the applied voltage
- Temperature acceleration, by changing the die temperature (below the maximum junction temperature allowed by the technology) with the ambient temperature.

The voltage acceleration has been defined based on JEDEC results, and is defined using Equation 2

$$A_{FV} = e^{\beta\,.\,(V_S - V_U)} \quad (2)$$

Where:

A_{FV} is the voltage acceleration factor

β is the voltage acceleration constant in 1/V, constant technology parameter (β = 1)

V_S is the stress voltage used for the accelerated test

V_U is the voltage used for the application

The temperature acceleration is driven by the Arrhenius model, and is defined in Equation 3.

$$A_{FT} = e^{\frac{E_a}{k}\cdot\left(\frac{1}{T_U} - \frac{1}{T_S}\right)} \quad (3)$$

Where:

A_{FT} is the temperature acceleration factor

E_a is the activation energy of the technology based on the failure rate

k is the Boltzmann constant (8.6173×10^{-5} eV . K^{-1})

T_U is the temperature of the die when V_U is used (K)

T_S is the temperature of the die under temperature stress (K)

The final acceleration factor, A_F, is the multiplication of the voltage acceleration factor and the temperature acceleration factor (Equation 4).

$$A_F = A_{FT}\,.\,A_{FV} \quad (4)$$

A_F is calculated using the temperature and voltage defined in the mission profile of the product. The A_F value can then be used in Equation x to calculate the number of months of use equivalent to 1000 hours of reliable stress duration.

Months = A_F × 1000 h × 12 months / (24 h × 365.25 days)

To evaluate the op amp reliability, a follower stress condition is used where V_{CC} is defined as a function of the maximum operating voltage and the absolute maximum rating (as recommended by JEDEC rules). The V_{io} drift (in µV) of the product after 1000 h of stress is tracked with parameters at different measurement conditions (see Equation 5).

$$V_{CC} = max\left(V_{op}\right) \; with \; V_{icm} = \frac{V_{cc}}{2} \quad (5)$$

The long term drift parameter ΔV_{io} (in µV.$month^{-1/2}$), estimating the reliability performance of the product, is obtained using the ratio of the V_{io} (input offset voltage value) drift over the square root of the calculated number of months (Equation 7).

$$\Delta V_{io} = \frac{V_{io} drift}{\sqrt{months}} \quad (6)$$

Where V_{io} drift is the measured drift value in the specified test conditions after 1000 h stress duration.

5.8 PCB layouts

For correct operation, it is advised to add 10 nF decoupling capacitors as close as possible to the power supply pins.

5.9 Macromodel

Accurate macromodels of the TSV52x, TSV52xA devices are available on STMicroelectronics™ website at www.st.com. These models are a trade-off between accuracy and complexity (that is, time simulation) of the TSV52x, TSV52xA operational amplifiers. They emulate the nominal performance of a typical device within the specified operating conditions mentioned in the datasheet. They also help to validate a design approach and to select the appropriate operational amplifier, but they do not replace onboard measurements.

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

6.1 SC70-5 (or SOT323-5) package information

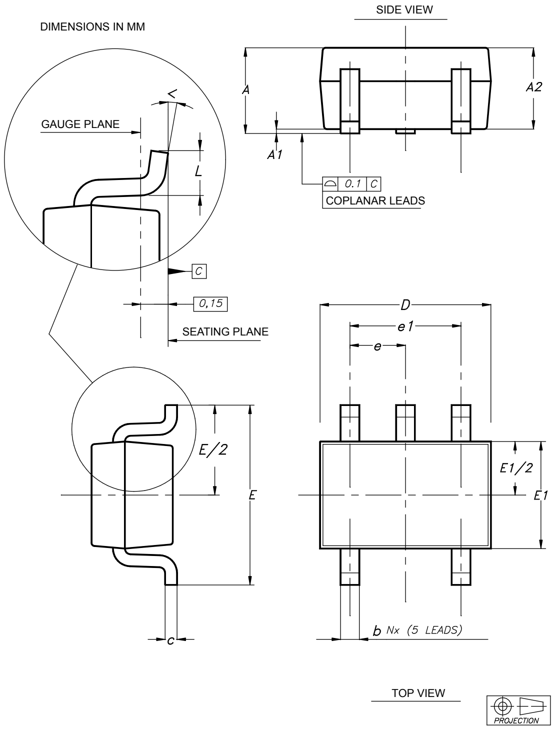


Figure 30. SC70-5 (or SOT323-5) package outline

Table 6. SC70-5 (or SOT323-5) package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80		1.10	0.032		0.043
A1			0.10			0.004
A2	0.80	0.90	1.00	0.032	0.035	0.039
b	0.15		0.30	0.006		0.012
c	0.10		0.22	0.004		0.009
D	1.80	2.00	2.20	0.071	0.079	0.087
E	1.80	2.10	2.40	0.071	0.083	0.094
E1	1.15	1.25	1.35	0.045	0.049	0.053
e		0.65			0.025	
e1		1.30			0.051	
L	0.26	0.36	0.46	0.010	0.014	0.018
<	0°		8°	0°		8°

6.2 DFN8 2x2 package information

Figure 31. **DFN8 2x2 package outline**

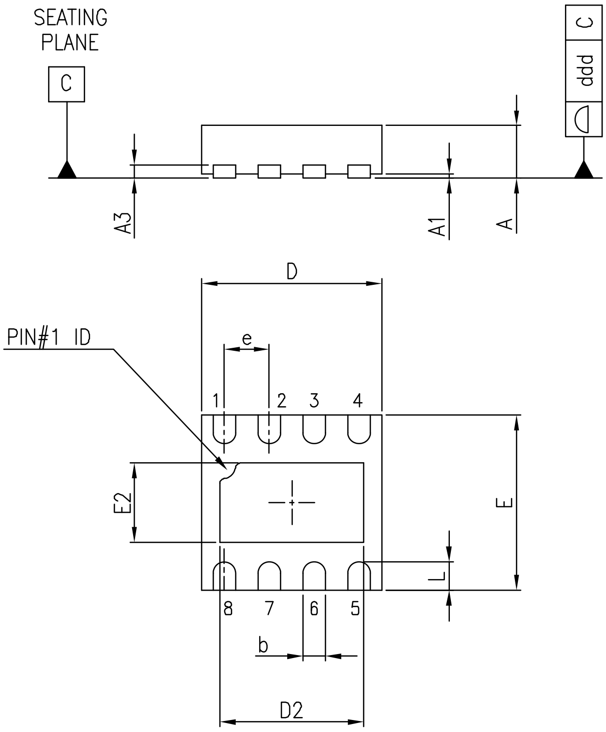
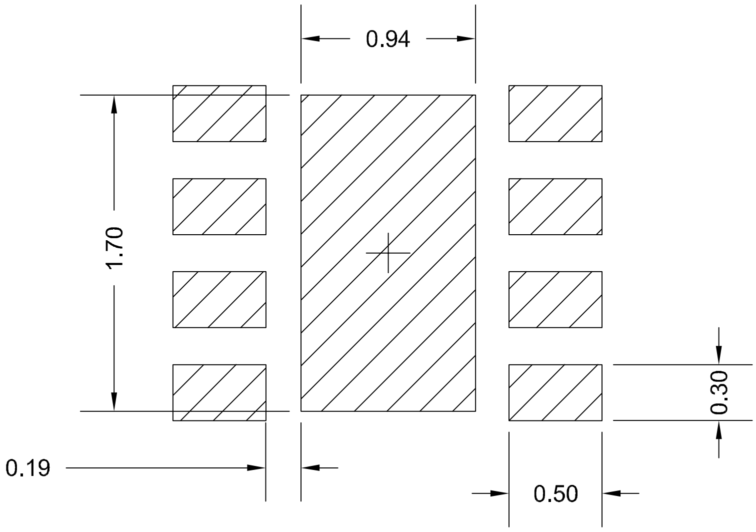


Table 7. **DFN8 2x2 package mechanical data**

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.51	0.55	0.60	0.020	0.022	0.024
A1			0.05			0.002
A3		0.15			0.006	
b	0.18	0.25	0.30	0.007	0.010	0.012
D	1.85	2.00	2.15	0.073	0.079	0.085
D2	1.45	1.60	1.70	0.057	0.063	0.067
E	1.85	2.00	2.15	0.073	0.079	0.085
E2	0.75	0.90	1.00	0.030	0.035	0.039
e		0.50			0.020	
L	0.225	0.325	0.425	0.009	0.013	0.017
ddd			0.08			0.003

Figure 32. **DFN8 2x2 recommended footprint**



6.3 MiniSO8 package information

Figure 33. MiniSO8 package outline

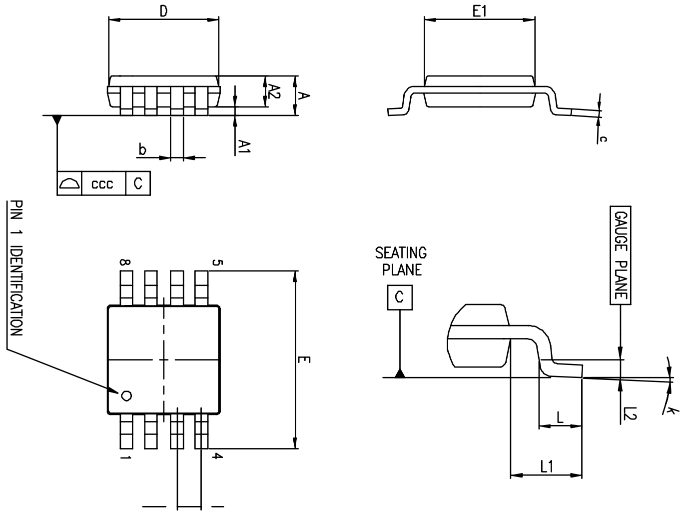


Table 8. MiniSO8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.1			0.043
A1	0		0.15	0		0.0006
A2	0.75	0.85	0.95	0.030	0.033	0.037
b	0.22		0.40	0.009		0.016
c	0.08		0.23	0.003		0.009
D	2.80	3.00	3.20	0.11	0.118	0.126
E	4.65	4.90	5.15	0.183	0.193	0.203
E1	2.80	3.00	3.10	0.11	0.118	0.122
e		0.65			0.026	
L	0.40	0.60	0.80	0.016	0.024	0.031
L1		0.95			0.037	
L2		0.25			0.010	
k	0°		8°	0°		8°
ccc			0.10			0.004

6.4 SO8 package information

Figure 34. SO8 package outline

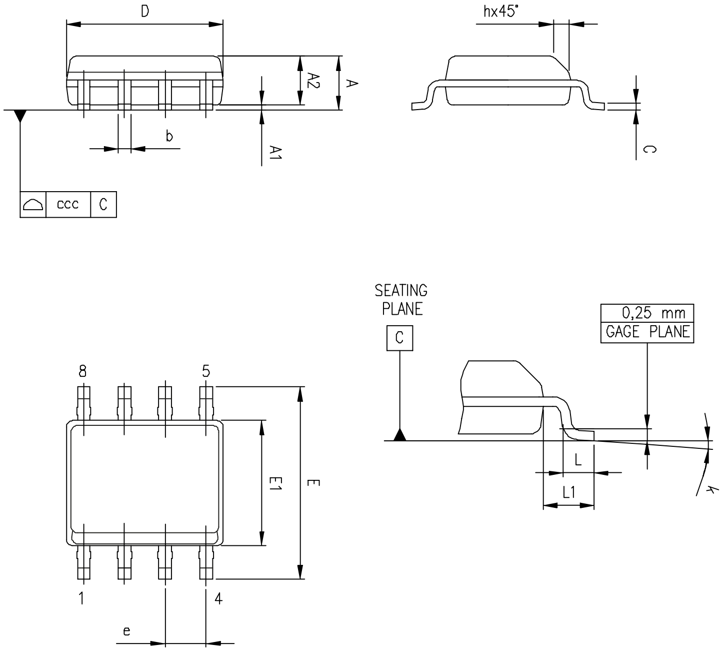


Table 9. SO-8 mechanical data

Dim.	mm			Inches		
	Min.	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**
A			1.75			0.069
A1	0.1		0.25	0.004		0.01
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
c	0.17		0.23	0.007		0.01
D	4.8	4.9	5	0.189	0.193	0.197
E	5.8	6	6.2	0.228	0.236	0.244
E1	3.8	3.9	4	0.15	0.154	0.157
e		1.27			0.05	
h	0.25		0.5	0.01		0.02
L	0.4		1.27	0.016		0.05
L1		1.04			0.04	
k	0		8 °	1 °		8 °
ccc			0.1			0.004

6.5 TSSOP14 package information

Figure 35. TSSOP14 package outline

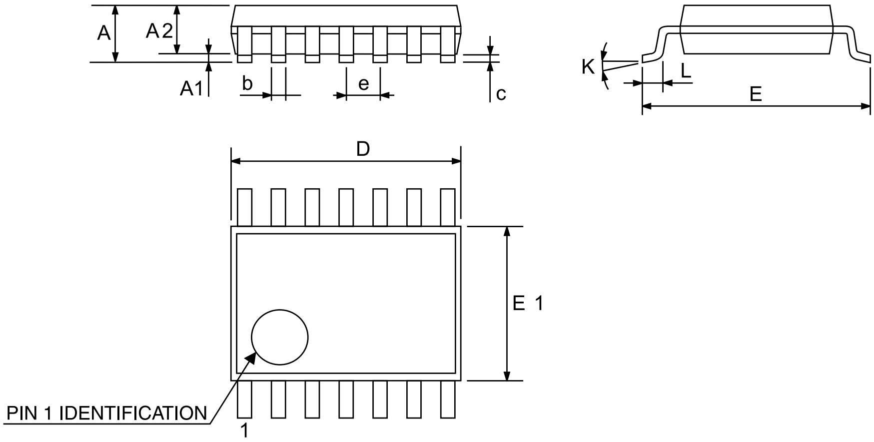


Table 10. TSSOP14 package mechanical data

Symbol	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L1	0.45	0.60	0.75	0.018	0.024	0.030

6.6 QFN16 3x3 wettable flank package information

Figure 36. **QFN16 3x3 mm wettable flank drawing outline**

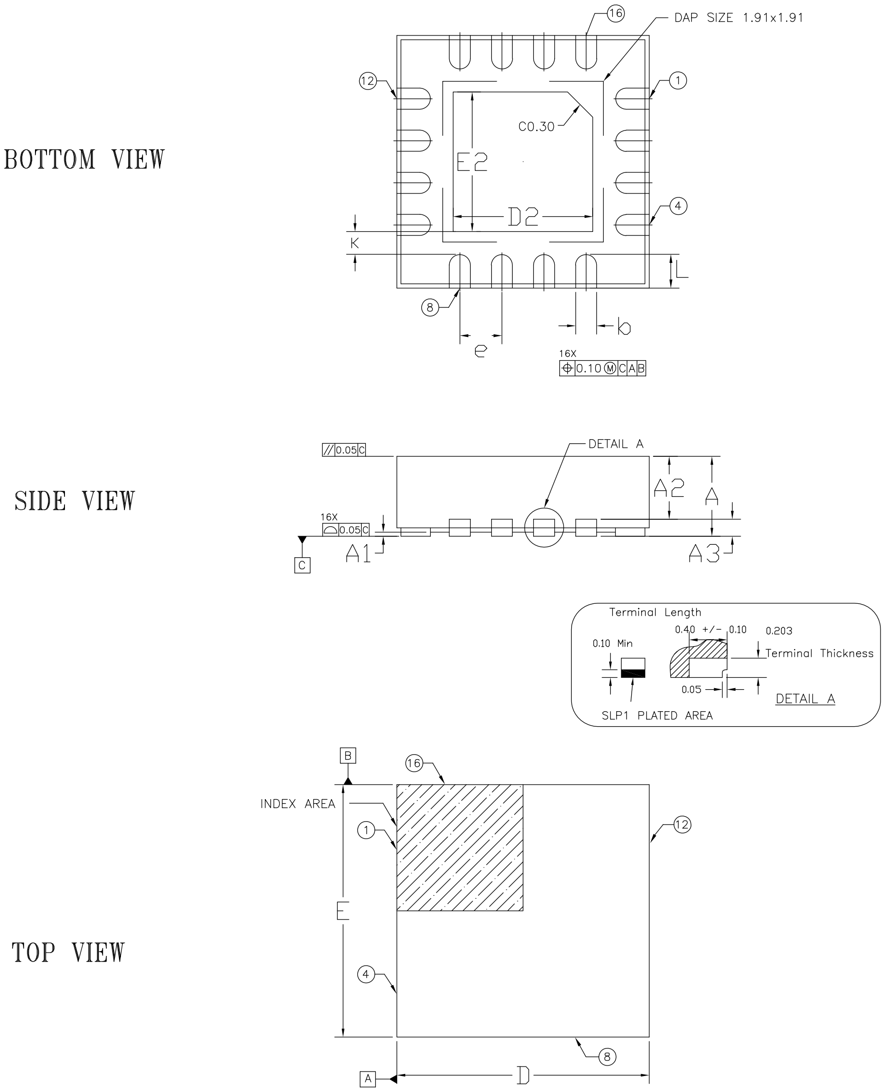
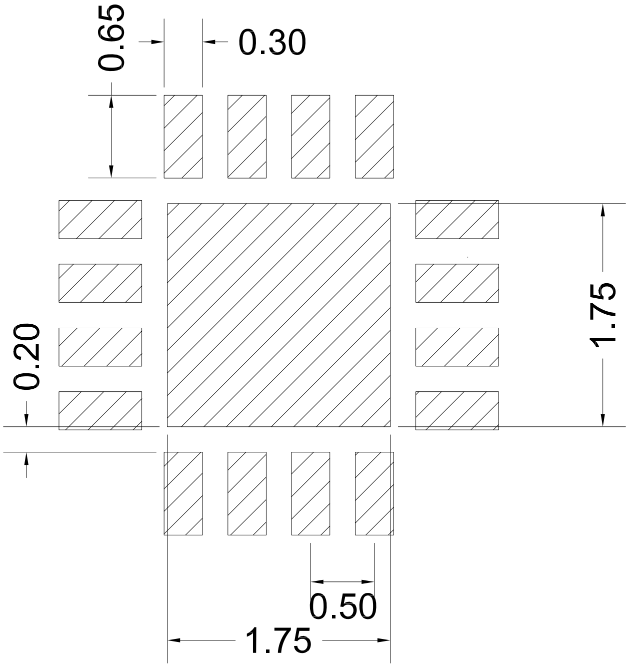


Table 11. **QFN16 3x3 wettable flank mechanical data**

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0,90	0,95	1,00	0,035	0,037	0,039
A1	0,00		0,05	0,000		0,002
A2		0,75			0,030	
A3		0,20			0,008	
b	0,20	0,25	0,30	0,008	0,010	0,012
D		3,00			0,118	
E		3,00			0,118	
e		0,50			0,020	
D2	1,56	1,66	1,76	0,061	0,065	0,069
E2	1,56	1,66	1,76	0,061	0,065	0,069
K		0,27			0,011	
L	0,30	0,40	0,50	0,012	0,016	0,020

Figure 37. **QFN16 3x3 wettable flank recommended footprint**



7 Ordering information

Table 12. **Order codes**

Order code	Temperature range	Package	Packing	Marking
TSV521ICT	-40 to 125 °C	SC70-	Tape and reel	K1G
TSV522IQ2T		DFN82 x 2		K1G
TSV522IST		MiniSO8		K1G
TSV524IQ4T		QFN163 x 3		K1G
TSV524IPT		TSSOP14		TSV524
TSV522IYST	-40 to 125 °C Automotive grade (1)	MiniSO8		K1H
TSV524IYPT		TSSOP14		TSV524Y
TSV521AICT	-40 to 125 °C	SC70-5		K1K
TSV522AIQ2T		DFN82 x 2		K1K
TSV522AIST		MiniSO8		K1K
TSV524AIQ4T		QFN163 x 3		K1K
TSV524AIPT		TSSOP14		TSV524A
TSV522AIYST	-40 to 125 °C Automotive grade(1)	MiniSO8		K1L
TSV524AIYPT		TSSOP14		TSV524AY

1. *Qualification and characterization according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 and Q 002 or equivalent.*

Revision history

Table 13. **Document revision history**

Date	Revision	Changes
19-Jun-2012	1	Initial release.
31-Jan-2014	2	Updated information of “Related products” “Figure1: Pin connections for each package (top view)”: added footnote 1. “Section4: Application information”: updated text to make it more readable “Table 12”: updated automotive footnotes.
12-Apr-2017	3	Updated Table 8: “L” dimension changed from 0.5 mm to 0.425 mm.
28-Nov-2023	4	Updated title and package figure on the cover page. Updated stylesheet and template.

Contents

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