



# STP17NK40Z - STP17NK40ZFP

N-CHANNEL 400V - 0.23Ω - 15A TO-220/TO-220FP

Zener-Protected SuperMESH™ Power MOSFET

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>	P <sub>w</sub>
STP17NK40Z	400 V	< 0.25 Ω	15 A	150 W
STP17NK40ZFP	400 V	< 0.25 Ω	15 A	35 W

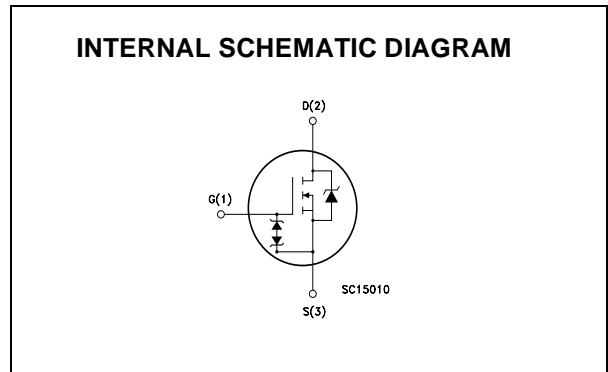
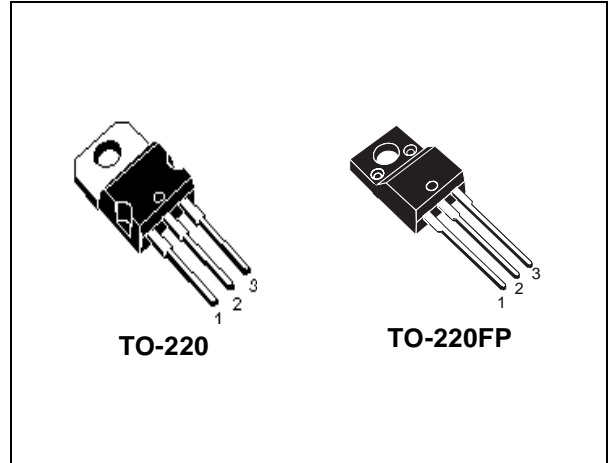
- TYPICAL R<sub>DS(on)</sub> = 0.23 Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- GATE CHARGE MINIMIZED
- VERY LOW INTRINSIC CAPACITANCES
- VERY GOOD MANUFACTURING REPEATIBILITY

## DESCRIPTION

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.

## APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- IDEAL FOR OFF-LINE POWER SUPPLIES, ADAPTORS AND PFC
- LIGHTING



## ORDERING INFORMATION

SALES TYPE	MARKING	PACKAGE	PACKAGING
STP17NK40Z	P17NK40Z	TO-220	TUBE
STP17NK40ZFP	P17NK40ZFP	TO-220FP	TUBE

## STP17NK40Z - STP17NK40ZFP

### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
		STP17NK40Z	STP17NK40ZFP	
V <sub>DS</sub>	Drain-source Voltage (V <sub>GS</sub> = 0)	400		V
V <sub>DGR</sub>	Drain-gate Voltage (R <sub>GS</sub> = 20 kΩ)	400		V
V <sub>GS</sub>	Gate- source Voltage	± 30		V
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 25°C	15	15 (*)	A
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 100°C	9.4	9.4 (*)	A
I <sub>DM</sub> (•)	Drain Current (pulsed)	60	60 (*)	A
P <sub>TOT</sub>	Total Dissipation at T <sub>C</sub> = 25°C	150	35	W
	Derating Factor	1.2	0.28	W/°C
I <sub>GS</sub>	Gate-source Current (DC)	± 20		mA
V <sub>ESD(G-S)</sub>	Gate source ESD(HBM-C=100pF, R=1.5KΩ)	4500		V
dv/dt (1)	Peak Diode Recovery voltage slope	4.5		V/ns
Viso	Insulation Withstand Voltage (DC)	--	2500	V
T <sub>j</sub> T <sub>stg</sub>	Operating Junction Temperature Storage Temperature	-55 to 150 -55 to 150		°C °C

(•) Pulse width limited by safe operating area

(1) I<sub>SD</sub> ≤ 15A, di/dt ≤ 200A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>, T<sub>j</sub> ≤ T<sub>JMAX</sub>.

(\*) Limited only by maximum temperature allowed

### THERMAL DATA

		TO-220	TO-220FP	
R <sub>thj-case</sub>	Thermal Resistance Junction-case Max	0.83	3.6	°C/W
R <sub>thj-amb</sub>	Thermal Resistance Junction-ambient Max	62.5		°C/W
T <sub>I</sub>	Maximum Lead Temperature For Soldering Purpose	300		°C

### AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I <sub>AR</sub>	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T <sub>j</sub> max)	15	A
E <sub>AS</sub>	Single Pulse Avalanche Energy (starting T <sub>j</sub> = 25 °C, I <sub>D</sub> = I <sub>AR</sub> , V <sub>DD</sub> = 50 V)	450	mJ

### GATE-SOURCE ZENER DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV <sub>GSO</sub>	Gate-Source Breakdown Voltage	I <sub>GS</sub> = ± 1mA (Open Drain)	30			V

### PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

**ELECTRICAL CHARACTERISTICS** ( $T_{CASE} = 25^{\circ}C$  UNLESS OTHERWISE SPECIFIED)  
 ON/OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 1 \text{ mA}, V_{GS} = 0$	400			V
$I_{DSS}$	Zero Gate Voltage Drain Current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}, T_C = 125^{\circ}C$			1 50	$\mu A$ $\mu A$
$I_{GSS}$	Gate-body Leakage Current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20 \text{ V}$			$\pm 10$	$\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 100 \mu A$	3	3.75	4.5	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 7.5 \text{ A}$		0.23	0.25	$\Omega$

## DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs} (1)$	Forward Transconductance	$V_{DS} = 15 \text{ V}, I_D = 7.5 \text{ A}$		10.6		S
$C_{iss}$ $C_{oss}$ $C_{rss}$	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25 \text{ V}, f = 1 \text{ MHz}, V_{GS} = 0$		1900 271 63		pF pF pF
$C_{oss \text{ eq.}} (3)$	Equivalent Output Capacitance	$V_{GS} = 0 \text{ V}, V_{DS} = 0 \text{ V to } 400 \text{ V}$		175		pF

## SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ $t_r$	Turn-on Delay Time Rise Time	$V_{DD} = 200 \text{ V}, I_D = 7.5 \text{ A}$ $R_G = 4.7 \Omega, V_{GS} = 10 \text{ V}$ (Resistive Load see, Figure 3)		25 23		ns ns
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 320 \text{ V}, I_D = 15 \text{ A},$ $V_{GS} = 10 \text{ V}$		65 13 35		nC nC nC

## SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ $t_f$	Turn-off Delay Time Fall Time	$V_{DD} = 200 \text{ V}, I_D = 7.5 \text{ A}$ $R_G = 4.7 \Omega, V_{GS} = 10 \text{ V}$ (Resistive Load see, Figure 3)		55 13		ns ns
$t_{r(voff)}$ $t_f$ $t_c$	Off-voltage Rise Time Fall Time Cross-over Time	$V_{DD} = 320 \text{ V}, I_D = 15 \text{ A},$ $R_G = 4.7 \Omega, V_{GS} = 10 \text{ V}$ (Inductive Load see, Figure 5)		12 13 25		ns ns ns

## SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$ $I_{SDM} (2)$	Source-drain Current Source-drain Current (pulsed)				15 60	A A
$V_{SD} (1)$	Forward On Voltage	$I_{SD} = 15 \text{ A}, V_{GS} = 0$			1.6	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 15 \text{ A}, di/dt = 100 \text{ A}/\mu s$ $V_{DD} = 100 \text{ V}, T_j = 150^{\circ}C$ (see test circuit, Figure 5)		332 2650 16		ns nC A

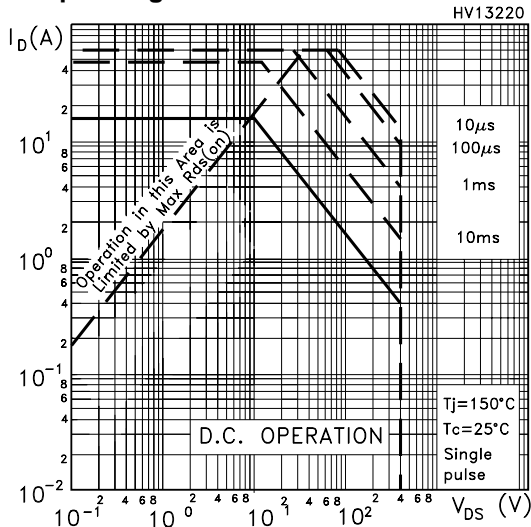
Note: 1. Pulsed: Pulse duration = 300  $\mu s$ , duty cycle 1.5 %.

2. Pulse width limited by safe operating area.

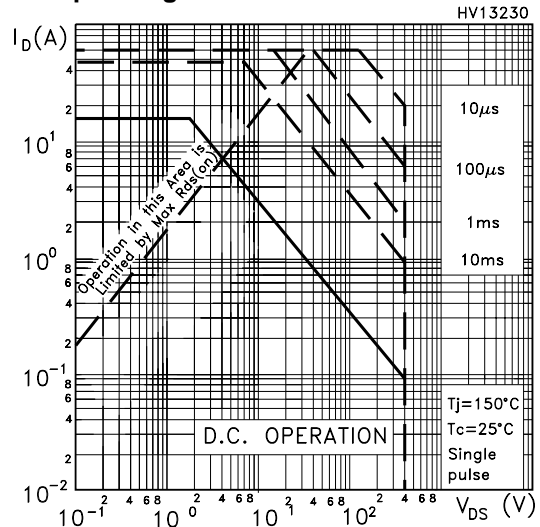
3.  $C_{oss \text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ .

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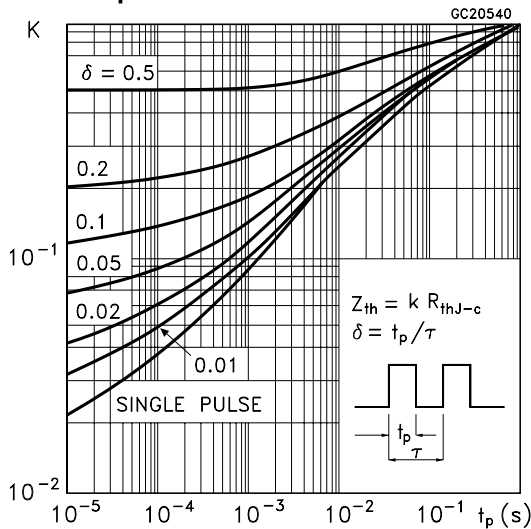
### Safe Operating Area For TO-220



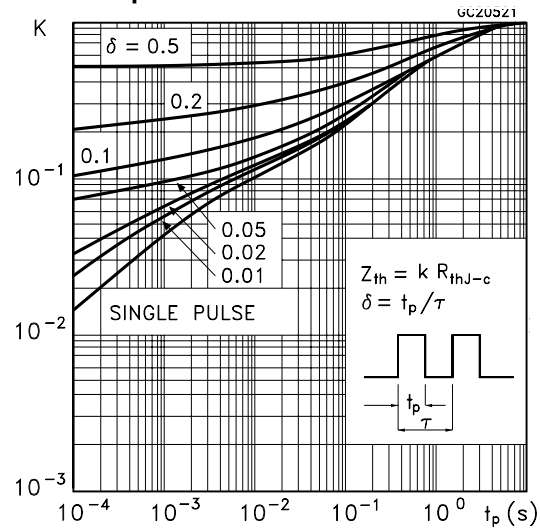
### Safe Operating Area For TO-220FP



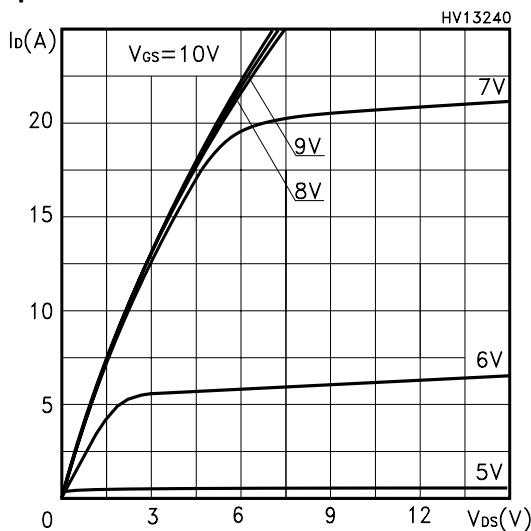
### Thermal Impedance For TO-220



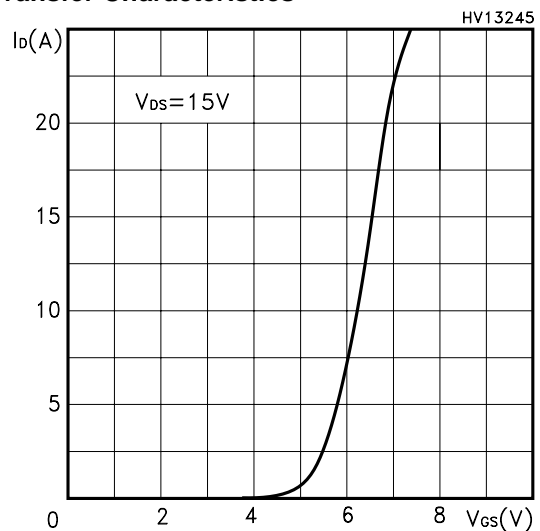
### Thermal Impedance For TO-220FP



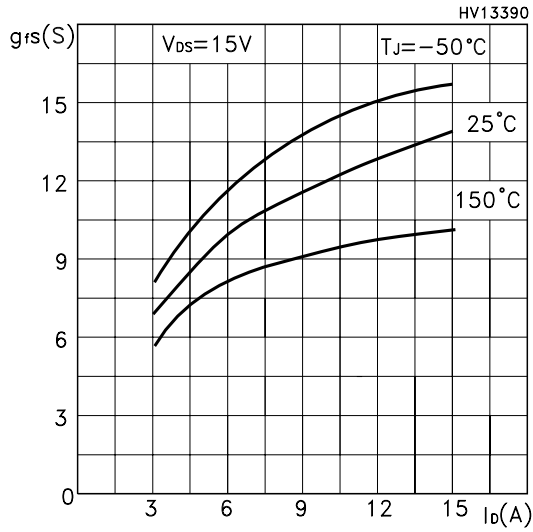
### Output Characteristics



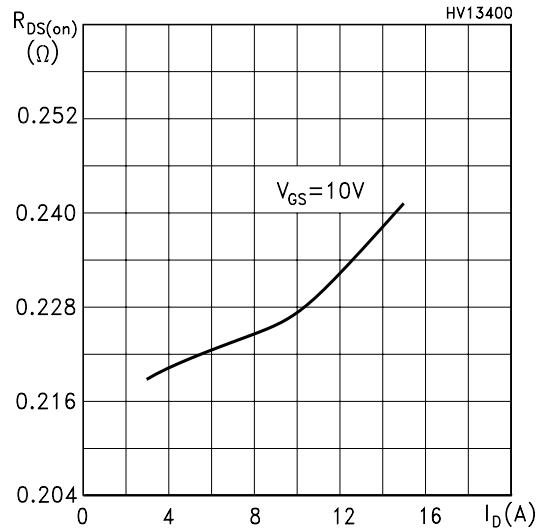
### Transfer Characteristics



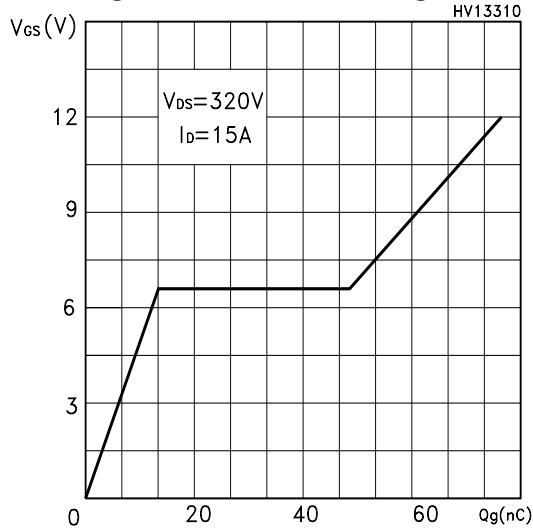
Transconductance



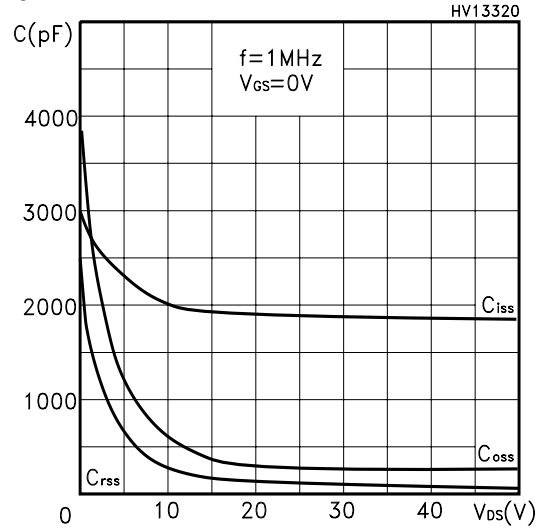
Static Drain-source On Resistance



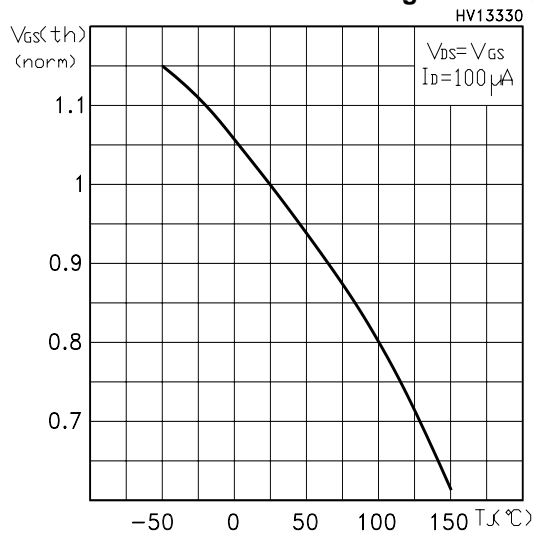
Gate Charge vs Gate-source Voltage



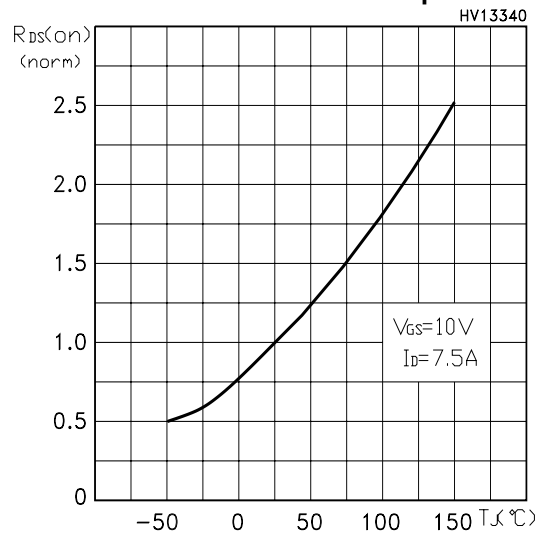
Capacitance Variations



Normalized Gate Threshold Voltage vs Temp.

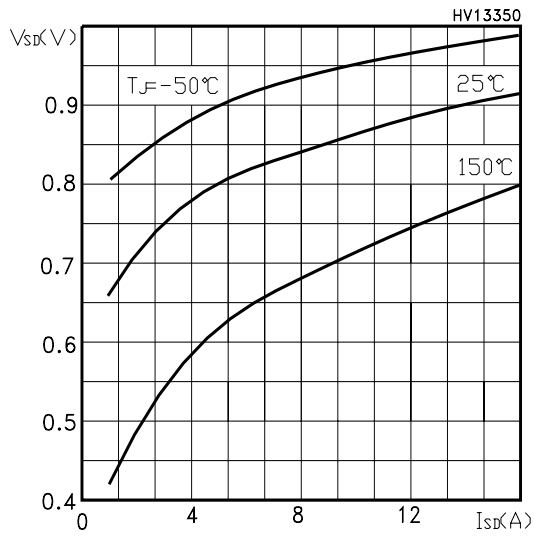


Normalized On Resistance vs Temperature

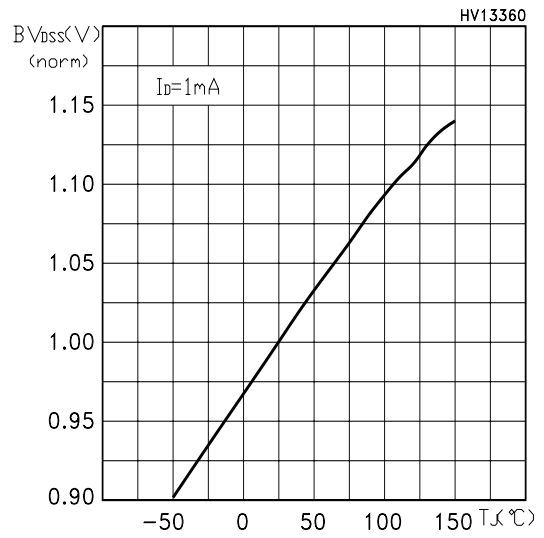


# STP17NK40Z - STP17NK40ZFP

**Source-drain Diode Forward Characteristics**



**Normalized BVDSS vs Temperature**



**Maximum Avalanche Energy vs Temperature**

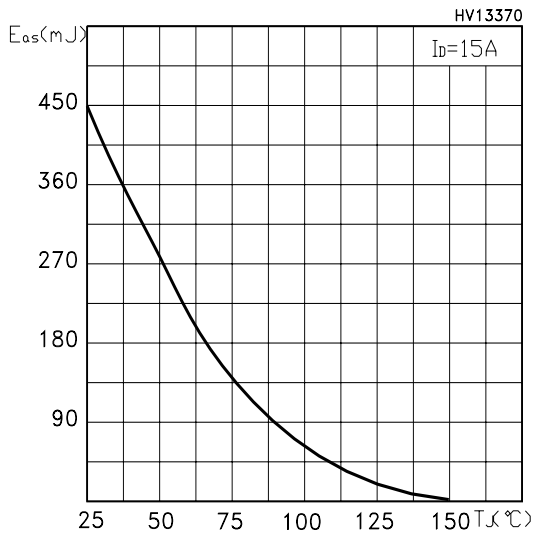


Fig. 1: Unclamped Inductive Load Test Circuit

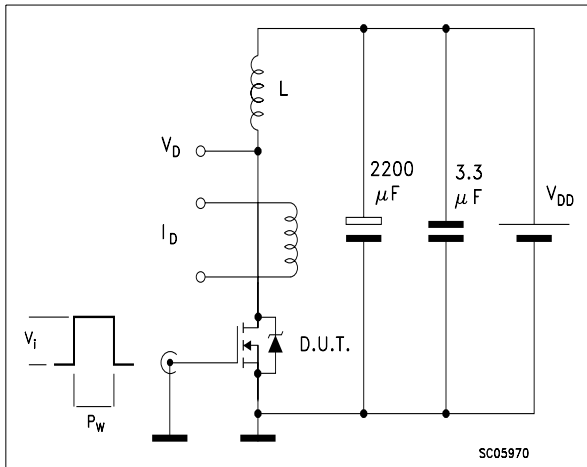


Fig. 2: Unclamped Inductive Waveform

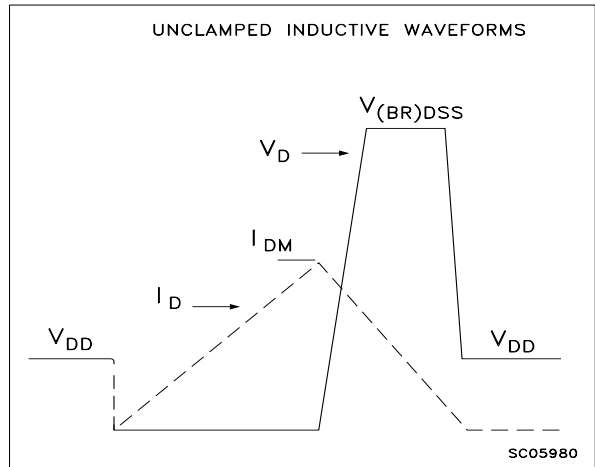


Fig. 3: Switching Times Test Circuit For Resistive Load

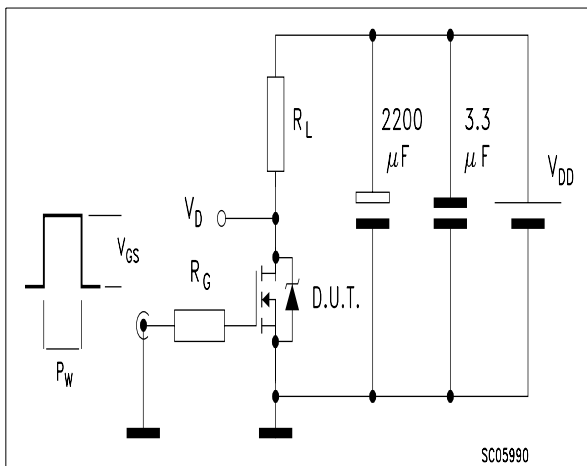


Fig. 4: Gate Charge test Circuit

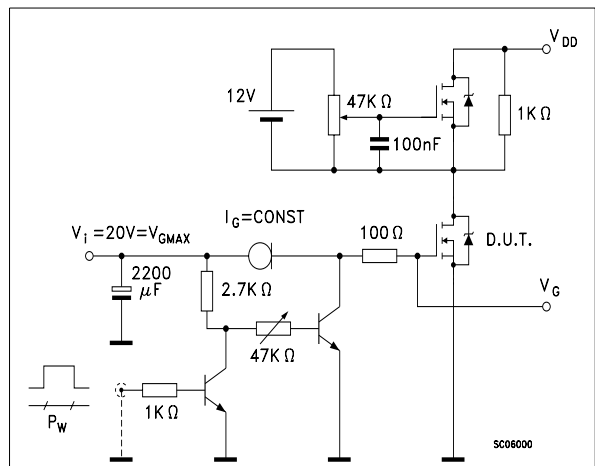
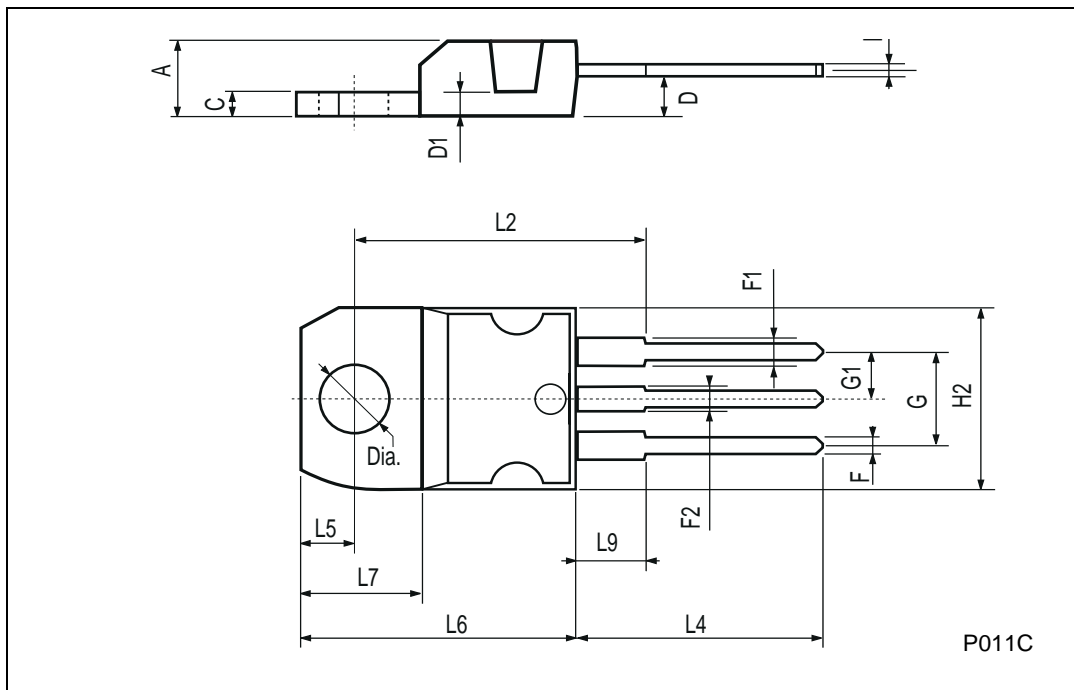


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



TO-220 MECHANICAL DATA

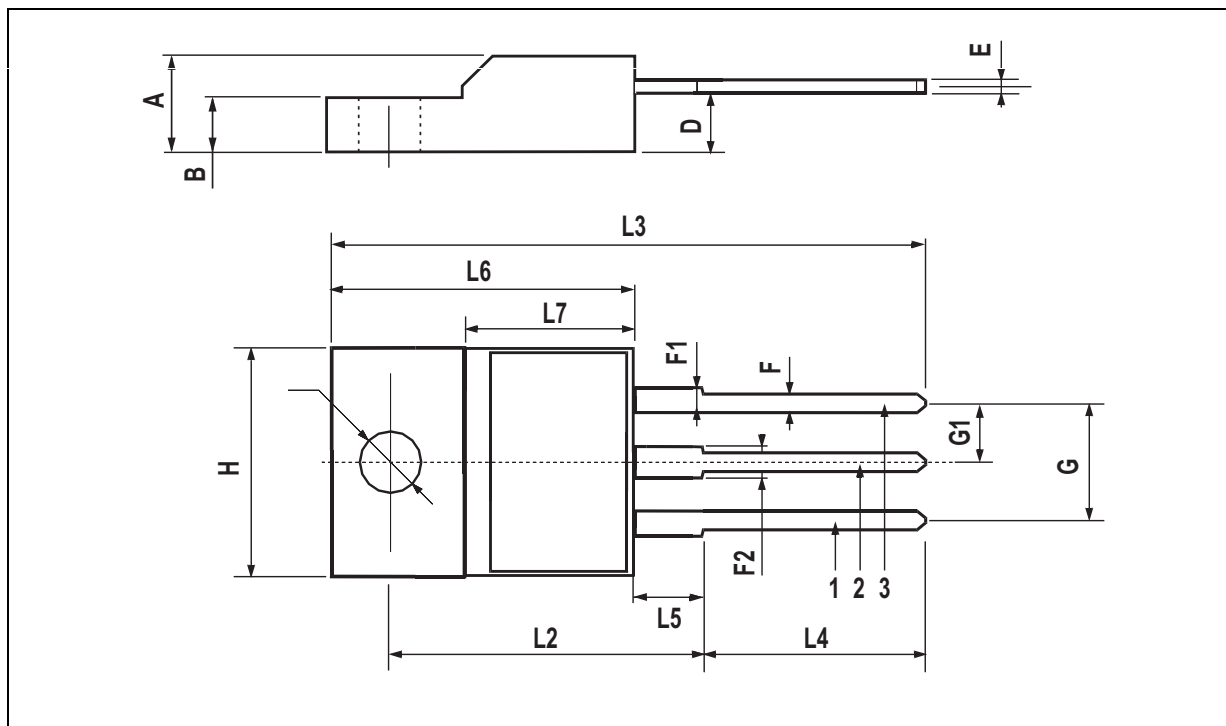
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
C	1.23		1.32	0.048		0.051
D	2.40		2.72	0.094		0.107
D1		1.27			0.050	
E	0.49		0.70	0.019		0.027
F	0.61		0.88	0.024		0.034
F1	1.14		1.70	0.044		0.067
F2	1.14		1.70	0.044		0.067
G	4.95		5.15	0.194		0.203
G1	2.4		2.7	0.094		0.106
H2	10.0		10.40	0.393		0.409
L2		16.4			0.645	
L4	13.0		14.0	0.511		0.551
L5	2.65		2.95	0.104		0.116
L6	15.25		15.75	0.600		0.620
L7	6.2		6.6	0.244		0.260
L9	3.5		3.93	0.137		0.154
DIA.	3.75		3.85	0.147		0.151





**TO-220FP MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.5	0.045		0.067
F2	1.15		1.5	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	.0385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
∅	3		3.2	0.118		0.126



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