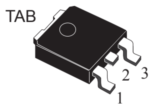
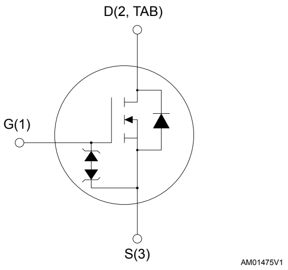
STD5N80K5

Datasheet

# N-channel 800 V, 1.50 Ω typ., 4 A MDmesh K5 Power MOSFET in a DPAK package




DPAK




## Features

| Order code | $V_{DS}$ | $R_{DS(on)}$ max. | $I_D$ |
|---|---|---|---|
| STD5N80K5 | 800 V | 1.75 Ω | 4 A |

- Industry's lowest $R_{DS(on)}$ x area
- Industry's best FoM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

## Applications

- Switching applications

## Description

This very high voltage N-channel Power MOSFET is designed using MDmesh K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

| Product status link |
|---|
| STD5N80K5 |

| Product summary | |
|---|---|
| **Order code** | STD5N80K5 |
| **Marking** | 5N80K5 |
| **Package** | DPAK |
| **Packing** | Tape and reel |



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# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{GS}$ | Gate-source voltage | ±30 | V |
| $I_D$ | Drain current (continuous) at $T_C$ = 25 °C | 4 | A |
| $I_D$ | Drain current (continuous) at $T_C$ = 100 °C | 2.3 | A |
| $I_{DM}$ (1) | Drain current (pulsed) | 16 | A |
| $P_{TOT}$ | Total power dissipation at $T_C$ = 25 °C | 60 | W |
| dv/dt (2) | Peak diode recovery voltage slope | 4.5 | V/ns |
| dv/dt (3) | MOSFET dv/dt ruggedness | 50 | |
| $T_J$ | Operating junction temperature range | - 55 to 150 | °C |
| $T_{stg}$ | Storage temperature range | | |

1. *Pulse width limited by safe operating area.*
2. *$I_{SD}$ ≤ 4 A, di/dt =100 A/µs; $V_{DS}$ (peak) < $V_{(BR)DSS}$, $V_{DD}$ = 640 V.*
3. *$V_{DS}$ ≤ 640 V.*

**Table 2. Thermal data**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{thj-case}$ | Thermal resistance junction-case | 2.08 | °C/W |
| $R_{thj-pcb}$ (1) | Thermal resistance junction-pcb | 50 | °C/W |

1. *When mounted on FR-4 board of 1 inch², 2 oz Cu.*

**Table 3. Avalanche characteristics**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $I_{AR}$ | Avalanche current, repetitive or not repetitive (pulse width limited by $T_J$ max) | 1.2 | A |
| $E_{AS}$ | Single pulse avalanche energy (starting $T_J$ = 25 °C, $I_D$ = $I_{AR}$, $V_{DD}$ = 50 V) | 165 | mJ |


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## 2 Electrical characteristics

$T_C$ = 25 °C unless otherwise specified

**Table 4. On/off-state**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $V_{GS}$ = 0 V, $I_D$ = 1 mA | 800 | | | V |
| $I_{DSS}$ | Zero gate voltage drain current | $V_{GS}$ = 0 V, $V_{DS}$ = 800 V | | | 1 | µA |
| | | $V_{GS}$ = 0 V, $V_{DS}$ = 800 V, $T_C$ = 125 °C (1) | | | 50 | |
| $I_{GSS}$ | Gate-body leakage current | $V_{DS}$ = 0 V, $V_{GS}$ = ±20 V | | | ±10 | µA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DD}$ = $V_{GS}$, $I_D$ = 100 µA | 3 | 4 | 5 | V |
| $R_{DS(on)}$ | Static drain-source on-resistance | $V_{GS}$ = 10 V, $I_D$ = 2 A | | 1.50 | 1.75 | Ω |

1. *Defined by design, not subject to production test.*

**Table 5. Dynamic**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $C_{iss}$ | Input capacitance | $V_{DS}$ = 100 V, f = 1 MHz, $V_{GS}$ = 0 V | - | 177 | - | pF |
| $C_{oss}$ | Output capacitance | | - | 15 | - | pF |
| $C_{rss}$ | Reverse transfer capacitance | | - | 0.3 | - | pF |
| $C_{o(tr)}$ (1) | Equivalent capacitance time related | $V_{DS}$ = 0 to 640 V, $V_{GS}$ = 0 V | - | 33 | - | nC |
| $C_{o(er)}$ (2) | Equivalent capacitance energy related | | - | 12 | - | nC |
| $R_g$ | Intrinsic gate resistance | $V_{DD}$ = 640 V, $I_D$ = 4 A, $V_{GS}$ = 0 to 10 V (see Figure 14. Test circuit for gate charge behavior) | - | 16 | - | nC |
| $Q_g$ | Total gate charge | | - | 5 | - | nC |
| $Q_{gs}$ | Gate-source charge | | - | 1.7 | - | nC |
| $Q_{gd}$ | Gate-drain charge | | - | 2.9 | - | nC |

1. *$C_{o(tr)}$ is a constant capacitance value that gives the same charging time as $C_{oss}$ while $V_{DS}$ is rising from 0 to 80% $V_{DSS}$.*
2. *$C_{o(er)}$ is a constant capacitance value that gives the same stored energy as $C_{oss}$ while $V_{DS}$ is rising from 0 to 80% $V_{DSS}$.*

**Table 6. Switching times**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{d(on)}$ | Turn-on delay time | $V_{DD}$ = 400 V, $I_D$ = 2 A, $R_G$ = 4.7 Ω, $V_{GS}$ = 10 V (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform) | - | 12.7 | - | ns |
| $t_r$ | Rise time | | - | 11.7 | - | ns |
| $t_{d(off)}$ | Turn-off delay time | | - | 23 | - | ns |
| $t_f$ | Fall time | | - | 14.8 | - | ns |


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**Table 7. Source-drain diode**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{SD}$ | Source-drain current | | - | | 4 | A |
| $I_{SDM}$ (1) | Source-drain current (pulsed) | | - | | 16 | A |
| $V_{SD}$ (2) | Forward on voltage | $I_{SD}$ = 4 A, $V_{GS}$ = 0 V | - | | 1.5 | V |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$ = 4 A, di/dt = 100 A/µs, $V_{DD}$ = 60 V (see Figure 15. Test circuit for inductive load switching and diode recovery times) | - | 265 | | ns |
| $Q_{rr}$ | Reverse recovery charge | | - | 1.59 | | µC |
| $I_{RRM}$ | Reverse recovery current | | - | 12 | | A |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$ = 4 A, di/dt = 100 A/µs, $V_{DD}$ = 60 V, $T_J$ = 150 °C (see Figure 15. Test circuit for inductive load switching and diode recovery times) | - | 386 | | ns |
| $Q_{rr}$ | Reverse recovery charge | | - | 2.18 | | µC |
| $I_{RRM}$ | Reverse recovery current | | - | 11.3 | | A |

1. *Pulse width limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

**Table 8. Gate-source Zener diode**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)GSO}$ | Gate-source breakdown voltage | $I_{GS}$ = ±1 mA, $I_D$ = 0 A | 30 | - | - | V |

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.


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## 2.1 Electrical characteristics (curves)

**Figure 1. Safe operating area**

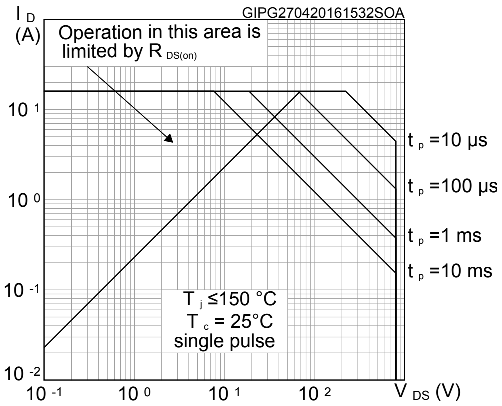


**Figure 2. Thermal impedance**

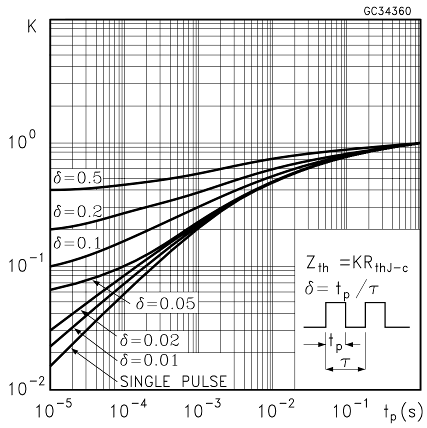


**Figure 3. Output characteristics**

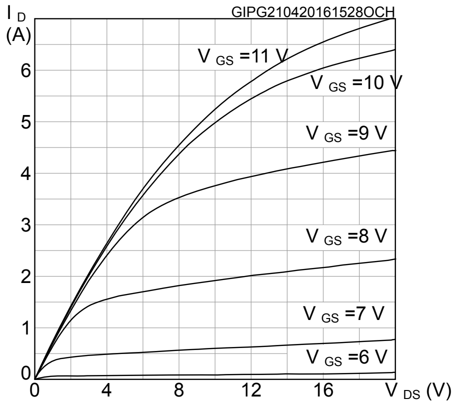


**Figure 4. Transfer characteristics**

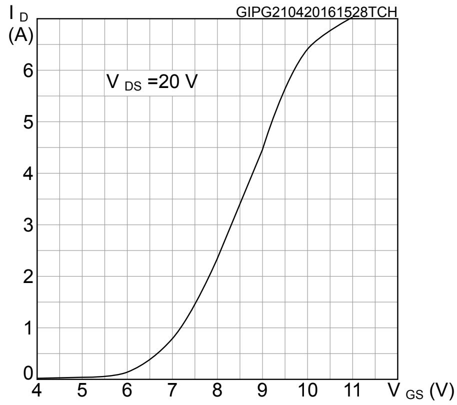


**Figure 5. Gate charge vs gate-source voltage**

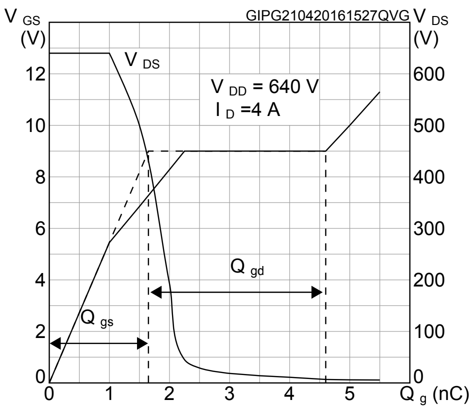


**Figure 6. Static drain-source on-resistance**

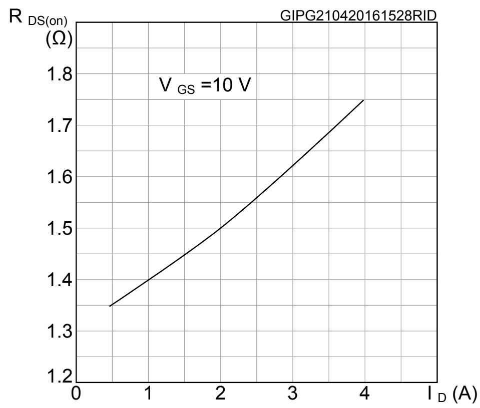



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Figure 7. Capacitance variations

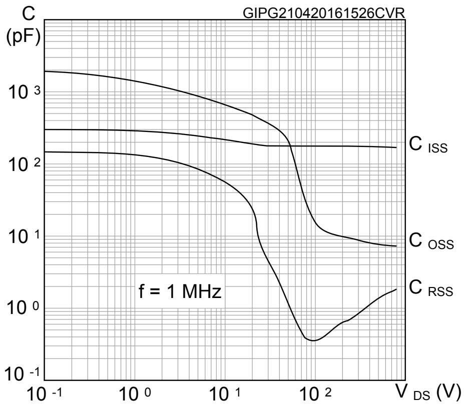



Figure 8. Normalized gate threshold voltage vs temperature

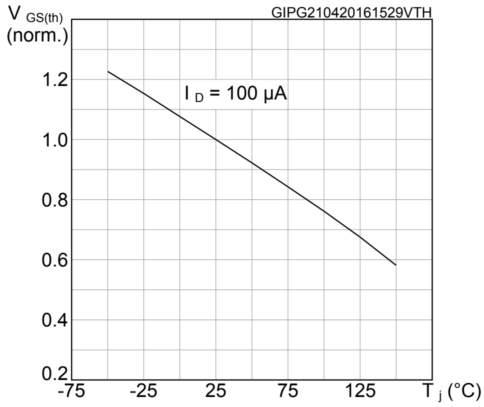



Figure 9. Normalized on-resistance vs temperature

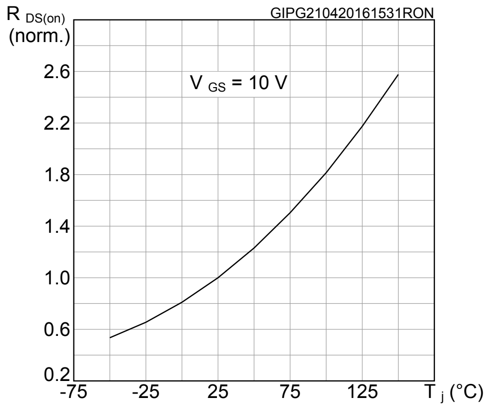



Figure 10. Normalized $V_{(BR)DSS}$ vs temperature

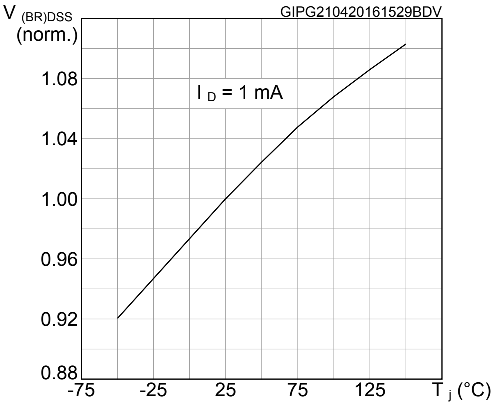



Figure 11. Maximum avalanche energy vs starting $T_J$

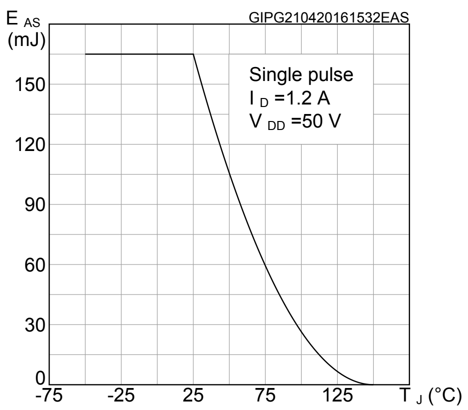
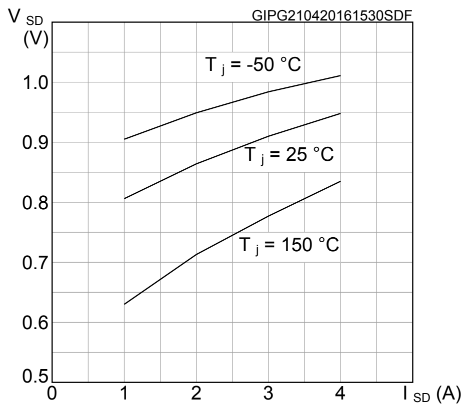



Figure 12. Source-drain diode forward characteristics





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# 3 Test circuits

**Figure 13. Test circuit for resistive load switching times**

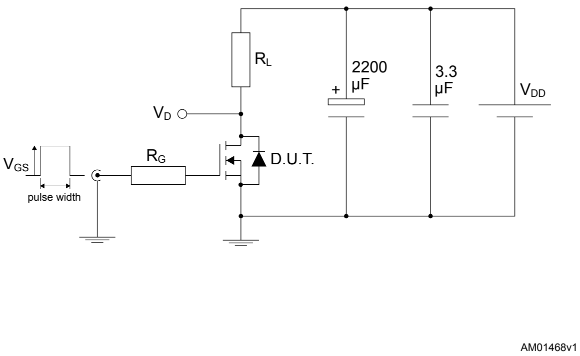



**Figure 14. Test circuit for gate charge behavior**

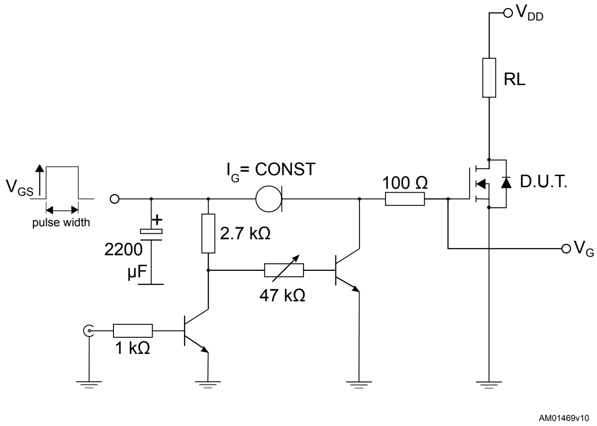



**Figure 15. Test circuit for inductive load switching and diode recovery times**

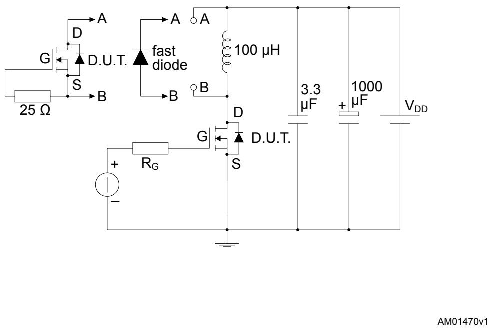



**Figure 16. Unclamped inductive load test circuit**

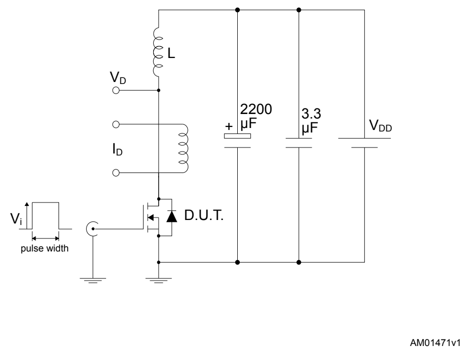



**Figure 17. Unclamped inductive waveform**

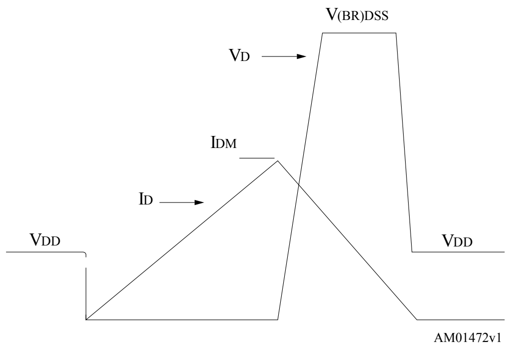
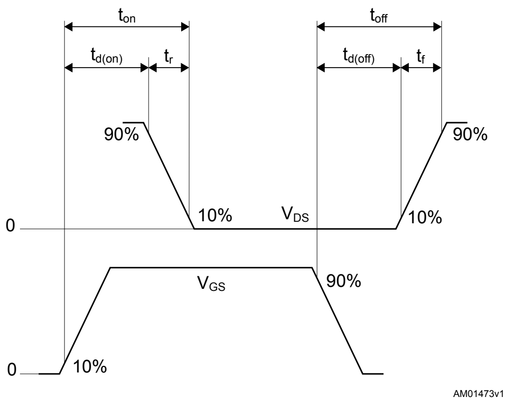



**Figure 18. Switching time waveform**





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# 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.


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## 4.1 DPAK (TO-252) type A package information

**Figure 19. DPAK (TO-252) type A package outline**

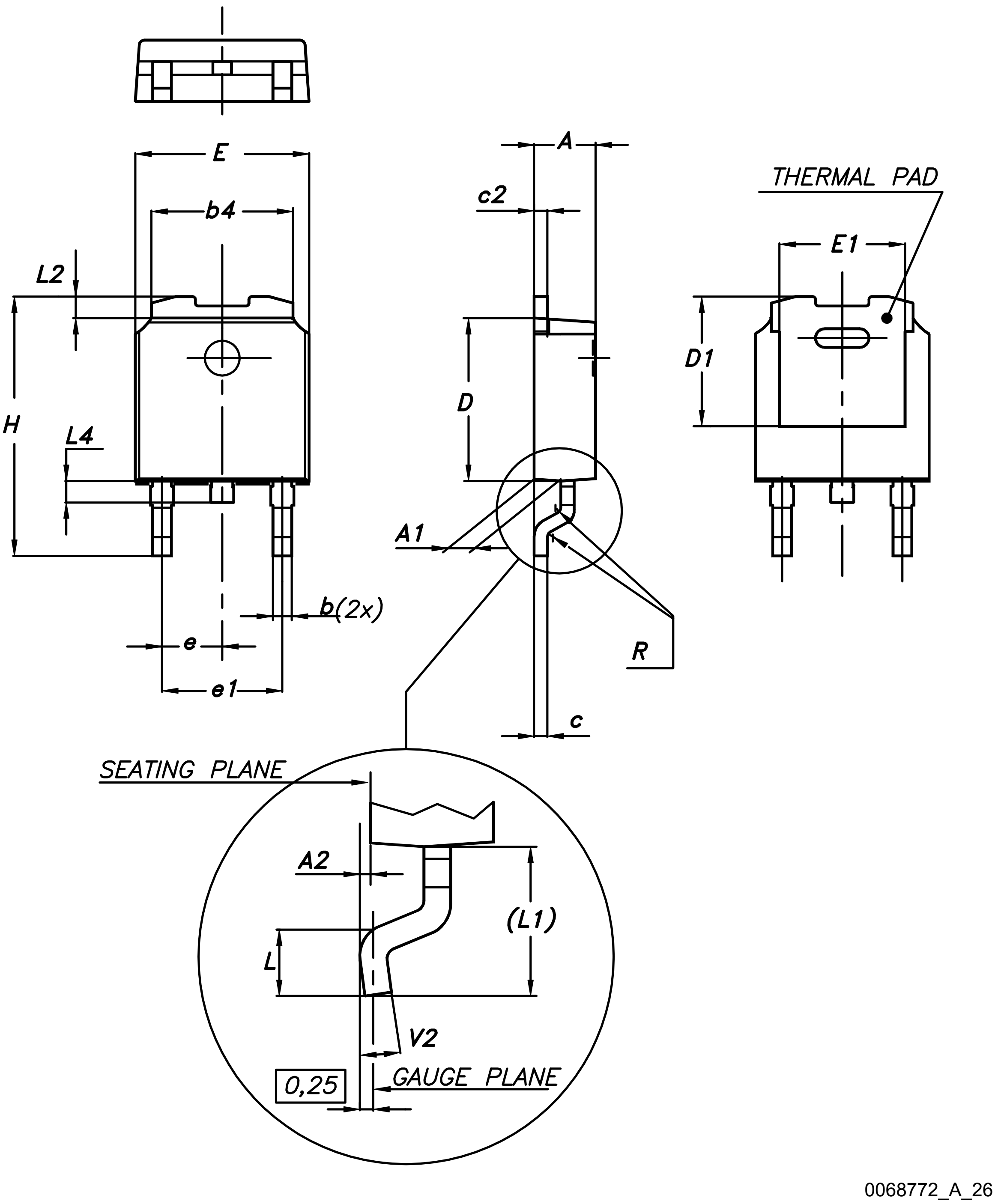



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**Table 9. DPAK (TO-252) type A mechanical data**

| Dim. | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 2.20 | | 2.40 |
| A1 | 0.90 | | 1.10 |
| A2 | 0.03 | | 0.23 |
| b | 0.64 | | 0.90 |
| b4 | 5.20 | | 5.40 |
| c | 0.45 | | 0.60 |
| c2 | 0.48 | | 0.60 |
| D | 6.00 | | 6.20 |
| D1 | 4.95 | 5.10 | 5.25 |
| E | 6.40 | | 6.60 |
| E1 | 4.60 | 4.70 | 4.80 |
| e | 2.159 | 2.286 | 2.413 |
| e1 | 4.445 | 4.572 | 4.699 |
| H | 9.35 | | 10.10 |
| L | 1.00 | | 1.50 |
| (L1) | 2.60 | 2.80 | 3.00 |
| L2 | 0.65 | 0.80 | 0.95 |
| L4 | 0.60 | | 1.00 |
| R | | 0.20 | |
| V2 | 0° | | 8° |


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## 4.2 DPAK (TO-252) type C package information

Figure 20. DPAK (TO-252) type C package outline

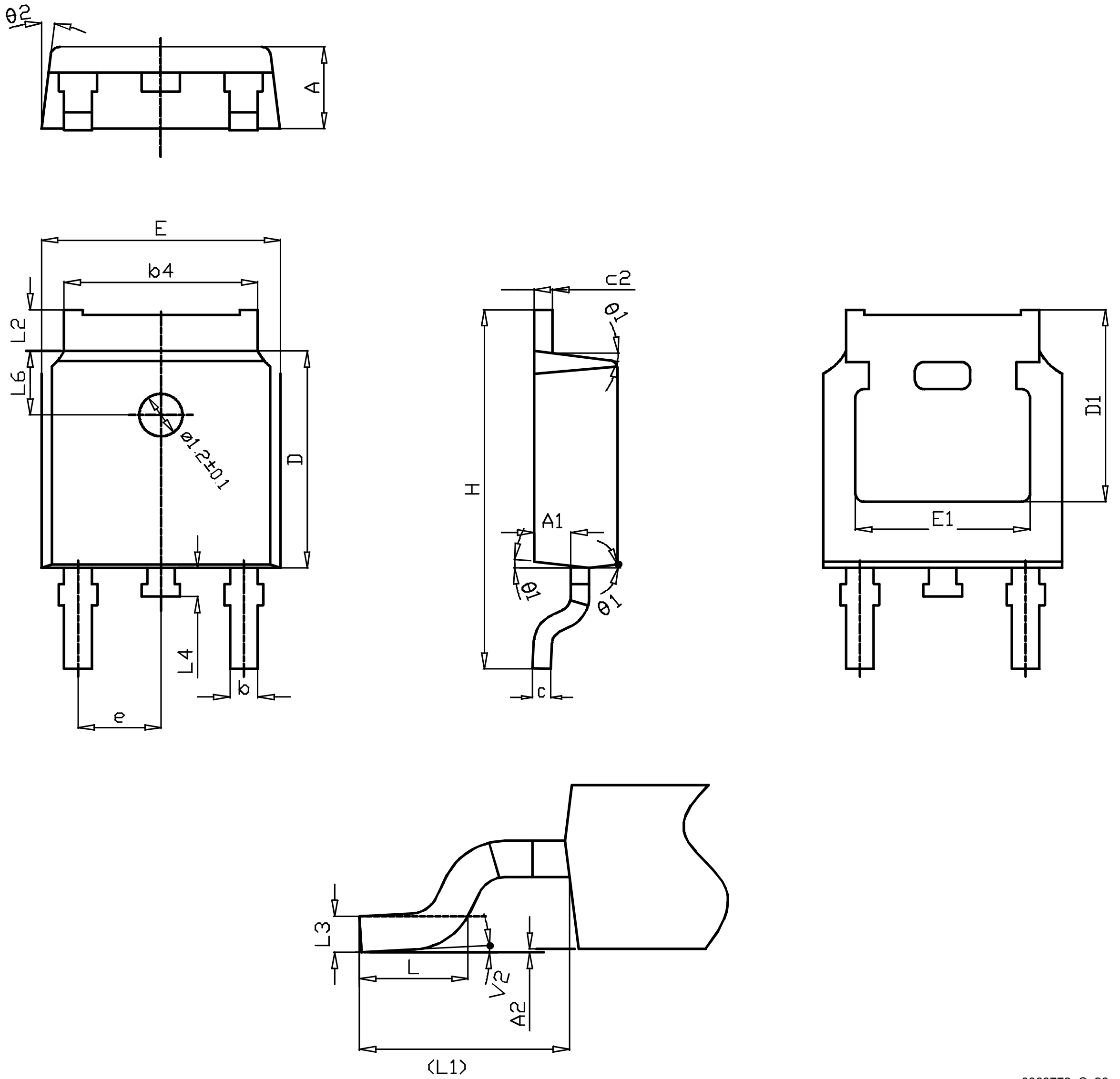



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Table 10. **DPAK (TO-252) type C mechanical data**

| Dim. | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 2.20 | 2.30 | 2.38 |
| A1 | 0.90 | 1.01 | 1.10 |
| A2 | 0.00 | | 0.10 |
| b | 0.72 | | 0.85 |
| b4 | 5.13 | 5.33 | 5.46 |
| c | 0.47 | | 0.60 |
| c2 | 0.47 | | 0.60 |
| D | 6.00 | 6.10 | 6.20 |
| D1 | 5.25 | | |
| E | 6.50 | 6.60 | 6.70 |
| E1 | 4.70 | | |
| e | 2.186 | 2.286 | 2.386 |
| H | 9.80 | 10.10 | 10.40 |
| L | 1.40 | 1.50 | 1.70 |
| L1 | | 2.90 REF | |
| L2 | 0.90 | | 1.25 |
| L3 | | 0.51 BSC | |
| L4 | 0.60 | 0.80 | 1.00 |
| L6 | | 1.80 BSC | |
| θ1 | 5° | 7° | 9° |
| θ2 | 5° | 7° | 9° |
| V2 | 0° | | 8° |


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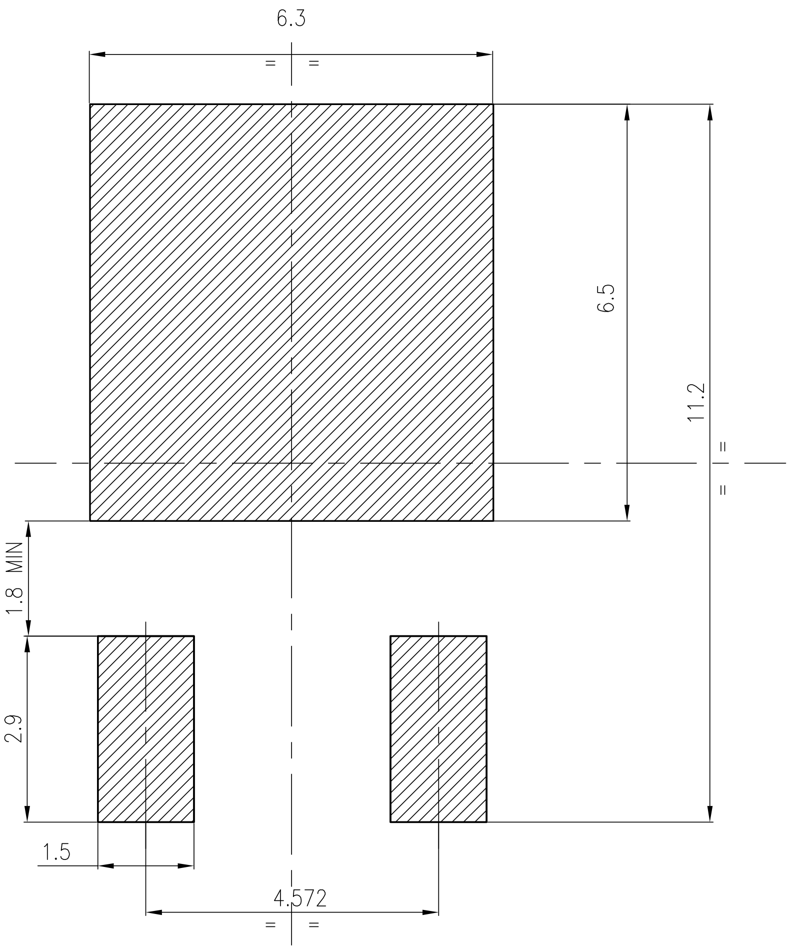
**Figure 21. DPAK (TO-252) recommended footprint (dimensions are in mm)**

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## 4.3 DPAK (TO-252) packing information

Figure 22. **DPAK (TO-252) tape outline**

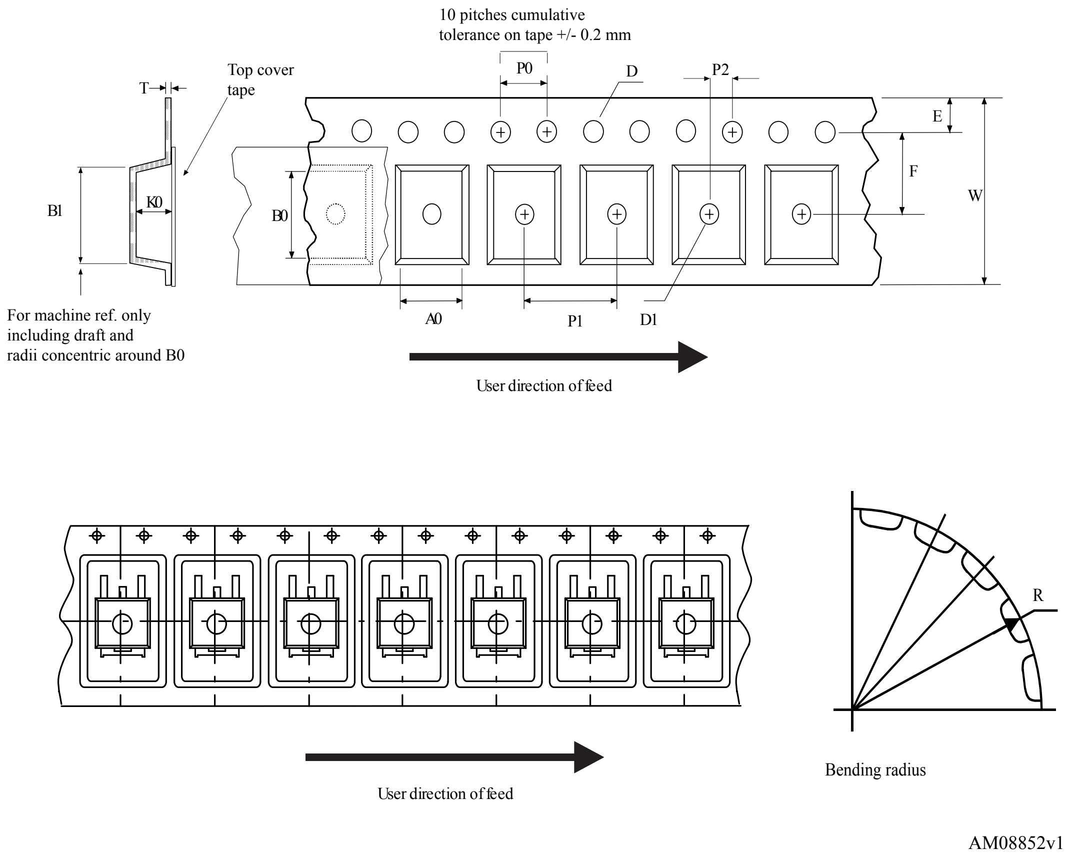



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**Figure 23.** DPAK (TO-252) reel outline

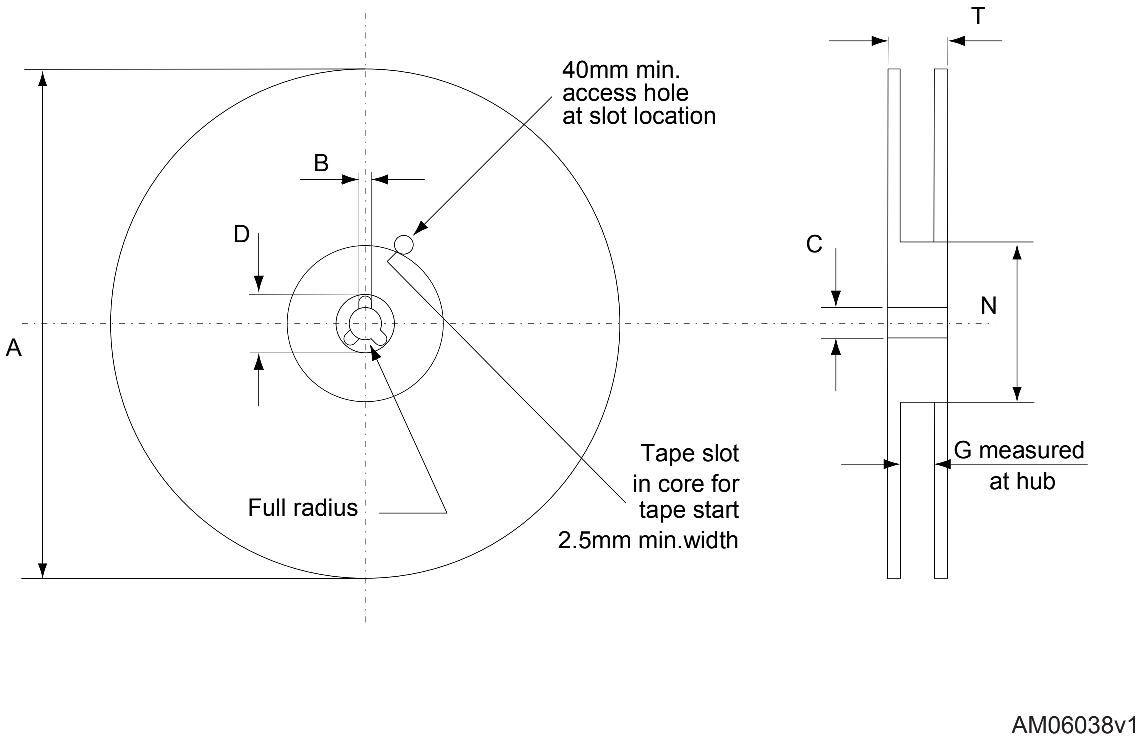


**Table 11.** DPAK (TO-252) tape and reel mechanical data

| Tape | | | Reel | | |
|---|---|---|---|---|---|
| Dim. | mm | | Dim. | mm | |
| | Min. | Max. | | Min. | Max. |
| A0 | 6.8 | 7 | A | | 330 |
| B0 | 10.4 | 10.6 | B | 1.5 | |
| B1 | | 12.1 | C | 12.8 | 13.2 |
| D | 1.5 | 1.6 | D | 20.2 | |
| D1 | 1.5 | | G | 16.4 | 18.4 |
| E | 1.65 | 1.85 | N | 50 | |
| F | 7.4 | 7.6 | T | | 22.4 |
| K0 | 2.55 | 2.75 | | | |
| P0 | 3.9 | 4.1 | Base qty. | | 2500 |
| P1 | 7.9 | 8.1 | Bulk qty. | | 2500 |
| P2 | 1.9 | 2.1 | | | |
| R | 40 | | | | |
| T | 0.25 | 0.35 | | | |
| W | 15.7 | 16.3 | | | |


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## Revision history

Table 12. **Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 08-Jan-2016 | 1 | First release. |
| 09-May-2016 | 2 | Modified: title<br>Modified: *Table 1. Absolute maximum ratings*, *Table 2. Thermal data*, *Table 4. On/off-state*, *Table 5. Dynamic*, *Table 6. Switching times* and *Table 7. Source-drain diode*.<br>Added: *Section 2.1 Electrical characteristics (curves)*.<br>Modified: *Section 3 Test circuits.*<br>Minor text changes |
| 03-Apr-2019 | 3 | Updated *Section 4 Package information*.<br>Minor text changes. |
| 05-Jul-2019 | 4 | Updated Section 4 Package information.<br>Minor text changes. |


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