

STF16N60M6

N-channel 600 V, 0.26 Ω typ., 12 A MDmesh™ M6 Power MOSFET in a TO-220FP package

Datasheet - production data

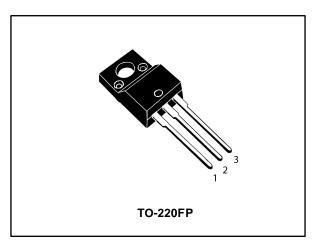
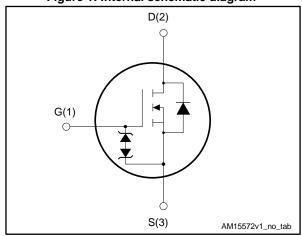


Figure 1: Internal schematic diagram



Features

Order code	Order code V _{DS} R _{DS(on}		l _D
STF16N60M6	600 V	0.32 Ω	12 A

- Reduced switching losses
- Lower R_{DS(on)} x area vs previous generation
- Low gate input resistance
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications
- LLC converters
- Boost PFC converters

Description

The new MDmeshTM M6 technology incorporates the most recent advancements to the well-known and consolidated MDmesh family of SJ MOSFETs. STMicroelectronics builds on the previous generation of MDmesh devices through its new M6 technology, which combines excellent $R_{DS(on)}$ * area improvement with one of the most effective switching behaviors available, as well as a user-friendly experience for maximum endapplication efficiency.

Table 1: Device summary

Order code	Marking	Package	Packing
STF16N60M6	16N60M6	TO-220FP	Tube

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STF16N60M6 Electrical ratings

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
Vgs	Gate-source voltage	±25	V
I_D	Drain current (continuous) at T _c = 25 °C	12 ⁽¹⁾	Α
ΙD	Drain current (continuous) at T _c = 100 °C	7.6 ⁽¹⁾	Α
I _{DM}	Drain current (pulsed)	32 ⁽¹⁾⁽²⁾	Α
P _{TOT}	Total dissipation at $T_c = 25$ °C	25	W
dv/dt ⁽³⁾	Peak diode recovery voltage slope	15	V/ns
dv/dt (4)	MOSFET dv/dt ruggedness	50	V/115
V _{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; T_C = 25 °C)	2.5	kV
T _{stg}	Storage temperature range	FF to 150	°C
Tj	Operating junction temperature range	-55 to 150	

Notes:

Table 3: Thermal data

Symbol	nbol Parameter		Unit
R _{thj-case}	Thermal resistance junction-case	5	°C/W
R _{thj-amb}	Thermal resistance junction-ambient	62.5	

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I _{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T _{jmax})	2.5	Α
Eas	Single pulse avalanche energy (starting $T_j = 25$ °C, $I_D = I_{AR}$; $V_{DD} = 50$ V)	110	mJ

⁽¹⁾ Limited by maximum junction temperature.

⁽²⁾Pulse width limited by safe operating area.

 $^{^{(3)}}I_{SD} \leq$ 12 A, di/dt \leq 400 A/ μ s; VDS(peak) < V(BR)DSS, VDD = 400 V

 $^{^{(4)}}$ V_{DS} ≤ 480 V

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 5: On /off states

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0 \text{ V}, I_D = 1 \text{ mA}$	600			V
	Zaro goto voltogo droin	$V_{GS} = 0 \text{ V}, V_{DS} = 600 \text{ V}$			1	
IDSS	Zero gate voltage drain current	$V_{GS} = 0 \text{ V}, V_{DS} = 600 \text{ V},$ $T_{C} = 125 \text{ °C}$ (1)			100	μΑ
I _{GSS}	Gate-body leakage current	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 25 \text{ V}$			±5	μΑ
V _{GS(th)}	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250 \mu A$	3.25	4	4.75	V
R _{DS(on)}	Static drain-source on- resistance	V _{GS} = 10 V, I _D = 6 A		0.26	0.32	Ω

Notes:

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
Ciss	Input capacitance		ı	575	ı	
Coss	Output capacitance	V _{GS} = 100 V, f = 1 MHz,	ı	33	ı	pF
Crss	Reverse transfer capacitance	Ves = 0 V	-	3	-	ρı
Coss eq. (1)	Equivalent output capacitance	V _{DS} = 0 to 480 V, V _{GS} = 0 V	1	104	1	pF
R _G	Intrinsic gate resistance	f = 1 MHz open drain	ı	5.2	ı	Ω
Qg	Total gate charge	$V_{DD} = 480 \text{ V}, I_{D} = 12 \text{ A}, V_{GS} = 0$	ı	16.7	ı	
Q _{gs}	Gate-source charge	to 10 V (see Figure 15: "Test circuit for gate charge	-	3.5	ı	nC
Q_{gd}	Gate-drain charge	behavior")	-	9.4	-	

Notes:

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t _{d(on)}	Turn-on delay time	$V_{DD} = 300 \text{ V}, I_D = 6 \text{ A}$	ı	13	ı	
tr	Rise time	$R_G = 4.7 \Omega$, $V_{GS} = 10 V$ (see Figure 14: "Test circuit for	-	7.6	-	
t _{d(off)}	Turn-off delay time	resistive load switching times"	-	19.8	-	ns
t _f	Fall time	and Figure 19: "Switching time waveform")	1	6.8	1	

 $^{^{(1)}}$ Defined by design, not subject to production test.

 $^{^{(1)}}$ C_{oss eq.} is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

Table 8: Source drain diode

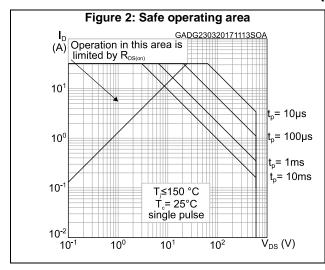
Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I _{SD}	Source-drain current		-		12	Α
I _{SDM} ⁽¹⁾	Source-drain current (pulsed)		-		32	Α
V _{SD} ⁽²⁾	Forward on voltage	V _{GS} = 0 V, I _{SD} = 12 A	-		1.6	V
t _{rr}	Reverse recovery time	I _{SD} = 12 A, di/dt = 100 A/µs,	-	210		ns
Qrr	Reverse recovery charge	V _{DD} = 60 V (see Figure 16: "Test circuit for inductive load	-	1.7		μC
I _{RRM}	Reverse recovery current	switching and diode recovery times")	-	13.8		Α
t _{rr}	Reverse recovery time	I _{SD} = 12 A, di/dt = 100 A/µs,	-	310		ns
Qrr	Reverse recovery charge	$V_{DD} = 60 \text{ V}, T_j = 150 ^{\circ}\text{C} \text{ (see}$ Figure 16: "Test circuit for	-	3.2		μC
I _{RRM}	Reverse recovery current	inductive load switching and diode recovery times")	-	15.4		Α

Notes:

 $^{^{(1)}}$ Pulse width is limited by safe operating area.

 $^{^{(2)}}$ Pulse test: pulse duration = 300 $\mu s,$ duty cycle 1.5%.

2.1 Electrical characteristics (curves)



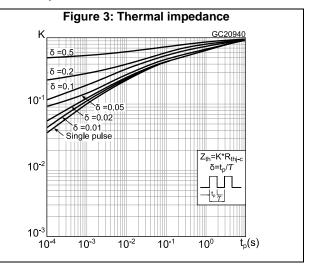
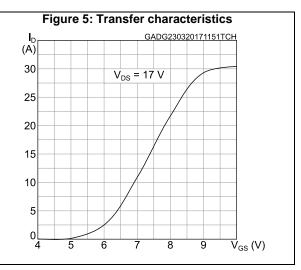
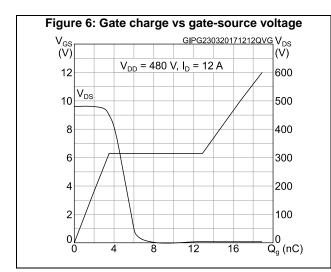
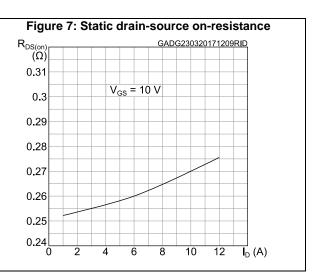


Figure 4: Output characteristics GADG230320171114OCH **I**_D (A) $V_{GS} = 9, 10 \text{ V}$ 30 25 8 V 20 15 7 V 10 5 6 V 8 12 16 $\overline{V}_{DS}(V)$







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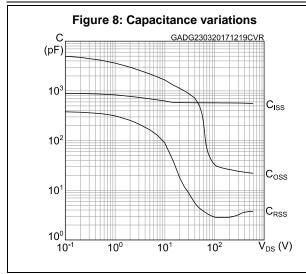


Figure 9: Normalized gate threshold voltage vs temperature $V_{GS(th)}$ (norm.)

1.1 $I_D = 250 \ \mu A$ 1.1

0.9

0.8

0.7

0.6

-75

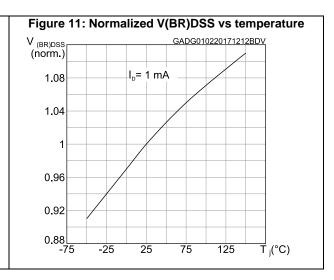
-25

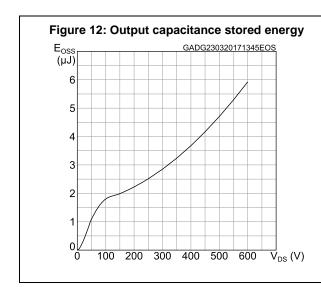
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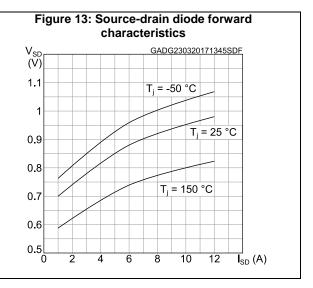
75

125 T_j (°C)

Figure 10: Normalized on-resistance vs temperature $R_{DS(on)}$ (norm.) $V_{GS} = 10 \text{ V}$ $V_{GS} = 10$







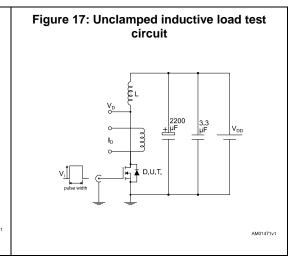


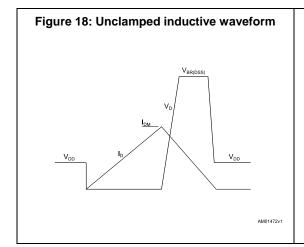
Test circuits STF16N60M6

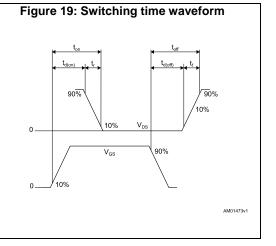
3 Test circuits

Figure 14: Test circuit for resistive load switching times

Figure 16: Test circuit for inductive load switching and diode recovery times







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STF16N60M6 Package information

4 Package information

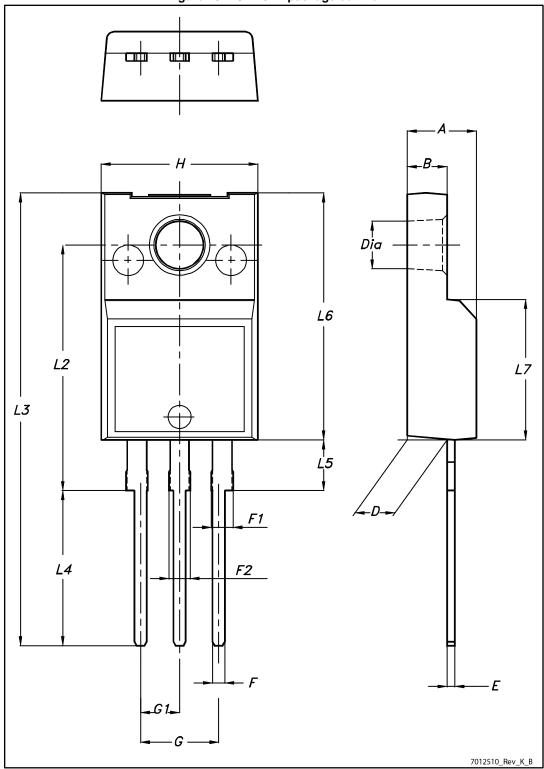
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: **www.st.com**. ECOPACK® is an ST trademark.



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4.1 TO-220FP package information

Figure 20: TO-220FP package outline



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Table 9: TO-220FP package mechanical data

Dim	mm		
Dim.	Min.	Тур.	Max.
А	4.4		4.6
В	2.5		2.7
D	2.5		2.75
Е	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
Н	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2



Revision history STF16N60M6

5 Revision history

Table 10: Document revision history

Date	Revision	Changes
23-Mar-2017	1	First release.

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