



## Dual Operational Amplifier and Voltage Reference

### OPERATIONAL AMPLIFIER

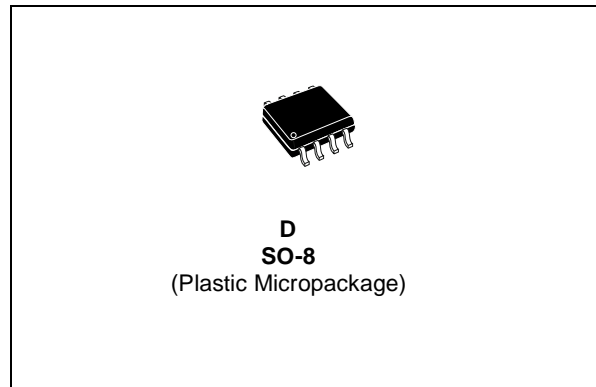
- **LOW INPUT OFFSET VOLTAGE** : 0.5mV typ.
- **LOW SUPPLY CURRENT** : 350 $\mu$ A/op. (@  $V_{CC} = 5V$ )
- **MEDIUM BANDWIDTH** (unity gain) : 0.9MHz
- **LARGE OUTPUT VOLTAGE SWING** : 0V to ( $V_{CC} - 1.5V$ )
- **INPUT COMMON MODE VOLTAGE RANGE INCLUDES GROUND**
- **WIDE POWER SUPPLY RANGE** : 3 to 32V  $\pm 1.5$  TO  $\pm 16V$
- **1.5kV ESD PROTECTION**
- **VOLTAGE REFERENCE**
- **FIXED OUTPUT VOLTAGE REFERENCE 2.5V**
- **$\pm 0.4\%$  OR  $\pm 0.7\%$  VOLTAGE PRECISION**
- **SINK CURRENT CAPABILITY** : 1 to 100mA
- **TYPICAL OUTPUT IMPEDANCE** : 0.2 $\Omega$

### DESCRIPTION

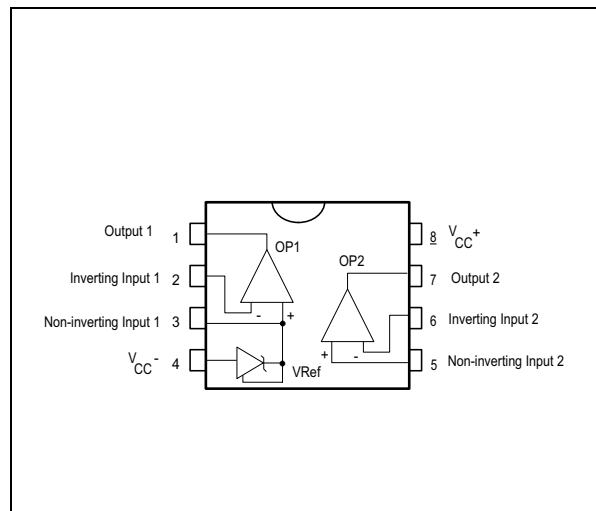
The TSM103W is a monolithic IC that includes one independent op-amp and another op-amp for which the non-inverting input is wired to a 2.5V fixed Voltage Reference. This device offers both space and cost savings in many applications such as power supply management or data acquisition systems.

### ORDER CODE

Part Number	Temperature Range	Package	Packaging
TSM103WID	-40, +105 $^{\circ}$ C	SO-8	Tube
TSM103WIDT			Tape & Reel
TSM103WAID			Tube
TSM103WAIDT			Tape & Reel



### PIN CONNECTIONS (top view)



## 1 ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage	36	V
$V_{id}$	Differential Input Voltage	$V_{CC} + 0.6$	V
$V_i$	Input VoltageL	-0.3 to $V_{CC} + 0.3V$	V
$T_{stg}$	Storage temperature range	-65 to + 150	°C
$I_k$	Continuous cathode current range	-100 to 150	mA
$T_j$	Maximum Junction Temperature	150	°C
$R_{thja}$	Thermal Resistance Junction to Ambient (SO package)	175	°C/W
$T_l$	Maximum Lead Temperature (10 seconds maximum)	260	°C
ESD	Electrostatic Discharge Protection	1.5	kV

## OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
$V_{CC}$	DC Supply Conditions	3 to 32	V
$I_k$	Vref Cathode Current	1 to 100	mA
$T_{oper}$	Operating Free-air Temperature Range	-40°C, +105°C	°C

## 2 ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Unit
$I_{CC}$	Total Supply Current, excluding Current in the Voltage Reference V <sub>CC+</sub> = 5V, no load T <sub>min.</sub> < T <sub>amb</sub> < T <sub>max.</sub> V <sub>CC+</sub> = 30V, no load T <sub>min.</sub> < T <sub>amb</sub> < T <sub>max.</sub>		0.7	1.2 2	mA

**OPERATOR 2** (independent op-amp)V<sub>CC+</sub> = +5V, V<sub>CC</sub> = Ground, V<sub>o</sub> = 1.4V, T<sub>amb</sub> = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_{io}$	Input Offset Voltage V <sub>icm</sub> = 0V TSM103WA, T <sub>amb</sub> = 25° T <sub>min.</sub> ≤ T <sub>amb</sub> ≤ T <sub>max.</sub> TSM103W, T <sub>amb</sub> = 25° T <sub>min.</sub> ≤ T <sub>amb</sub> ≤ T <sub>max.</sub>		0.5 1	2 3 4 5	mV
DV <sub>io</sub>	Input Offset Voltage Drift		7		μV/°C
$I_{io}$	Input Offset Current T <sub>min.</sub> ≤ T <sub>amb</sub> ≤ T <sub>max.</sub>		2	75 150	nA
$I_{ib}$	Input Bias Current T <sub>min.</sub> ≤ T <sub>amb</sub> ≤ T <sub>max.</sub>		20	150 200	nA
Avd	Large Signal Voltage Gain V <sub>CC</sub> = 15V, R <sub>L</sub> = 2k, V <sub>o</sub> = 1.4V to 11.4V T <sub>min.</sub> ≤ T <sub>amb</sub> ≤ T <sub>max.</sub>	50 25	100		V/mV
SVR	Supply Voltage Rejection Ratio V <sub>CC</sub> = 5V to 30V	65	100		dB
V <sub>icm</sub>	Input Common Mode Voltage Range V <sub>CC</sub> = +30V - see note <sup>1</sup> T <sub>min.</sub> ≤ T <sub>amb</sub> ≤ T <sub>max.</sub>	0 0		(V <sub>CC+</sub> ) -1.5 (V <sub>CC+</sub> ) -2	V
CMR	Common Mode Rejection Ratio T <sub>min.</sub> ≤ T <sub>amb</sub> ≤ T <sub>max.</sub>	70 60	85		dB
$I_{source}$	Output Current Source V <sub>CC</sub> = +15V, V <sub>o</sub> = 2V, V <sub>id</sub> = +1V	20	40		mA
$I_o$	Short Circuit to Ground V <sub>CC</sub> = +15V		40	60	mA
$I_{sink}$	Output Current Sink V <sub>id</sub> = -1V, V <sub>CC</sub> = +15V, V <sub>o</sub> = 2V V <sub>CC</sub> = +15V, V <sub>o</sub> = 0.2V	10 12	20 50		mA μA
V <sub>OH</sub>	High Level Output Voltage V <sub>CC+</sub> = 30V T <sub>amb</sub> = 25°C, R <sub>L</sub> = 2k T <sub>min.</sub> ≤ T <sub>amb</sub> ≤ T <sub>max.</sub> T <sub>amb</sub> = 25°C, R <sub>L</sub> = 10k T <sub>min.</sub> ≤ T <sub>amb</sub> ≤ T <sub>max.</sub>	26 26 27 27	27 28		V
V <sub>OL</sub>	Low Level Output Voltage R <sub>L</sub> = 10k T <sub>min.</sub> ≤ T <sub>amb</sub> ≤ T <sub>max.</sub>		5	20 20	mV
SR	Slew Rate at Unity Gain V <sub>i</sub> = 0.5 to 3V, V <sub>CC</sub> = 15V R <sub>L</sub> = 2k, C <sub>L</sub> = 100pF, unity gain	0.2	0.4		V/μs

Symbol	Parameter	Min.	Typ.	Max.	Unit
GBP	Gain Bandwidth Product $V_{CC} = 30V, R_L = 2k, C_L = 100pF$ $f = 100kHz, V_{in} = 10mV$	0.5	0.9		MHz
THD	Total Harmonic Distortion $f = 1kHz$ $A_V = 20dB, R_L = 2k, V_{CC} = 30V$ $C_L = 100pF, V_o = 2V_{pp}$		0.02		%
$e_n$	Equivalent Input Noise Voltage $f = 1kHz, R_s = 100\Omega$ $V_{CC} = 30V$		50		nV/ $\sqrt{Hz}$

1) The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is  $V_{CC}^+ - 1.5V$ . Both inputs can go to  $V_{CC} + 0.3V$  without damage.

### OPERATOR 1 (op-amp with non-inverting input connected to the internal Vref)

$V_{CC}^+ = +5V, V_{CC}^- = \text{Ground}, T_{amb} = 25^\circ C$  (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_{io}$	Input Offset Voltage $V_{icm} = 0V$ TSM103WA, $T_{amb} = 25^\circ$ $T_{min.} \leq T_{amb} \leq T_{max.}$ TSM103W, $T_{amb} = 25^\circ$ $T_{min.} \leq T_{amb} \leq T_{max.}$		0.5 1	2 3 4 5	mV
$DV_{io}$	Input Offset Voltage Drift		7		$\mu V/^\circ C$
$I_{ib}$	Input Bias Current negative input		20		nA
Avd	Large Signal Voltage Gain $V_{CC} = 15V, R_L = 2k, V_o = 1.4V \text{ to } 11.4V$ $T_{min.} \leq T_{amb} \leq T_{max.}$		100		V/mV
SVR	Supply Voltage Rejection Ratio $V_{icm} = 0V$ $V_{CC}^+ = 5V \text{ to } 30V$	65	100		dB
$I_{source}$	Output Current Source $V_o = 2V$ $V_{CC} = +15V, V_{id} = +1V$	20	40		mA
$I_o$	Short Circuit to Ground $V_{CC} = +15V$		40	60	mA
$I_{sink}$	Output Current Sink $V_{id} = -1V,$ $V_{CC} = +15V, V_o = 2V$ $V_{CC} = +15V, V_o = 0.2V$	10 12	20 50		mA $\mu A$
$V_{OH}$	High Level Output Voltage $V_{CC}^+ = 30V$ $T_{amb} = 25^\circ C, R_L = 2k$ $T_{min.} \leq T_{amb} \leq T_{max.}$ $T_{amb} = 25^\circ C, R_L = 10k$ $T_{min.} \leq T_{amb} \leq T_{max.}$	26 26 27 27	27 28		V
$V_{OL}$	Low Level Output Voltage $R_L = 10k$ $T_{min.} \leq T_{amb} \leq T_{max.}$		5	20 20	mV
SR	Slew Rate at Unity Gain $V_i = 0.5 \text{ to } 2V, V_{CC} = 15V$ $R_L = 2k, C_L = 100pF, \text{ unity gain}$	0.2	0.4		V/ $\mu s$

Symbol	Parameter	Min.	Typ.	Max.	Unit
GBP	Gain Bandwidth Product $V_{CC} = 30V, R_L = 2k, C_L = 100pF$ $f = 100kHz, V_{in} = 10mV$	0.5	0.9		MHz
THD	Total Harmonic Distortion $f = 1kHz$ $A_V = 20dB, R_L = 2k, V_{CC} = 30V$ $C_L = 100pF, V_o = 2V_{pp}$		0.02		%

## VOLTAGE REFERENCE

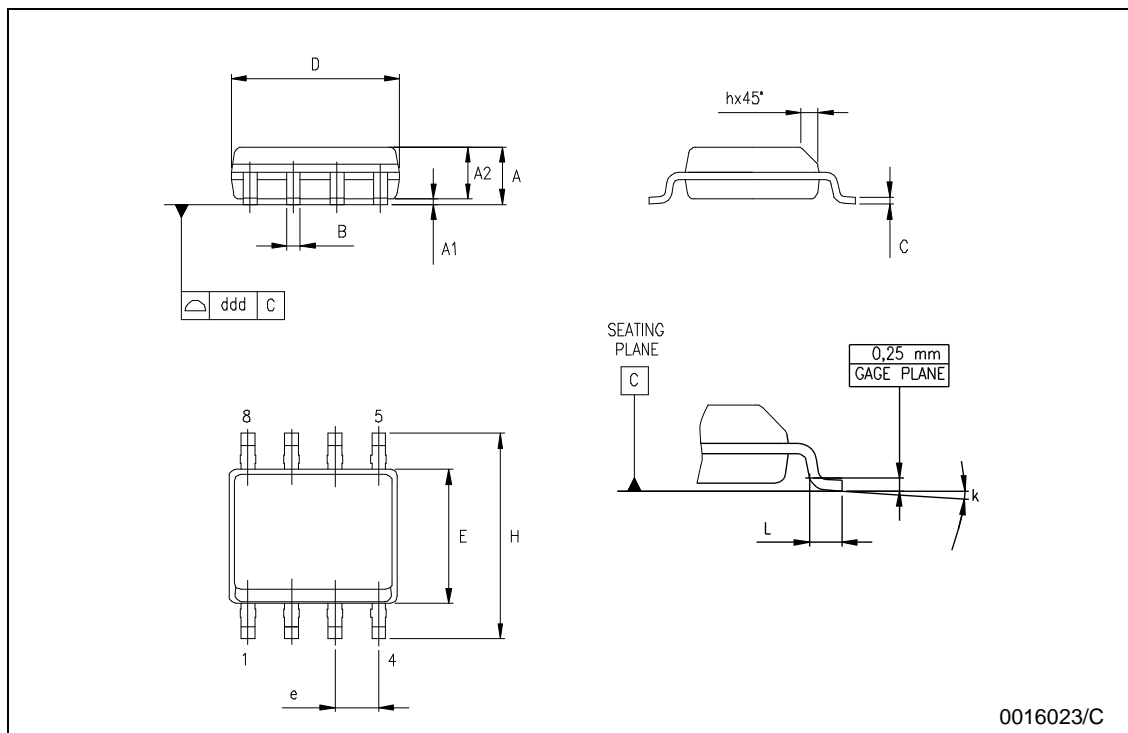
Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_{ref}$	Reference Input Voltage, $I_k = 10mA$ TSM103WA $\pm 0.4\%$ $T_{amb} = 25^\circ C$ $T_{min.} \leq T_{amb} \leq T_{max.}$ TSM103W $\pm 0.7\%$ $T_{amb} = 25^\circ C$ $T_{min.} \leq T_{amb} \leq T_{max.}$	2.49 2.48 2.482 2.465	2.5 2.500	2.51 2.52 2.518 2.535	V
$\Delta V_{ref}$	Reference Input Voltage Deviation Over Temperature Range $V_{KA} = V_{ref}; I_k = 10mA$ $T_{min.} \leq T_{amb} \leq T_{max.}$		7	30	mV
$I_{min}$	Minimum Cathode Current for Regulation $V_{KA} = V_{ref}$		0.5	1	mA
$ Z_{KA} $	Dynamic Impedance - note <sup>1</sup> $V_{KA} = V_{ref}; \Delta I_K = 1 \text{ to } 100mA, f < 1kHz$		0.2	0.5	$\Omega$

1) The dynamic impedance is defined as  $|Z_{KA}| = \Delta V_{KA} / \Delta I_K$

## PACKAGE MECHANICAL DATA

## SO-8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.04		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D	4.80		5.00	0.189		0.197
E	3.80		4.00	0.150		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	$8^{\circ}$ (max.)					
ddd			0.1			0.04



**3 SUMMARY OF CHANGES**

Date	Revision	Description of Changes
	1-2	First Release
02-April-2004	3	1 - Vid=Vcc+0.6 modified on AMR table - page 2 2 - Add I <sub>k</sub> parameter on AMR table - page 2 3 - Avd test condition equal on both tables Operator 1 & Operator 2 - pages 3 & 4

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